

IXIDM1401 TEST BOARD

The Test Board is designed to test IXIDM1401 Module performance after assembly to separate good products and find draft source of the problem for failed ones. It is a standalone device that does not require any additional equipment except power source to operate.

DESCRIPTION AND BOARD SCHEMATIC

The Test Board consists from two boards – Power Module and MCU Module.

The Power Module is a two-layer surface mount board, which contains connectors to install Device-under-Test (DUT) – IXIDM1401 Module, power regulators to provide required power for DUT and MCU Module, LED Display to visualize test results, connector for MCU Module, and some additional components to adjust DUT output signals to the MCU module input levels.

The MCU Module contains Zilog’s MCU Z8F3281AN024XK and some passive components required to its operation. The Test Board is delivered with MCU Module pre-programmed and installed. MCU Module does not need any attention during test procedure.

The Test Board powers from a single polarity 20 V DC power supply with current limiting to prevent DUT and Test Board damage in case of DUT malfunction. Recommended current limit is at 50 mA – 75 mA level.

Test Board dimensions are 4.5” x 4.5” x 1.2” (L x W x H) without DUT.

Test procedure starts after DUT is installed and START button is pressed once. The Test Board performs 13 tests in sequence in respect to the Table 1. Test results are displayed on LED display after last successful test performed. If DUT fails test, test procedure is automatically interrupted, DUT turned off, and results of the successful tests displayed. If DUT fails first test, all tests will be shown as failed.

Pressing START button twice after failed DUT test displays intermediate results for multistep tests in respect with Table 2 to provide additional information about possible cause of failure.

The Power Module and MCU Module Schematic Diagrams are shown at Appendix 1. Power Module Components location is shown on Figure 1.

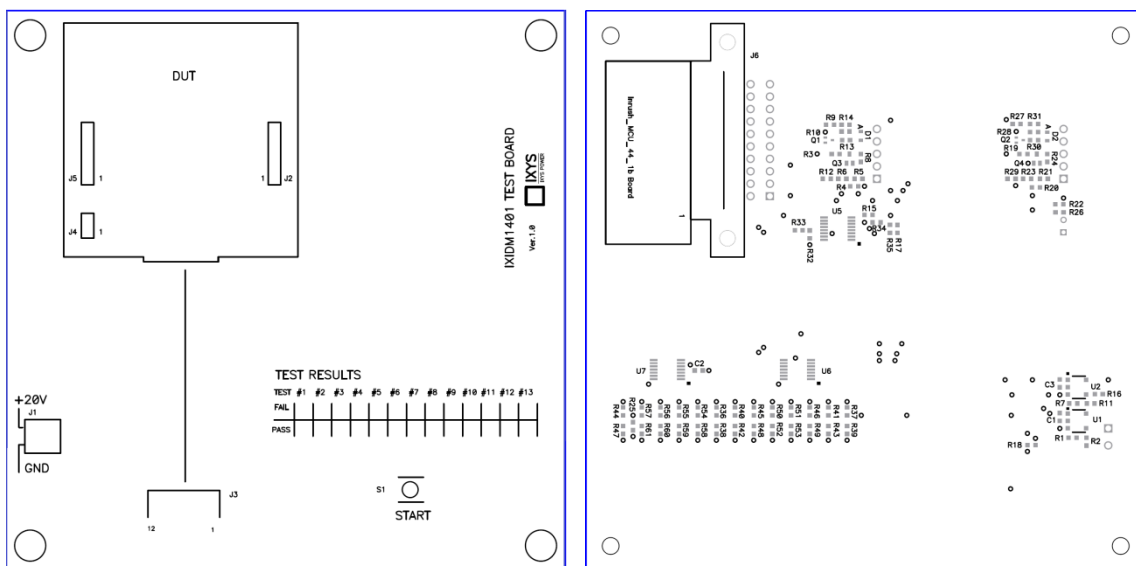


Figure 1: Power Module Components Location (top and bottom layers)

USING THE TEST BOARD

1. DUT Installation

The Test Board contains four connectors to accommodate DUT. Device should be installed in an area marked as "DUT" with receptacles J3, J4 and J5 firmly coupled with corresponding DUT headers. Connector J1 of the DUT should be coupled with connector J2 on the Test Board with a 12-wire 1 mm pitch Flex cable (FFC). Jumper cable 98267-0277 from Molex is recommended. Cable should be inserted in both connectors with bare conductor side up in respect to Test Board top surface. To reduce unnecessary tear and wear of the Test Board, it is recommended to keep flex cable connected to J2 of the Test Board while replacing DUT. Connect flex cable to J1 of the DUT first and install then DUT on the Test Board.

2. Powering IXIDM1401

The Test board should be powered from a unipolar 20 V power supply. Current limit should be set between 50 mA and 75 mA to prevent DUT and Test Board damage in case of DUT malfunction. Power should be provided through connector J1 in respect with polarity shown on the board.

WARNING!

Test board does not have reverse polarity protection. Close attention should be paid to correct polarity connection of the power supply to prevent DUT and Test Board damage.

Power to the DUT is provided during test only. In case of any test failure or after last test performed, DUT is disabled, while test Board remains powered.

3. Testing the Module

Push button "START" to start tests sequence.

4. Reading Test Results

The Test Board contains LED display "TEST RESULTS" with LEDs marked from #1 to #13 in respect to tests performed as shown in the Table 1. Red LEDs indicate failing test, while green LEDs indicate tests that DUT pass. All LEDs are red by default at the start of the test and change color to green in respect to test results. Green LED with biggest number indicates number of the last test DUT pass successfully. If DUT pass all tests, all LEDs become green. If DUT fails first test, all LEDs remain red.

In case of a multistep test failure, Test Board allows get more detailed information about reason of the failure by providing a respective code as a combination of the green/red LEDs in respect with information disclosed in the Table 2. This information is provided to "TEST RESULTS" display after double click on "START" button after test failure is indicated.

"TEST RESULTS" display hold information about least test or additional information about test failure as long as "START" button is not pressed again. If after test failure "START" button pressed once, information about previous tests is cleared and new test of the DUT starts.

Table 1: IXIDM1401 Test Description

Test #	Description	Action	Expected Result	Pass if
1	DUT Pin #J1/1, pin #J1/11 continuity test, short circuit test	Apply pin #J1/1 = 15 V, measure consumed current	$10 \text{ mA} < I_c < 25 \text{ mA}$	Current is in expected range
2	Pin #J1/2 continuity, 3.3 V LDO functionality	Apply pin #J1/1 = 15, measure voltage at pin #J1/2	$3.0 < \text{Pin \#J1/2} < 3.6 =$	Pin #J1/2 voltage is as expected
3	Pin #J1/3 continuity, functionality	Apply pin #J1/1 = 15, measure voltage at pin #J1/2,	$3.0 < \text{Pin \#J1/2} < 3.6 \text{ V}$	Pin #J1/2 new < Pin #J1/2 initial -0.1 V
		Set pin #J1/3 logic high , wait 0.1 s, measure voltage at pin #J1/2	Pin #J1/2 voltage become less than initial value $X_0 < X_0 \text{ ini}$	
4	Pin #J1/10 continuity, channel A functionality, isolated power supply functionality	Apply pin #J1/1 = 15 V, set pin #J1/10 logic high (, measure voltage at pin #J2/1	$18 \text{ V} < \text{pin \#j2/1} < 25 \text{ V}$	Logic state of the pin #J2/1 copy logic state of the pin #J1/10 and logic high voltage is in the expected range
		Set pin #J1/10 logic low, measure voltage at pin #J2/1	$-10 \text{ V} < \text{pin J2/1} < -5 \text{ V}$	
5	Pin #J1/9 continuity, channel B functionality, isolated power supply functionality	Apply pin #J1/1 = 15 V, set pin #J1/9 logic high, measure voltage at pin #J3/1	$18 \text{ V} < \text{pin \#j3/1} < 25 \text{ V}$	Logic state of the pin #J3/1 copy logic state of the pin #J1/9 and logic high voltage is in the expected range
		Set pin #J1/9 logic low, check status of the pin #J2/1	$-10 \text{ V} < \text{pin J3/1} < -5 \text{ V}$	

Table 1: IXIDM1401 Test Description (continued)

Test #	Description	Action	Expected Result	Pass if
6	Pin #J1/7 (Fault1), pin #J1/8 (Fault 2), pin #J1/4 (Fault Reset) continuity and functionality test, primary side under-/over-voltage test	Apply pin #J1/1 = 17 V, set pin #J1/10 logic high/low	Pin #J2/1 should not change logic state from low, pin #J1/7 (Fault 1) should remain logic low and pin #J1/8 (Fault 2) outputs should become logic high	Pin #J1/7, pin #J1/8 behavior is as expected
		Apply pin #J1/1 = 8.6 V, set pin #J1/10 logic high/low	Pin #J2/1 should not change logic state from low, pin #J1/7 (Fault 1) should become logic high and pin #J1/8 (Fault 2) outputs should remain logic high	
		Apply pin #J1/1 = 13.6 V, apply to the pin #J1/4 short pulse, check status of the pins #J1/7 and pin #J1/8	Pin #J1/7 (Fault 1) and pin #J1/8 (Fault 2) outputs should become logic low	
7	Pin #J1/12, pin #J4/2 continuity	Set pin J4/2 logic high	Pin #J1/12 should become logic high	Pin #J1/12 behavior is as expected
		Set pin J4/2 logic low	Pin #J1/12 should become logic low	

Table 1: IXIDM1401 Test Description (continued)

Test #	Description	Action	Expected Result	Pass if
8	Pin J2/3 continuity, channel A over-current protection	Apply pin #J1/1 = 13.6 V, set pin #J1/10 logic high,	Check status of the pin J2/1 - it should be high. Check status of the pin #J1/7 and pin #J1/8 - it should be logic low	Pin #J2/1, pin #J1/7, pin #J1/8 behavior is as expected
		Set pin #J2/3= 300 mV above local ground	Check status of the pin J2/1 - it should become logic low. Check status of the pin #J1/8 - it should become logic high. Status of the pin #J1/7 should remain logic low	
		Apply pulse to the pin #J1/4	Check status of the pin J2/1 - it should remain logic low. Check status of the pin #J1/8 - it should become logic low. Status of the pin #J1/7 should remain logic low.	
9	Pin J3/3 continuity, channel B over-current protection	Apply pin #J1/1 = 15 V, set pin #J1/9 logic high,	Check status of the pin J3/1 - it should be high. Check status of the pin #J1/7 and pin #J1/8 - it should be logic high	Pin #J3/1, pin #J1/7, pin #J1/8 behavior is as expected
		Set pin #J3/3= 300 mV above local ground	Check status of the pin J3/1 - it should become logic low. Check status of the pin #J1/8 - it should become logic high. Status of the pin #J1/7 should remain logic low	
		Apply pulse to the pin #J1/4	Check status of the pin J3/1 - it should remain logic low. Check status of the pin #J1/8 - it should become logic low. Status of the pin #J1/7 should remain logic low	

Table 1: IXIDM1401 Test Description (continued)

Test #	Description	Action	Expected Result	Pass if
10	Pin #J2/5 continuity test	Apply pin #J1/1 = 15 V, measure voltage at pin #J2/5	Voltage should be in the range -10 V - - 5 V	Voltage is as expected
11	Pin #J3/5 continuity test	Apply pin #J1/1 = 15 V, measure voltage at pin #J3/5	Voltage should be in the range - -10 V - - 5 V	Voltage is as expected
12	Pin #J2/4 continuity test, channel A ACL functionality test	Apply pin #J1/1 = 15, apply current limited +10 V to pin #J2/1	Check voltage at pin #J2/1, it should be < 0.2 V	Pin #J2/4 behavior is as expected
		Apply > +3.1 V in respect to local Vee voltage to the pin #J2/4	Check voltage at pin #J2/1, it should be +10 V	
13	Pin #J3/4 continuity test, channel B ACL functionality test	Apply pin #J1/1 = 15 V, apply current limited +10 V to pin #J3/1	Check voltage at pin #J3/1, it should be < 0.2 V	Pin #J3/4 behavior is as expected
		Apply > +3 V in respect to local Vee voltage to the pin #J3/4	Check voltage at pin #J3/1, it should be +10 V	

Table 2: Intermediate Results for failed multistep tests

Test #	LED Display Information	Cause of the Test Interruption	Possible Source of the Problem	Recommended Correction
1	RGGG GGGG GGG G*	DUT input current is less than 10 mA	DUT is not installed properly on the test board	Install DUT properly
			DUT Isolation power transformer is not installed or malfunctions	Check power transformer assembly
	GRGG GGGG GGG G	DUT input current is more than 25 mA	One of the DUT rectifying diodes installed in wrong polarity	Check polarity of the rectifying diodes
			Short circuit at primary or secondary side	Check assembly for solder bridges
2	RGGG GGGG GGG G	DUT LDO voltage is less than 3.0 V	Short circuit in 3.3 V net	Check assembly for solder bridges
	GRGG GGGG GGG G	DUT LDO voltage is more than 3.6 V	Short circuit between Vaux and 3.3 V nets	Check assembly for solder bridges
4	RGGG GGGG GGG G	pin #j2/1 < 18 V or pin #j2/1 > 25 V	DUT power transformer malfunction, rectifying diode malfunction, bad soldering	Check power transformer's output voltage and assembly for cold soldering
	GRGG GGGG GGG G	pin J2/1 < -10 V or pin J2/1 > -5 V		
5	RGGG GGGG GGG G	pin #j3/1 < 18 V or pin #j2/1 > 25 V	DUT power transformer malfunction, rectifying diode malfunction, bad soldering	Check power transformer's output voltage and assembly for cold soldering
	GRGG GGGG GGG G	pin J3/1 < -10 V or pin J2/1 > -5 V		

NOTE:

G – Green LED is on

R – Red LED is on

Table 2: Intermediate Results for failed multistep tests (continued)

Test #	LED Display Information	Cause of the Test Interruption	Possible Source of the Problem	Recommended Correction
6	RGGG GGGG GGG G	Fault 1 is active at OVLO	IX6610 Logic malfunction	DUT requires manual test
	GRGG GGGG GGG G	Fault 2 is not activated at OVLO	Cold soldering in Fault 2 network	Fault 2 net for cold soldering
	GGRG GGGG GGG G	Fault 1 activated after fault reset at OVLO	IX6610 Logic malfunction	DUT requires manual test
	GGGR GGGG GGG G	Fault 2 deactivated after fault rest at OVLO	IX6610 Logic malfunction	DUT requires manual test
	GGGG RGGG GGG G	Fault 1 is not active at UVLO	Cold soldering in Fault 1 network	Fault 1 net for cold soldering
	GGGG GRGG GGG G	Fault 2 becomes deactivated without fault reset	IX6610 Logic malfunction	DUT requires manual test
	GGGG GGRG GGG G	Fault 1 becomes deactivated after fault reset at UVLO	IX6610 Logic malfunction	DUT requires manual test
	GGGG GGGR GGG G	Fault 2 is not deactivated after fault reset at UVLO	IX6610 Logic malfunction	DUT requires manual test
	GGGG GGGG RGGG G	Fault Reset does not reset Fault 1 signal at normal mode	Under-voltage protection on primary side is triggered	DUT requires manual test
	GGGG GGGG GRGG G	Fault Reset activates Fault 2 signal at normal mode	IX6610 Logic malfunction	DUT requires manual test
7	RGGG GGGG GGG G	J4/2 pin is not connected	J4 is not installed or have bed soldering	Check DUT for cold soldering in J4 area
	GRGG GGGG GGG G	J4/1 pin is not connected		

Table 2: Intermediate Results for failed multistep tests (continued)

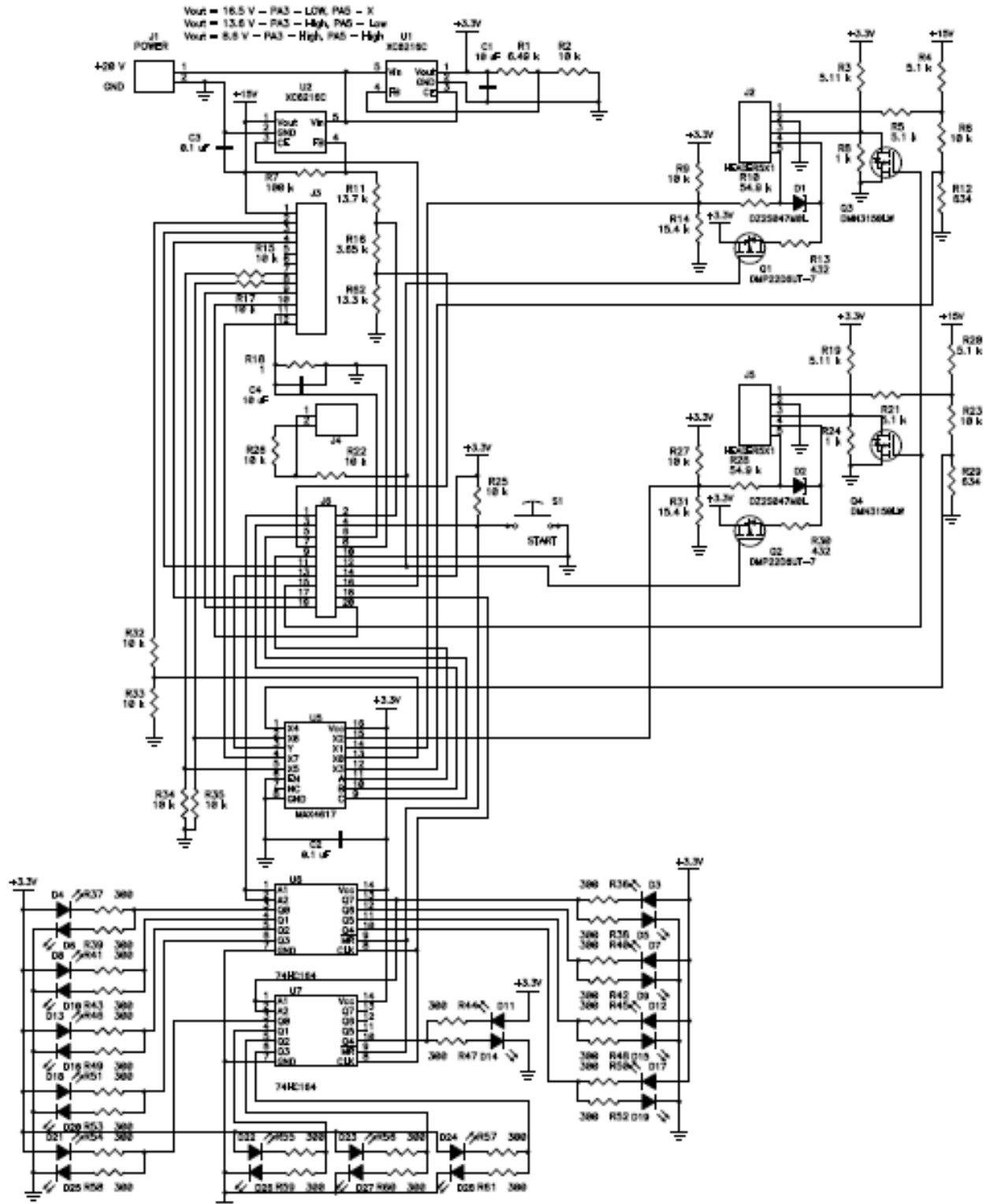
Test #	LED Display Information	Cause of the Test Interruption	Possible Source of the Problem	Recommended Correction
8	RGGG GGGG GGG G	If DUT pass previous tests, these error codes should not appear	Gate A is not activated	Check DUT connectivity to the Test Board
	GRGG GGGG GGG G		Fault 1 becomes active	
	GGRG GGGG GGG G		Fault 2 becomes active	
	GGGR GGGG GGG G	OC trigger does not deactivate gate A	Bad soldering in channel A OC trigger net	Check OC net for cold soldering
	GGGG RGGG GGG G	Fault 1 becomes active	Fault 1 secondary side network malfunction	Check Signal transformer and Fault 1 net for cold soldering/solder bridge
	GGGG GRGG GGG G	Fault 2 is not activated	Fault 2 secondary side network malfunction , pulse generator at IX6611 does not work	Check Signal transformer and Fault 2 net for cold soldering/solder bridge. Replace fault IX6611
	GGGG GGRG GGG G	OC trigger unlocks before next PWM pulse is applied	Fault IX6611	Replace fault IX6611
	GGGG GGGR GGG G	False Fault 1 triggering	No defined source of the problem	DUT requires manual test
	GGGG GGGG RGGG G	Fault Reset does not reset Fault 2 signal		

Table 2: Intermediate Results for failed multistep tests (continued)

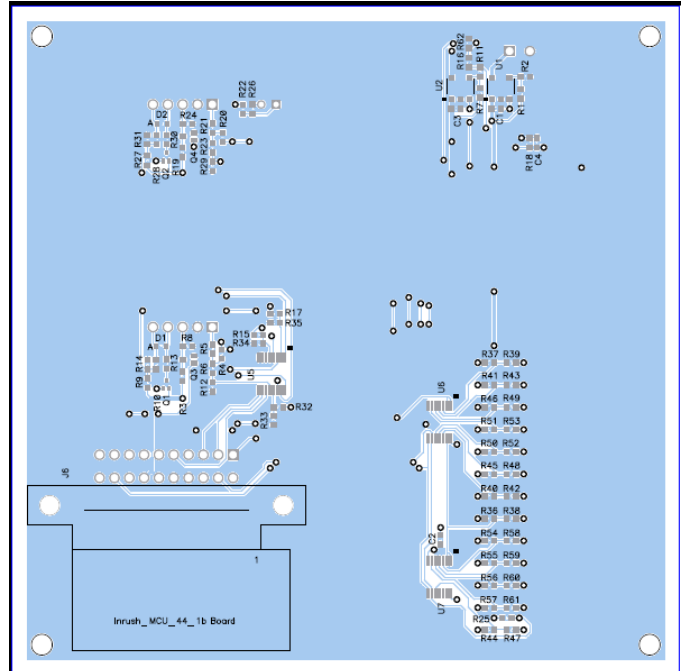
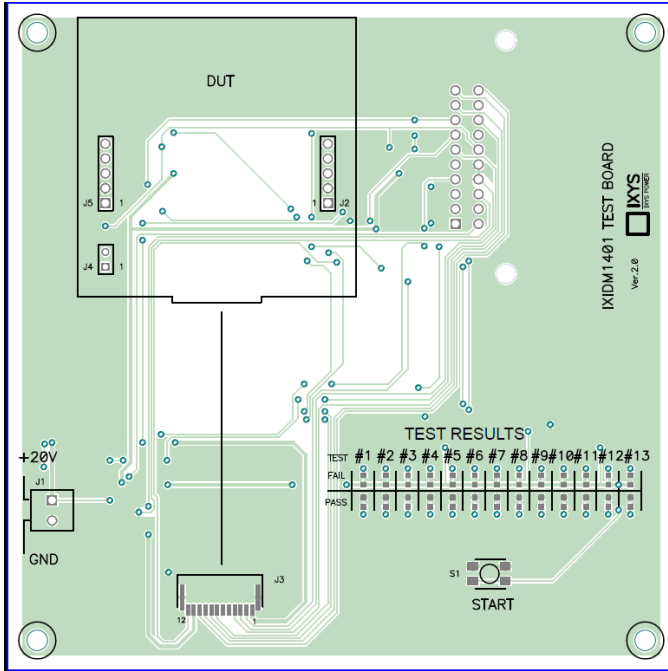
Test #	LED Display Information	Cause of the Test Interruption	Possible Source of the Problem	Recommended Correction
9	RGGG GGGG GGG G	If DUT pass previous tests, these error codes should not appear	Gate B is not activated Fault 1 becomes active Fault 2 becomes active	Check DUT connectivity to the Test Board
	GRGG GGGG GGG G			
	GGRG GGGG GGG G			
	GGGR GGGG GGG G	OC trigger does not deactivate gate A	Bad soldering in channel A OC trigger net	Check OC net for cold soldering
	GGGG RGGG GGG G	Fault 1 becomes active	Fault 1 secondary side network malfunction	Check Signal transformer and Fault 1 net for cold soldering/solder bridge
	GGGG GRGG GGG G	Fault 2 is not activated	Fault 2 secondary side network malfunction , pulse generator at IX6611 does not work	Check Signal transformer and Fault 2 net for cold soldering/solder bridge. Replace fault IX6611
	GGGG GGRG GGG G	OC trigger unlocks before next PWM pulse is applied	Fault IX6611	Replace fault IX6611
	GGGG GGGR GGG G	False Fault 1 triggering	No defined source of the problem	DUT requires manual test
	GGGG GGGG RGGG G	Fault Reset does not reset Fault 2 signal		
10	RGGG GGGG GGG G	Channel A Vee voltage is out of range	Vee network malfunction	Check Vee network for cold soldering
11	RGGG GGGG GGG G	Channel B Vee voltage is out of range	Vee network malfunction	Check Vee network for cold soldering
12	RGGG GGGG GGG G	Because DUT pass previous tests, this error code should not appear	Gate A voltage is out of range	Check DUT connectivity to the Test Board
	GRGG GGGG GGG G	ACL Comparator is not triggered	Fault soldering in channel A ACL trigger net	Check ACL net for cold soldering
13	RGGG GGGG GGG G	Because DUT pass previous tests, this error code should not appear	Gate B voltage is out of range	Check DUT connectivity to the Test Board
	GRGG GGGG GGG G	ACL Comparator is not triggered	Fault soldering in channel B ACL trigger net	Check ACL net for cold soldering

APPENDIX 1. DEMO BOARD SCHEMATIC DIAGRAMS

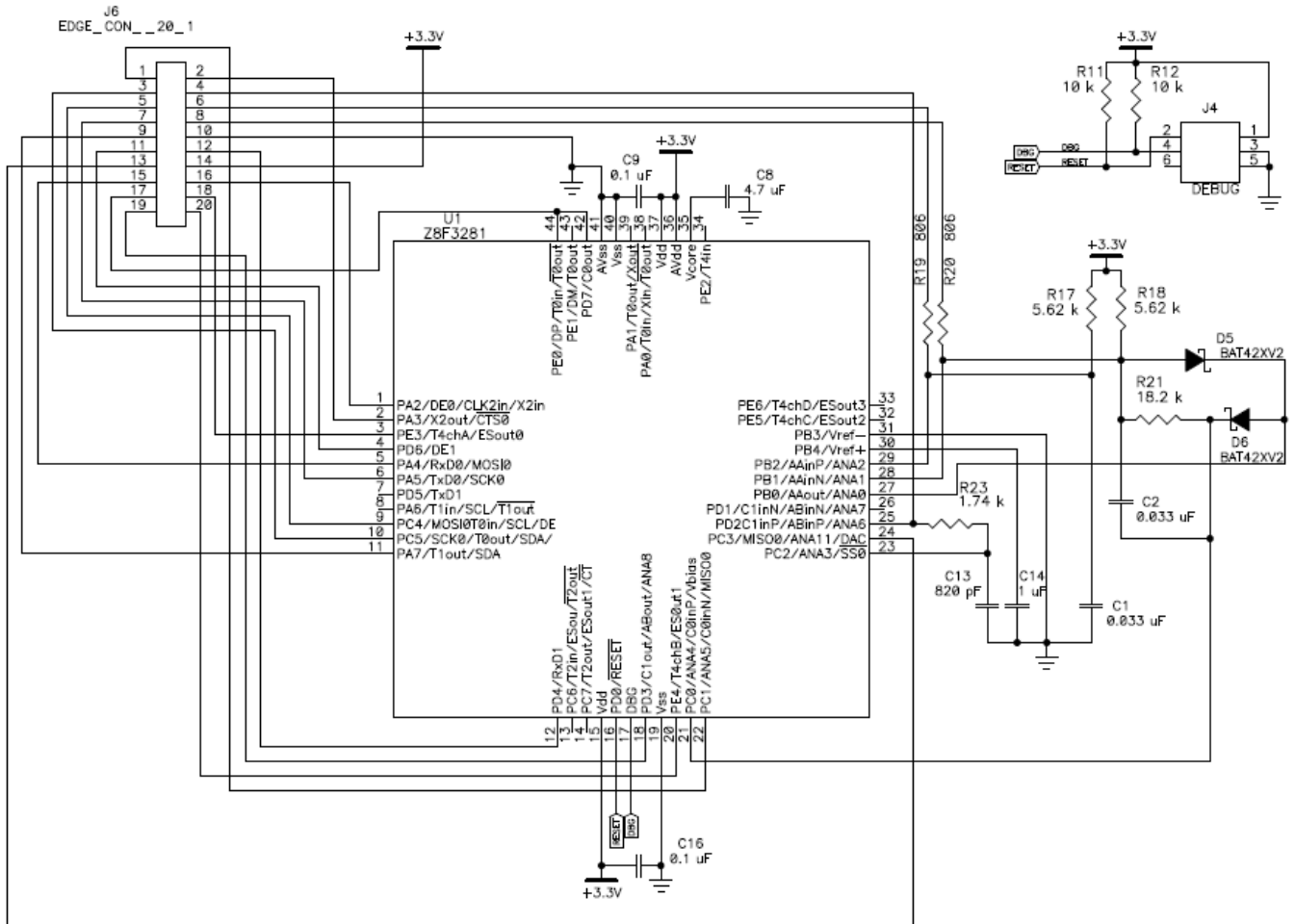
Power Module Schematic Diagram



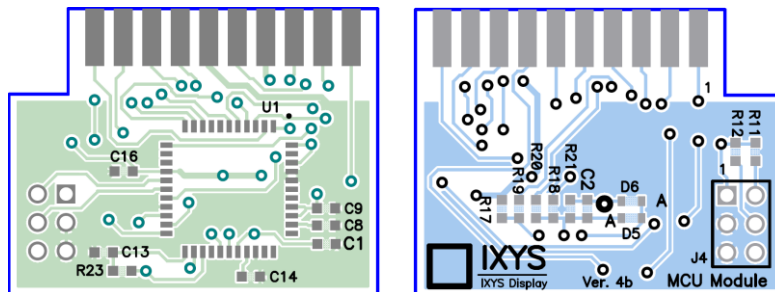
Power Module layout (top and bottom layers)



MCU Module Schematic Diagram



MCU Module Layout (top and bottom layers)





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