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Evaluating the ADPA1105 46 dBm (40 W), 0.9 GHz to 1.6 GHz, GaN Power Amplifier

FEATURES

2-Layer Rogers 4350B evaluation board with heat spreader
End launch SMA jack RF connectors
Through calibration path
Drain or gate pulsing capability

EVALUATION KIT CONTENTS

ADPA1105-EVALZ evaluation board
50 V drain pulser board

EQUIPMENT NEEDED

Pulse generator
Oscilloscope
50 V, 2 A power supply
−4 V power supply
Tektronix TCPA312A current probe
Tektronix TCPA300 current probe amplifier
RF signal generator
Directional coupler
RF power sensor
RF power meter
RF attenuator

DOCUMENTS NEEDED

ADPA1105 data sheet

GENERAL DESCRIPTION

The ADPA1105-EVALZ consists of a 2-layer printed circuit board (PCB) fabricated from a 10 mil thick, Rogers 4350B copper clad mounted to an aluminum heat spreader. The heat spreader assists in providing thermal relief to the device as well as mechanical support to the PCB. Mounting holes on the heat spreader allow the spreader to be attached to a heat sink. Alternatively, the spreader can be clamped to a hot and cold plate. The RFIN and RFOUT ports on the ADPA1105-EVALZ are populated by Subminiature Version A (SMA) female coaxial connectors, and the respective RF traces have a 50 Ω characteristic impedance. The ADPA1105-EVALZ is populated with components suitable for use over the entire operating temperature range of the device. To calibrate board trace losses, a through calibration path is provided between the J6 and J5 connectors. J6 and J5 must be populated with SMA RF connectors to use the through calibration path.

Ground, power, gate control, and the detector output voltage are provided through two 4-pin headers (P1 and P2) and two 24-pin headers (P3 and P4) on the ADPA1105-EVALZ. The pinouts for these four headers are shown in Table 1.

RF traces on the ADPA1105-EVALZ are 50 Ω, grounded, coplanar waveguide. The package ground leads and the exposed paddle connect directly to the ground plane. Multiple vias connect the top and bottom ground planes with particular focus on the area directly beneath the ground pad to provide adequate electrical conduction and thermal conduction to the heat spreader.

The ADPA1105-EVALZ ships with a drain pulsing board (pulser board) that can be plugged into the ADPA1105-EVALZ headers and configured to control the biasing of the ADPA1105 by providing a negative gate voltage and a control signal that connects and disconnects the drain voltage to the ADPA1105-EVALZ. The ADPA1105-EVALZ can also be operated alone in gate pulsed mode where a negative pulse is applied to the ADPA1105 V_{GG1} and V_{GG2} pins.

For full details on the ADPA1105, see the ADPA1105 data sheet, which must be consulted in conjunction with this user guide when using the ADPA1105-EVALZ.

TABLE OF CONTENTS

REVISION HISTORY

10/2020—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

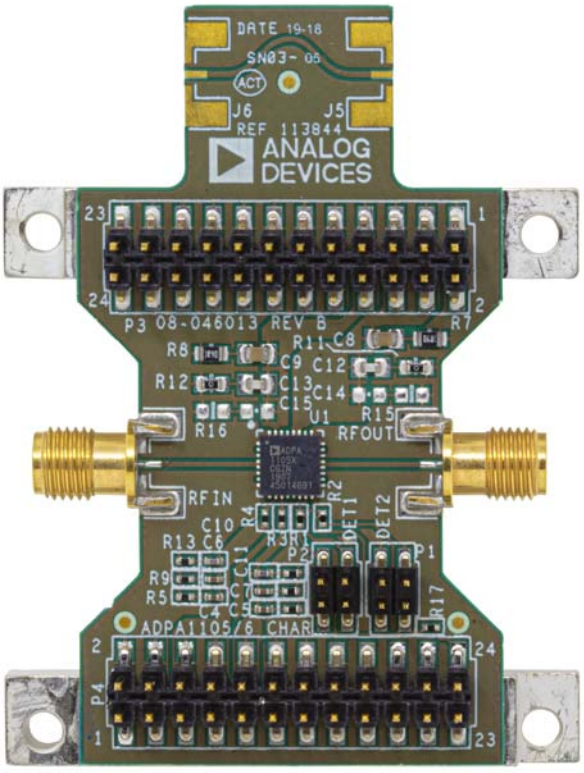

Figure 1. ADPA1105-EVALZ Evaluation Board, Primary Side

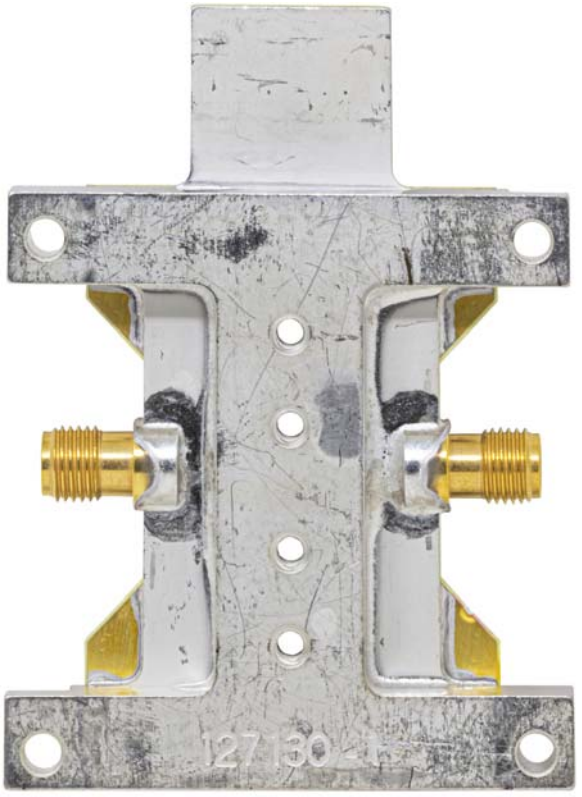

Figure 2. ADPA1105-EVALZ Evaluation Board, Secondary Side

HEADER PINOUT

The schematic for the ADPA1105-EVALZ is shown in Figure 6. The ADPA1105-EVALZ contains four headers, P1, P2, P3, and P4. Table 1 describes the pinout of these headers.

Table 1. P1 to P4 Header Connections on the ADPA1105-EVALZ

Header	Header Pin Number	Header Pin Name
P1	1, 3	GND
	2	DET2_OUT
	4	DET2_BIAS
P2	1, 3	GND
	2	DET1_OUT
	4	DET1_BIAS
P3	1, 3, 5, 7, 9, 10, 11, 12, 13, 14, 15, 17, 19, 21, 22, 23, 24	GND
	2, 16, 18, 20	Not connected
	4, 6	VDD2
	8	VDD1
P4	1, 2, 3, 4, 5, 7, 9, 11, 12, 13, 14, 15, 16, 17, 19, 21, 23	GND
	18, 20, 22	Not connected
	6, 8	VGG1
	10	VGG2
	24	DET2_BIAS

INSERTION LOSS OF THE THROUGH CALIBRATION PATH

To calibrate board trace losses, a through calibration path is provided between the J6 and J5 connectors. J6 and J5 must be populated with SMA RF connectors to use the through calibration path. Figure 3 shows the insertion loss, input return loss, and output return loss of the through calibration path. Table 2 lists the insertion loss of the through path vs. frequency.

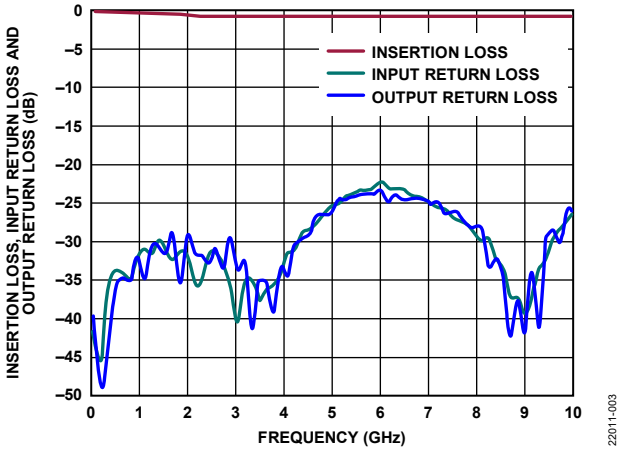

Figure 3. Insertion Loss, Input Return Loss, and Output Return Loss of Through Calibration Path

Table 2. Insertion Loss of Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)
1	−0.24
2	−0.36
3	−0.48
4	−0.45
5	−0.5
6	−0.55
7	−0.61
8	−0.64
9	−0.65
10	−0.65

OPERATING THE ADPA1105-EVALZ WITH A PULSED GATE VOLTAGE

To implement gate pulsed operation, apply a negative voltage pulse to the ADPA1105 V_{GG1} and V_{GG2} inputs while the voltage on the ADPA1105 V_{DD1} and V_{DD2} pins is held constant.

SETUP

All power supply, ground, and control signals are applied to the P3 and P4 headers of the ADPA1105-EVALZ. For this mode of operation, pulse the gate voltage between −4 V (off) and approximately −2.3 V (on) to set the quiescent current (I_{DQ}) to approximately 400 mA. The pulse width and duty cycle must be approximately 100 µs and 10%, respectively.

OPERATION

Take the following steps to power-up:

1. Set VDDx (P3 Pin 4, Pin 6, and Pin 8) to 0 V.
2. Set VGGx (P4 Pin 6, Pin 8, and Pin 10) to off (V_{GG1} = V_{GG2} = −4 V).
3. Set VDD to 50 V.
4. Turn on the gate voltage pulse (V_{GG1} and V_{GG2} pulsing between −4 V and approximately −2.3 V).
5. Fine tune the pulse high voltage to achieve the desired I_{DQ} (nominally 400 mA) while maintaining the pulse off voltage level at −4 V.
6. Apply the RF input signal.

Take the following steps to power-down:

1. Turn off the RF signal.
2. Turn off the pulse to V_{GG1} and V_{GG2} (V_{GG1} = V_{GG2} = −4 V).
3. Set VDD to 0 V.
4. Increase the pulse to V_{GG1} and V_{GG2} to 0 V.

OPERATING THE ADPA1105-EVALZ WITH THE DRAIN BIAS PULSER BOARD

The ADPA1105-EVALZ ships with a drain bias pulser board. A block diagram of the pulser board is shown in Figure 4. The pulser board has two primary components. The BSC340N08NS3 is an 80 V/23 A, metal-oxide semiconductor field effect transistor (MOSFET) that switches the drain voltage to the ADPA1105 on and off, and the LTC7000 is a high-side, negative channel metal-oxide semiconductor (NMOS), static switch driver that controls the MOSFET.

The pulser board plugs into the P3 and P4 headers of ADPA1105-EVALZ and can be configured to provide a pulsed drain voltage and a negative gate control voltage to control the biasing of the ADPA1105.

Table 3. Pulser Board J1, J2, and J3 Header Connections to ADPA1105

Header	Header Pin Number	Header Pin Name
J1	1, 2, 3, 4, 5, 6	VDD
	7, 8, 25	No connect
	9, 10, 11, 12, 13, 14	VGG1, VGG2
	15, 16, 17, 18, 21, 22, 23, 24	GND
	19, 20	PULSE
	26	V_{DET_BIAS}, V_{REF_BIAS}
J2	1, 3, 5, 7, 9, 10, 11, 12, 13, 14, 15, 17, 19, 21, 22, 23, 24	GND
	2, 16, 18, 20	No connect
	4, 6, 8	PULSED_VDD_DUT
J3	1, 2, 3, 4, 5, 7, 9, 11, 12, 13, 14, 15, 16, 17, 19, 21, 23	GND
	6, 8 ,10	VGG1, VGG2
	24	V_{DET_BIAS}, V_{REF_BIAS}

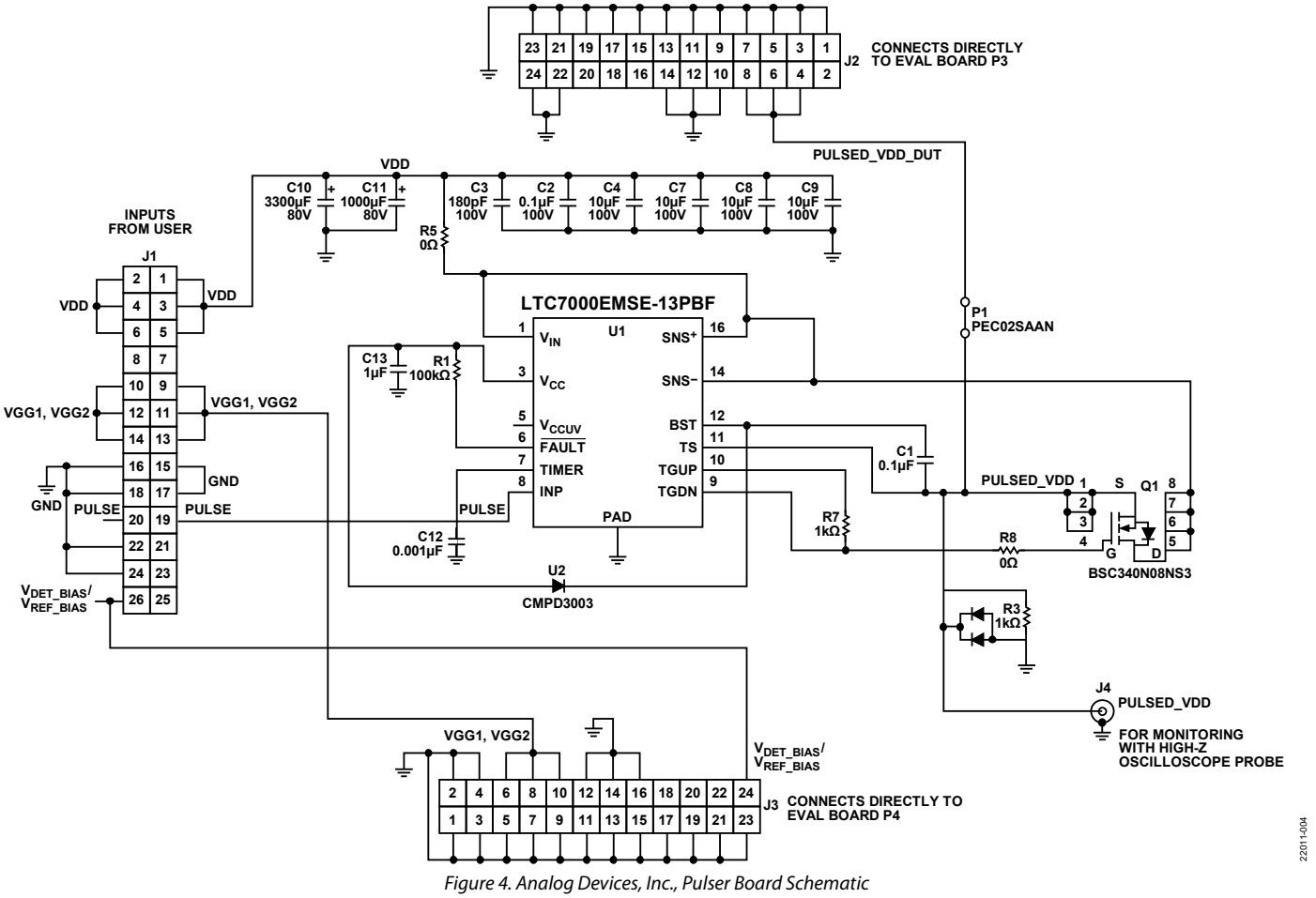

Figure 4. Analog Devices, Inc., Pulser Board Schematic

SETUP

The connections required to use the ADPA1105-EVALZ with the drain bias pulser board are shown in Figure 5. Before applying any bias or signals, plug the pulser board into ADPA1105-EVALZ so that the pulser board J2 header connector connects to the ADPA1105-EVALZ P3 header, and the pulser board J3 header connects to the ADPA1105-EVALZ P4 header. All external supply voltages and control signals are applied to the pulser board J1 header, which are listed in Table 3.

The gate control voltage applied to the J1 connector, Pin 9 to Pin 14, passes directly through the pulser board and drives the ADPA1105 V_{GG1} pin and V_{GG2} pin. Because the VDD and GND lines carry currents up to 2 A, the use of heavy gauge twister pair wires is recommended to minimize voltage drops. To observe the pulsed drain voltage (PULSED_VDD) that drives the ADPA1105 V_{DD1} and V_{DD2} pins, connect an oscilloscope to the J4 coaxial connector on the pulser board.

Connect a digital pulse generator that can generate 0 V to 5 V pulses with a pulse width of 100 µs and a duty cycle of 10% to the pulse pins of J1, Pin 19 and Pin 20.

To observe and measure the drain current and the ADPA1105 RF output power, use a current probe and a pulsed RF power meter. If these methods are not available, make approximations as described in the Making Average to Pulsed Approximations section.

OPERATION

Take the following steps to power-up (unless otherwise stated, all signals are applied to the pulser board):

1. Set the voltage on Pin 19 and Pin 20 of J1 (PULSE) to 0 V.
2. Set the voltage on Pin 9 to Pin 14 of J1 (VGG1, VGG2) to −4 V.
3. Set the voltage on Pin 1, Pin 2, Pin 3, Pin 4, Pin 5 and Pin 6 of J1 (VDDx) to 50 V.
4. Turn on PULSE (0 V/5 V, 100 µs, 10% duty cycle).
5. Increase the voltage on Pin 9 to Pin 14 of J1 (VGG1, VGG2) until the target I_{DQ} is reached (nominally 400 mA).
6. Apply the RF input signal to the ADPA1105-EVALZ RFIN connector.

Take the following steps to power-down:

1. Turn off the RF input signal.
2. Set the voltage on Pin 9 to Pin 14 of J1 (VGG1, VGG2) to −4 V.
3. Turn off PULSE (set to 0 V).
4. Set the voltage on Pin 1 to Pin 6 of J1 (VDD) to 0 V.
5. Set the voltage on Pin 9 to Pin 14 of J1 (VGG1, VGG2) to 0 V.

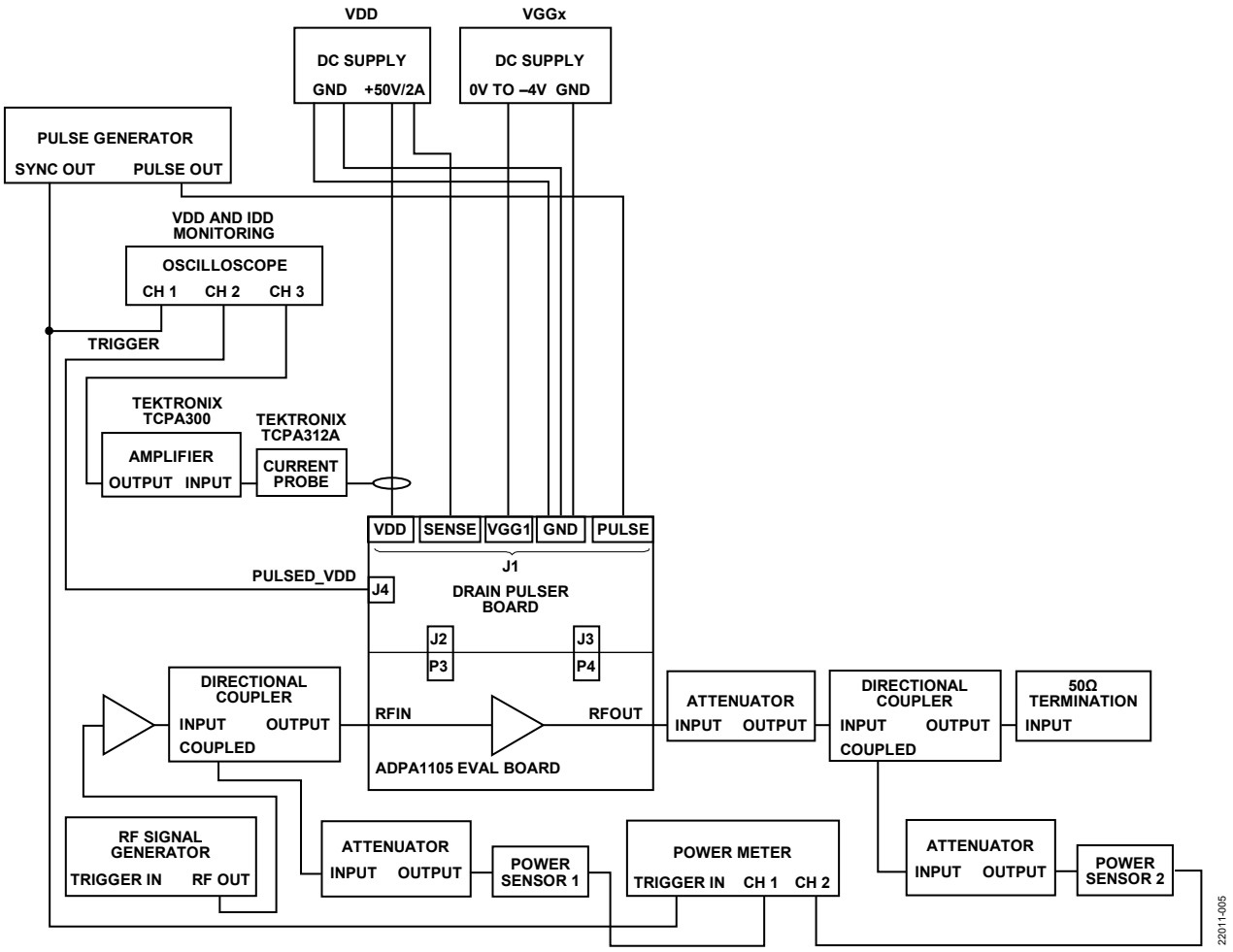

Figure 5. Setup Block Diagram

MAKING AVERAGE TO PULSED APPROXIMATIONS

Instruments that can be triggered are required to measure the RF power, drain current, and power added efficiency (PAE) accurately under pulsed operation. When such instrumentation is not available, use averaging and approximations. The most common approximations involve measuring the average values and then adjusting those values to account for the duty cycle. These approximations can result in errors because of limited measurement bandwidths of instruments and/or the inclusion of on and off transients and/or partial periods in the measurement.

To ensure that partial periods do not contribute significant errors to the measurements, perform averaging over a large number of pulse periods. The results of such approximations can vary with the instruments and settings used. Therefore, experimentation can be necessary to achieve credible and repeatable results. When it is not possible to make pulse triggered measurements, the only pulse connection required is the connection from the pulse generator to the J1 connector of the pulser (see Figure 5).

EVALUATION BOARD SCHEMATIC AND ARTWORK

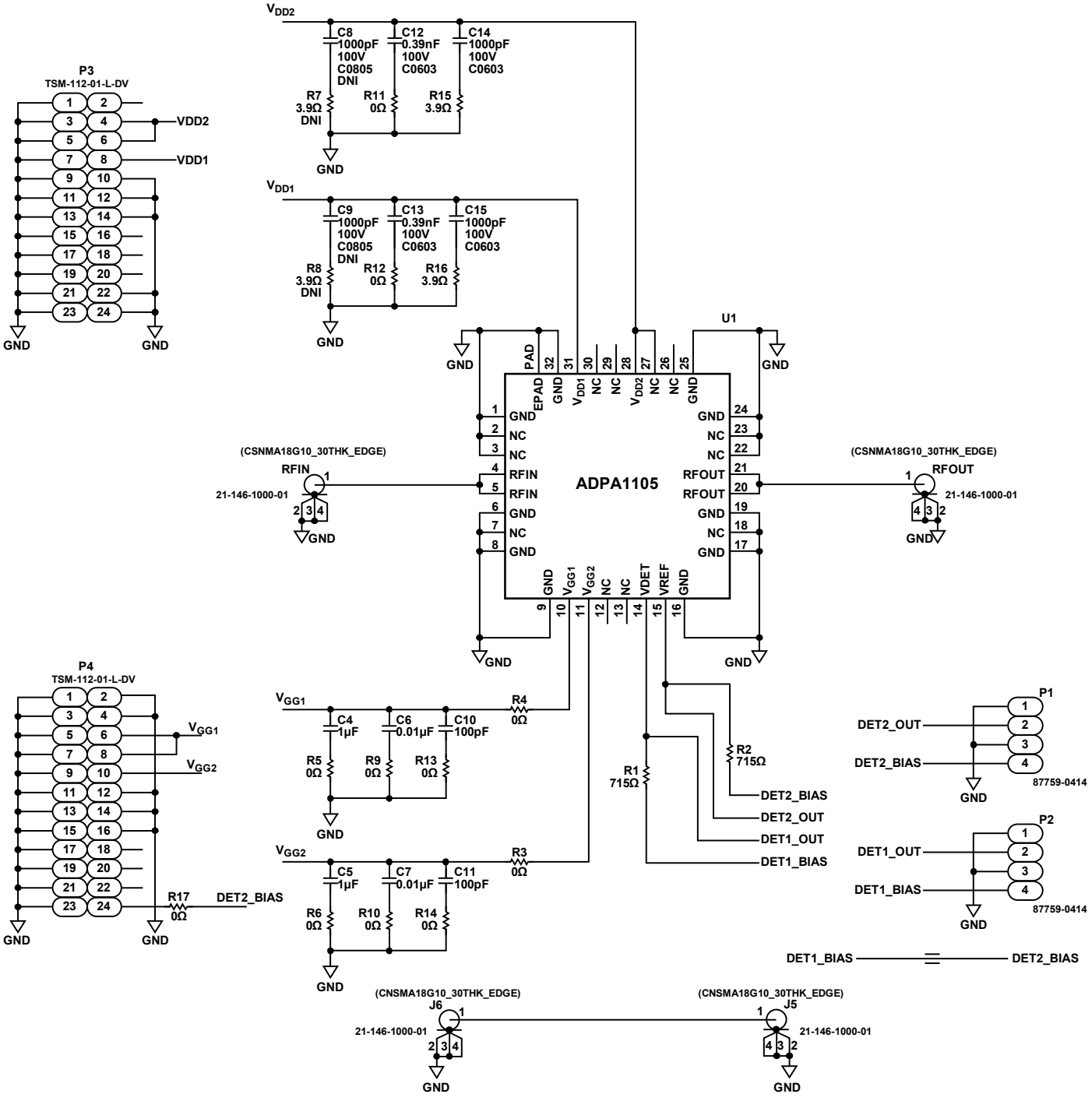

Figure 6. ADPA1105-EVALZ Evaluation Board Schematic

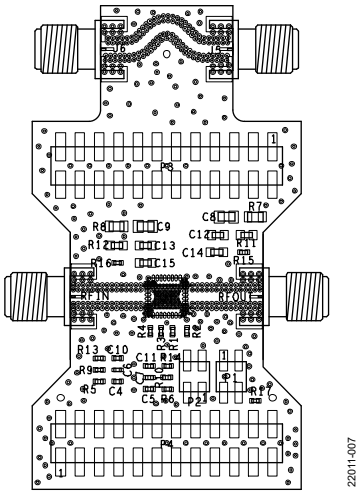

Figure 7. ADPA1105-EVALZ Assembly Drawing (J6 and J5 Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Reference Designator	Description	Manufacturer	Part Number
C4, C5	Capacitors, ceramic, 1 µF	AVX	04026D105KAT2A
C6, C7	Capacitors, ceramic, 0.01 µF	TDK	CGA2B3X7S2A103K050BB
C8, C9	Capacitors, ceramic, not installed	AVX Corporation	08051C102KAT2A
C10, C11	Multilayer capacitors, ceramic, 100 pF	TDK KEMET	C1005NP01H101J050BA
C12, C13	Capacitors, ceramic, 0.39 nF		C0603C391J1GAC7867
C14, C15	Capacitors, ceramic, 1000 pF	TDK	C1608C0G2A102J
P1, P2	Connectors, PCB header, vertical, dual row, 4-pin, 2 mm pitch	Molex	87759-0414
P3, P4	Connectors, PCB header, vertical, dual row, 24-pin, 2.54 mm pitch	SAMTEC INC.	TSM-112-01-L-DV
R1, R2	Resistors, thick film chip, 100 kΩ	Multicomp (SPC)	MC 0.0625W 0402 1% 100K
R3, R4, R17	Resistors, thick film chip, 0 Ω	Multicomp (SPC)	MC00625W040210R
R5, R6, R9, R10, R13, R14	Resistors, surface-mount device (SMD) chip jumper, 0 Ω	Panasonic	ERJ-2GE0R00X
R7, R8	Resistors, thick film chip, not installed	Stachpole Electronics, Inc.	RMCF0805FT3R90
R11, R12	Resistors, film SMD, 0 Ω	Panasonic	ERJ-3GEY0R00V
R15, R16	Resistors, thick film chip, 3.9 Ω	Panasonic	ERJ-2GEJ3R9X
J5, J6	Connectors, SMA jack edge, not installed	SRI Connector Gage Co.	21-146-1000-01
J1 RFIN, J2 RFOUT	Connectors, SMA jack edge	SRI Connector Gage Co.	21-146-1000-01
U1	40 W, 0.9 GHz to 1.6 GHz, GaN power amplifier	Analog Devices	ADPA1105ACGZN
Not Applicable	Aluminum heatsink 2.51 in × 1.91 in	Not applicable	Not applicable