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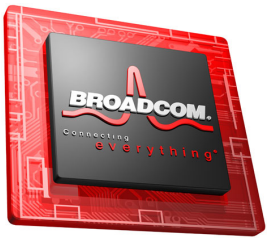
BCM8073 PRODUCT Brief



DUAL-CHANNEL SERIAL 10GBASE-KR TO XAUI™ TRANSCEIVER

FEATURES

- Two 10G-XAUI™ interfaces in one compact package
- High-performance DFE/FFE receive equalizer with full adaptation on chip
- Multitap transmit preemphasis with automated start-up routine
- Auto-negotiates to 1.25G/10G
- Complete 1G and 10G PCS layers
- Low-power equalization mode for shorter reach stackable systems
- Programmable amplitude control on 10G serial transmitter
- Selectable FEC encoder/decoder for added performance
- Input sensitivity 20 mV peak-to-peak differential
- Multiple interface support
  - PMD interface: Serial 10.3125-Gbps CML
  - 4-lane XAUI (3.125 Gbps)
- Low-power 65-nm CMOS design with 1.2W/10G KR port
- Core supply—1.0V, I/O—3.3V
- Loss-of-signal detection
- On-chip diagnostics include 10G eye monitor, SNR, and BER monitors
- Integrated packet generator and checker
- 19 mm x 19 mm, 1-mm pitch, 324-pin BGA, RoHS compliant package

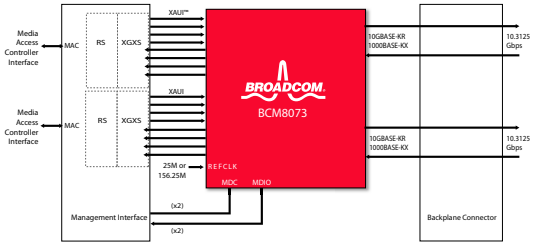
SUMMARY OF BENEFITS

- Targeted to meet the IEEE 802.3ap standard
- High-performance equalization supports new and legacy backplane channels.
- XAUI and 10G differential pairs can be reversed to facilitate layout.
- Enhanced diagnostics provide users with signal quality monitors.
- Single 156.25-MHz or 25-MHz REFCLK reduces overall linecard BOM cost.
- Low-latency design for high-performance computing.
- Broadcom Signal Integrity Tool - LINKEYE(TM) assists customers with high-speed system designs.

APPLICATIONS

- Backplane links
- Copper-cable stackable links
- Onboard and board-to--board links

BCM8073 Functional Block Diagram



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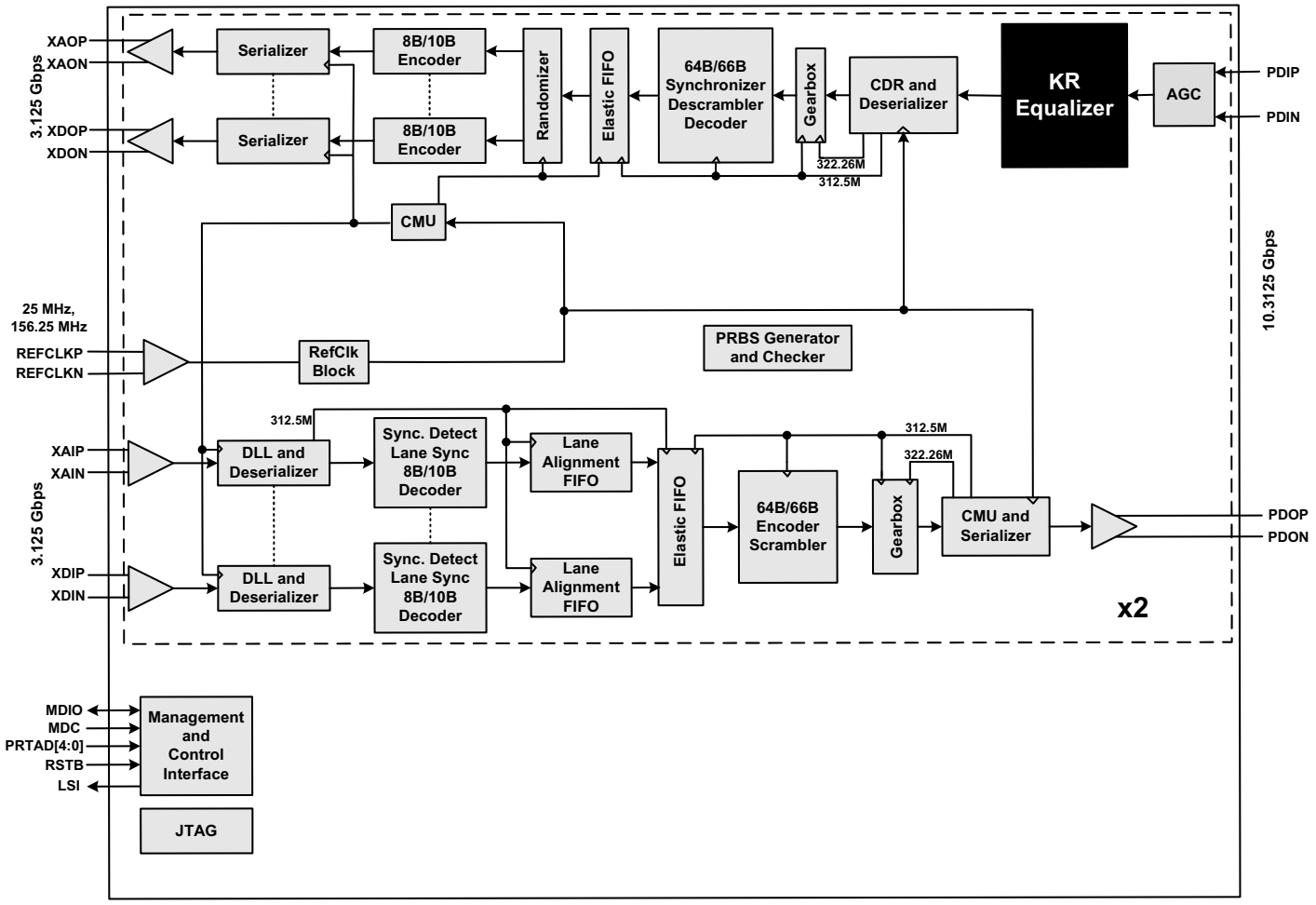
OVERVIEW



BCM8073 Block Diagram

The BCM8073 is a dual-channel 10-GbE serial transceiver targeting the new IEEE 10GBASE-KR standard for running 10G serial data over backplane systems. The device incorporates sophisticated receive equalizers, which extend the life of legacy systems currently running at 1G or XAUI data rates by providing a 4x or 10x bandwidth improvement on each channel.

On-chip clock synthesis is performed by the high-frequency, low-jitter phase-locked loops (PLL) for the PMD and XAUI output retimers. Individual PMD and XAUI clock recovery is performed on the device by synchronizing directly with the respective incoming data streams. An external 25-MHz or 156.25-MHz oscillator is required for the reference clock input.

The BCM8073 dual Ethernet 10GBASE-KR PHY is a fully integrated dual SerDes (10.3125 Gbps) interface device performing the extension functions for a 10-GbE reconciliation sublayer (RS) interface. The XGXS, PCS, and PMA include 8B/10B coding, 64B/66B coding, SerDes, a clock multiplication unit (CMU), and clock and data recovery (CDR).

Polarity of the XAUI and 10G differential pairs can be reversed to facilitate layout. The ordering of the XAUI lanes can also be changed.

The BCM8073 is available in a 19 mm × 19 mm, 1-mm pitch, 324-pin BGA, RoHS-compliant package.

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