8-Output Very Low Phase Jitter HCSL Fanout Buffer

8INT31H800A

DATA SHEET

General Description

The 8INT31H800A is an 8-output very high performance HCSL fanout buffer for High Performance Interconnect applications. It can also be used at speeds up to 350MHz. There are four OE pins on the device, each controlling two outputs.

Recommended Application

DB800H

Output Features

- Eight HCSL differential pairs

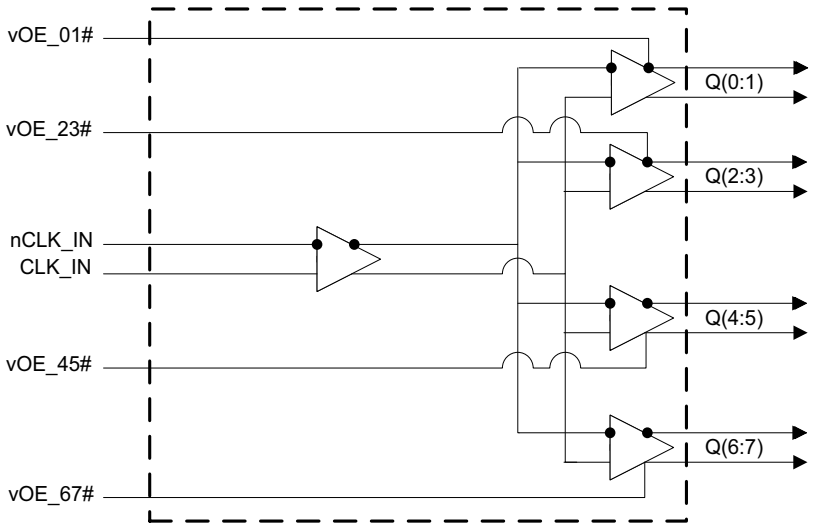
Key Specifications

- Qx output-to-output skew within a pair: 22ps (typical)
- Qx output-to-output skew across all outputs: 32ps (typical)
- RMS additive phase jitter: 65fs (typical)

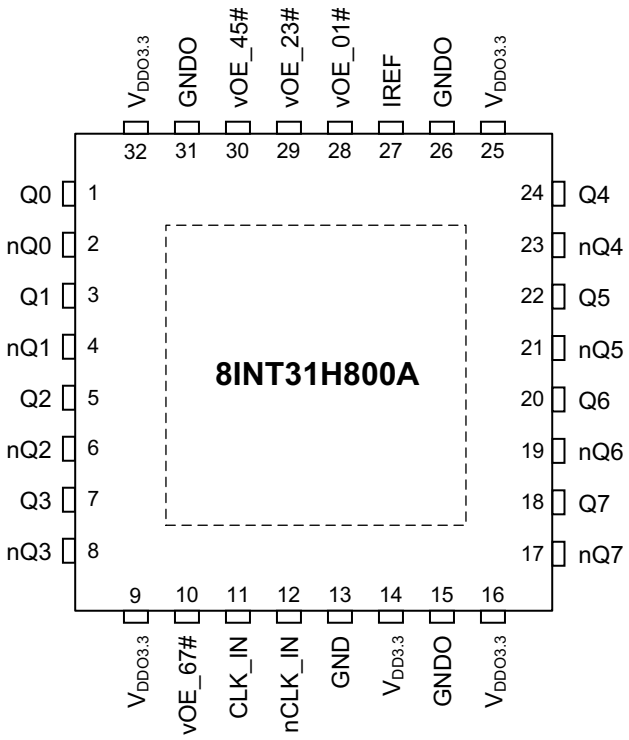
Features/Benefits

- Extremely low additive phase jitter; supports DB800H requirements
- 3.3V operation; standard industry power supply
- Four OE pins each controlling two outputs; easy control of clocks to CPU sockets
- Universal differential input; can be driven by HCSL or LVPECL clock sources
- 1MHz to 350MHz operating frequency; covers all popular Ethernet frequencies
- Space saving 32-pin 5x5mm VFQFN; minimal board space

Block Diagram



Pin Assignment



32-pin, 5mm x 5mm VFQFN Package

v prefix indicates internal 50kΩ pull-down resistor

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Pin#	Name	Type		Pin Description
1	Q0	Output		Non-inverting output of Differential Pair 0.
2	nQ0	Output		Inverting output of Differential Pair 0.
3	Q1	Output		Non-inverting output of Differential Pair 1.
4	nQ1	Output		Inverting output of Differential Pair 1.
5	Q2	Output		Non-inverting output of Differential Pair 2.
6	nQ2	Output		Inverting output of Differential Pair 2.
7	Q3	Output		Non-inverting output of Differential Pair 3.
8	nQ3	Output		Inverting output of Differential Pair 3.
9	$V_{DDO3.3}$	Power		Power supply for outputs, nominal 3.3V.
10	vOE_67#	Input	Pulldown	Active Low input for enabling outputs 6 and 7. 0 = enable outputs, 1 = disable outputs
11	CLK_IN	Input		True Input for differential reference clock.
12	nCLK_IN	Input		Complementary Input for differential reference clock.
13	GND	GND		Ground pin.
14	$V_{DD3.3}$	Power		Power supply, nominal 3.3V.
15	GNDO	GND		Ground pin for outputs.
16	$V_{DDO3.3}$	Power		Power supply for outputs, nominal 3.3V.
17	nQ7	Output		Inverting output of Differential Pair 7.
18	Q7	Output		Non-inverting output of Differential Pair 7.
19	nQ6	Output		Inverting output of Differential Pair 6.
20	Q6	Output		Non-inverting output of Differential Pair 6.
21	nQ5	Output		Inverting output of Differential Pair 5.
22	Q5	Output		Non-inverting output of Differential Pair 5.
23	nQ4	Output		Inverting output of Differential Pair 4.
24	Q4	Output		Non-inverting output of Differential Pair 4.
25	$V_{DDO3.3}$	Power		Power supply for outputs, nominal 3.3V.
26	GNDO	GND		Ground pin for outputs.
27	IREF	Output		This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475Ω is the standard value for 100Ω differential impedance. Other impedances require different values. See data sheet.
28	vOE_01#	Input	Pulldown	Active Low input for enabling outputs 0 and 1. 0 = enable outputs, 1 = disable outputs
29	vOE_23#	Input	Pulldown	Active Low input for enabling outputs 2 and 3 0 = enable outputs, 1 = disable outputs
30	vOE_45#	Input	Pulldown	Active Low input for enabling outputs 4 and 5. 0 = enable outputs, 1 = disable outputs
31	GNDO	GND		Ground pin for outputs.
32	$V_{DDO3.3}$	Power		Power supply for outputs, nominal 3.3V.

Table 2A. Output Enable (OE) Functionality Table[1]

CLK_IN	vOE_x# Pin	Qx	nQx
Running	1	Low[2]	Low[2]
Running	0	Running	Running
Not Running	X	X	X

NOTE 1: vOE_X# denotes: vOE_01#, vOE_23#, vOE_45#, vOE67#.

NOTE 2: The outputs are tristated and the termination networks pulls them low.

Table 2B. Power Connections[1]

Pin Number		Description
V_{DDx}	GND	
14	13	Core Power Supply
9, 16, 25, 32	15, 26, 31	Output Power Supply

NOTE 1: V_{DDx} denotes either $V_{DD3.3}$ or $V_{DDO3.3}$.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 8INT31H800A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DDx}	3.3V Supply Voltage[1]				3.6	V
V_{IL}	Input Low Voltage		GND - 0.5			V
V_{IH}	Input High Voltage				3.6	V
Outputs (V_O)					3.6	V
T_S	Storage Temperature		-65		150	°C
T_J	Junction Temperature				125	°C
ESD (HBM)	ESD protection[2]	Human Body Model	2000			V
ESD (CDM)		Charged Device Model	1000			V

NOTE 1: V_{DDx} denotes either $V_{DD3.3}$ or $V_{DDO3.3}$.

NOTE 2: According to JEDEC/JS-001-2012/JESD22-C101E.

Electrical Characteristics

Table 3A. Input/Supply/Common Parameters,
Supply Voltage V_{DDx}[1] = 3.3 V ±5%, $T_A = T_{IND}$[2]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
T_{IND}	Ambient Operating Temperature	Industrial Range	-40	25	85	°C
V_{IH}	Input High Voltage	vOE_01#, vOE_23# vOE_45#, vOE_67#	2.2		$V_{DD3.3}$ + 0.3	V
V_{IL}	Input Low Voltage	vOE_01#, vOE_23# vOE_45#, vOE_67#	GND - 0.3		0.8	V
I_{IH}	Input High Current	vOE_01#, vOE_23# vOE_45#, vOE_67# $V_{DD3.3} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	vOE_01#, vOE_23# vOE_45#, vOE_67# $V_{DD3.3} = 3.465V$, $V_{IN} = 0V$	-5			µA
F_{max}	Maximum Input Frequency[3]		1		350	MHz
L_{pin}	Pin Inductance				7	nH
C_{IN}	Capacitance	vOE_01#, vOE_23# vOE_45#, vOE_67#			5	pF
C_{INDIF_IN}		CLK_IN, nCLK_IN			3	pF
C_{OUT}		Output Pin Capacitance			6	pF
t_{LATOE}	OE# Latency[4]	Input Clock must be running	4		12	clocks

NOTE 1: V_{DDx} denotes either $V_{DD3.3}$ or $V_{DDO3.3}$.

NOTE 2: Guaranteed by design and characterization, not 100% tested in production.

NOTE 3: Signal edge is required to be monotonic when transitioning through this region.

NOTE 4: Time from de-assertion until outputs are stopped or time from assertion until outputs are running.

Table 3B. Clock Input Parameters, Supply Voltage $V_{DD}x$[1] = 3.3 V ±5%, $T_A = T_{IND}$,

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{PP}	Peak-to-Peak Voltage	CLK_IN, nCLK_IN		0.3		1.0	V
V_{CMR}	Common Mode Input Voltage[2, 3]	CLK_IN, nCLK_IN		GND + 0.3		$V_{DD3.3}$ - 1	V
dv/dt	Input Slew Rate[4]		Measured Differentially	0.4		8	V/ns
I_{IN}	Input Leakage Current		$V_{IN} = V_{DD3.3}$, V_{IN} = GND	-5		5	µA
d_{tin}	Input Duty Cycle		Measurement from Differential Waveform	40		60	%

NOTE 1: V_{DDx} denotes either $V_{DD3.3}$ or $V_{DDO3.3.}$

NOTE 2: Common mode voltage is defined as the crosspoint.

NOTE 3: Input voltage cannot be less than GND - 300mV or more than $V_{DD3.3.}$

NOTE 4: Slew rate measured through ±75mV window centered around differential zero.

Table 3C. Qx HCSL Differential Outputs, Supply Voltage V_{DDx}[1]= 3.3 V ±5%, $T_A = T_{IND}$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
dv/dt	Slew Rate[2, 3]		0.6		4	V/ns
ΔTrf	Rise/Fall Time Matching[4]	Rise/Fall Time Matching			20	%
V_{HIGH}	Voltage High[5]	Statistical Measurement on Single-ended Signal using Oscilloscope Math Function	650		875	mV
V_{Low}	Voltage Low[5]		-150		150	mV
V_{max}	Max. Voltage[5]	Measurement on Single-ended Signal using Absolute Value			1150	mV
V_{min}	Min. Voltage[5]		-300			
V_{cross_abs}	Crossing Voltage (abs)[6]		240		550	mV
Δ-V_{cross}	Crossing Voltage (var)[5, 7]				140	mV

NOTE 1: V_{DDx} denotes either $V_{DD3.3}$ or $V_{DDO3.3}$.

NOTE 2: Measured from differential waveform.

NOTE 3: Slew rate is measured through the V_{swing} voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.

NOTE 4: Rise/Fall matching derived using the following, $2*(T_{RISE} - T_{FALL}) / (T_{RISE} + T_{FALL})$

NOTE 5: Measured from single-ended waveform.

NOTE 6: V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

NOTE 7: The total variation of all V_{cross} measurements in any system. Note that this is a subset of $V_{\_cross\_min/max}$ ($V_{\_cross\ absolute}$) allowed. The intent is to limit V_{cross} induced modulation by setting $V_{\_cross\_delta}$ to be smaller than $V_{\_cross\ absolute}$.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500ppm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Guaranteed by design and characterization, not 100% tested in production.

Table 3D. Current Consumption, Supply Voltage V_{DDx}[1] = 3.3V ±5%, $T_A = T_{IND}$

Test Conditions	Minimum	Typical	Maximum	Units
All outputs running @ 350MHz		191	225	mA
2 outputs running @ 350MHz other outputs disabled.		84	100	mA
All outputs stopped, input clock running @ 350MHz or stopped.		34	40	mA

NOTE 1: V_{DDx} denotes either $V_{DD3.3}$ or $V_{DDO3.3}$.

Table 3E. Qx Output Duty Cycle, Jitter, and Skew Characteristics, Supply Voltage V_{DDx}[1, 2] = 3.3 V ±5%, $T_A = T_{IND}$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
t_{OCD}	Output Duty Cycle[3]	Measured Differentially	45		55	%
t_{PD}	Skew, Input to Output	V_T = 50%	1		1.6	ns
$t_{SKEWpair}$	Skew, Output to Output	Between Two Output Pairs Controlled by Same OE Pin, V_T = 50%			38	ps
t_{sk3}	Skew, Output to Output	Across all Outputs, V_T = 50%		32	80	ps
$t_{jcyc-cycadd}$	Jitter, Cycle to Cycle Additive[4]	Across all Outputs, V_T = 50% f_{OUT} = 156.25MHz			50	ps

NOTE 1: V_{DDx} denotes either $V_{DD3.3}$ or $V_{DDO3.3}$.
NOTE 2: Guaranteed by design and characterization, not 100% tested in production.
NOTE 3: Input duty cycle = 50%
NOTE 4: Measured from differential waveform.

Table 3F. Additive Phase Jitter, Supply Voltage V_{DDx} = 3.3 V ±5%, $T_A = T_{IND}$[1 2 3]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
t_{jph}	Additive Phase Jitter	f_{OUT} = 156.25MHz, All Outputs Running, Integration Range: 12kHz to 20MHz		65	75	fs (RMS)

NOTE 1: Applies to all output
NOTE 2: Signal Source Wenzel Oscillator.
NOTE 3: For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 – (input jitter)^2]

HCSL Test Loads

Table 3G. Differential Output Termination Table[1]

DIF Zo (Ω)	IREF (Ω)	Rs (Ω)	Rp (Ω)
100	475	33	50
85	412	27	42.2 or 43.2

NOTE 1: It is recommended to use the components for differential output impedance of 85Ω for optimal performance.

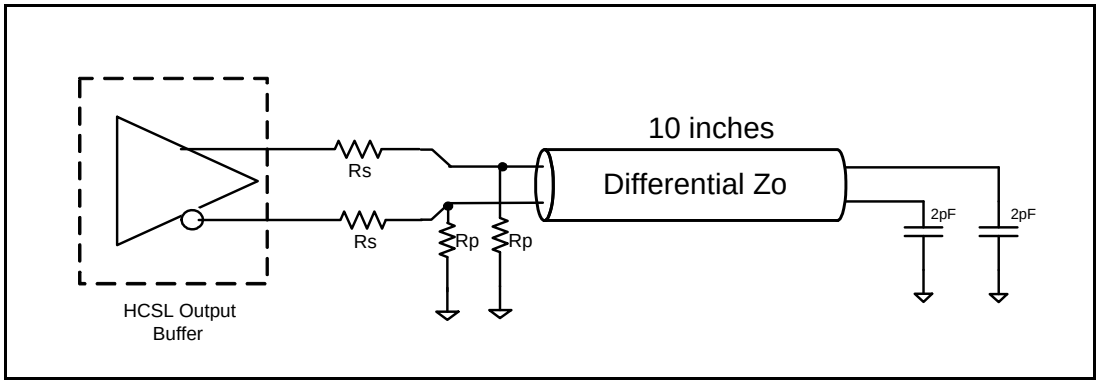
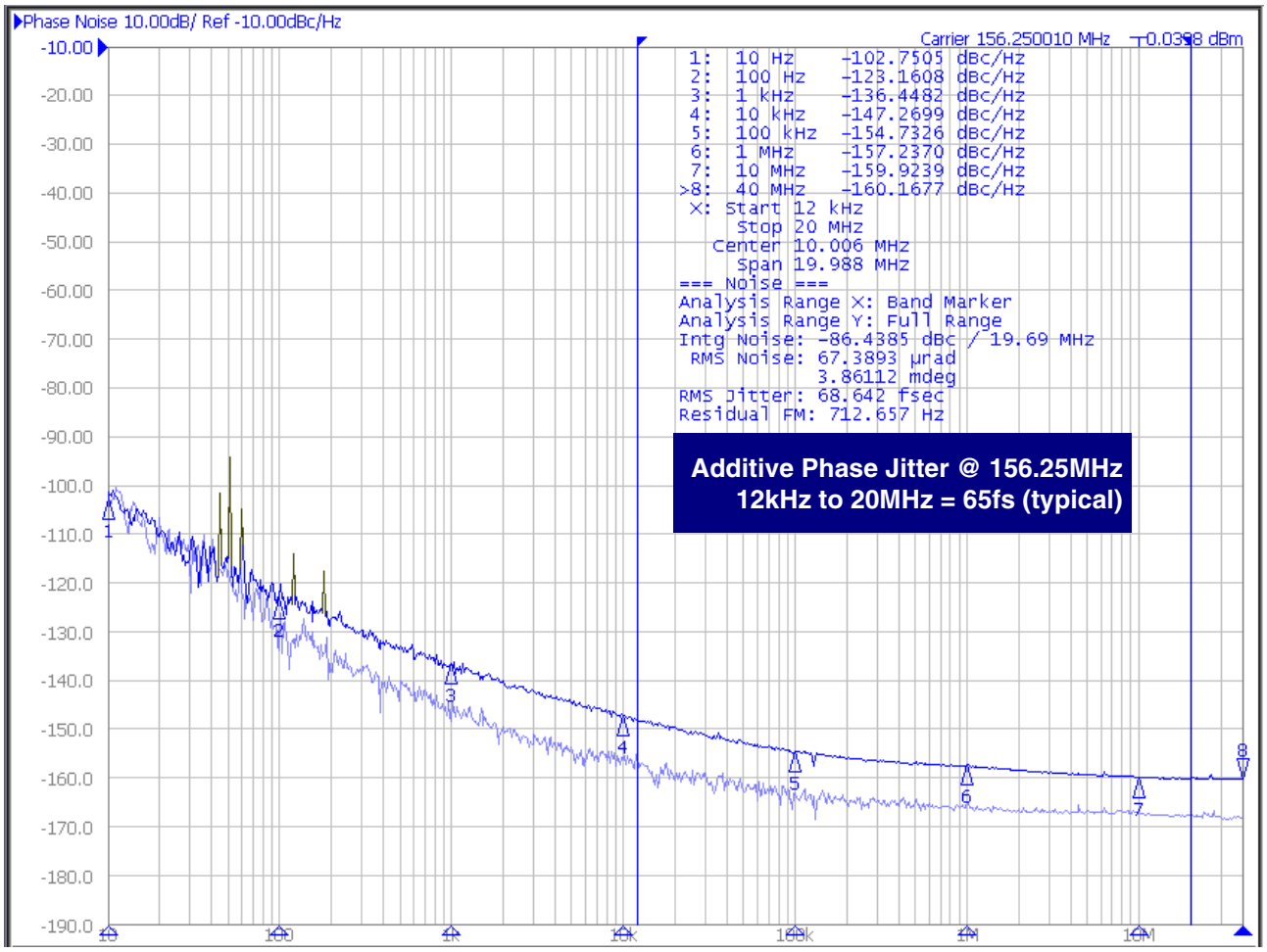


Figure 1. HCSL Test Load

Additive Phase Jitter

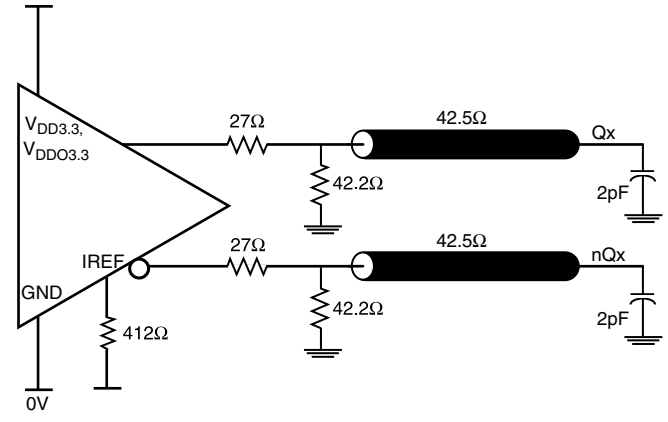
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

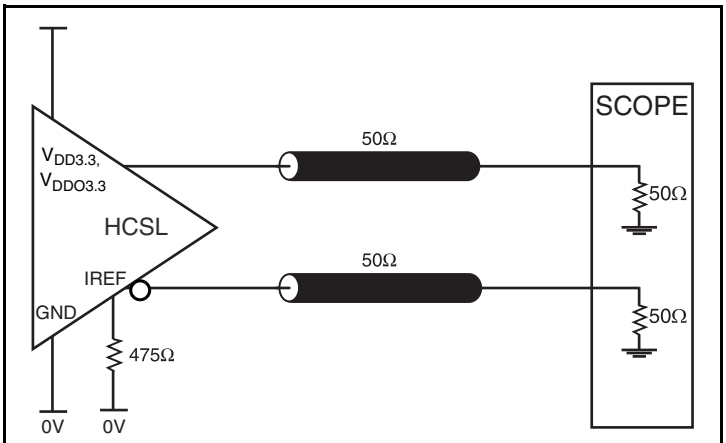
The source generator used is, low noise Wenzel Oscillator at 156.25MHz, and the additive phase jitter for this device was measured using an Agilent E5052 Phase Noise Analyzer.

Parameter Measurement Information



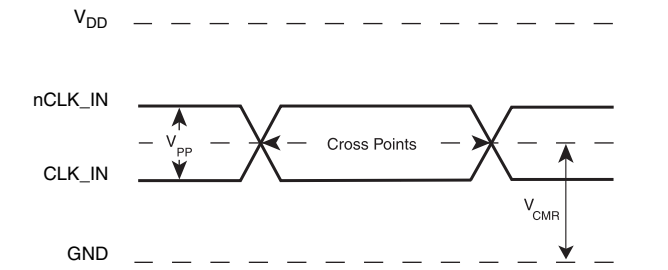
This load condition is used for I_{DD}, V_{MAX}, V_{MIN}, V_{RB}, t_{STABLE}, V_{CROSS}, ΔV_{CROSS} and Rise/Fall Edge Rate measurements.

3.3VCore/3.3V HCSL Output Load AC Test Circuit

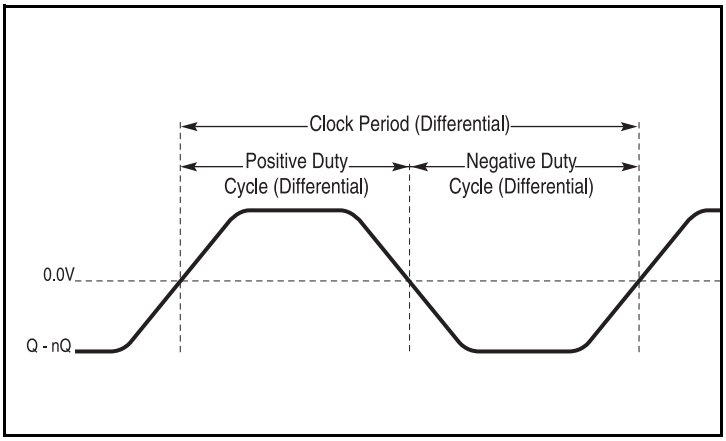


This load condition is used for tjit(cc), tjit and tsk(o), tsk(pp) and t_{PD} measurements.

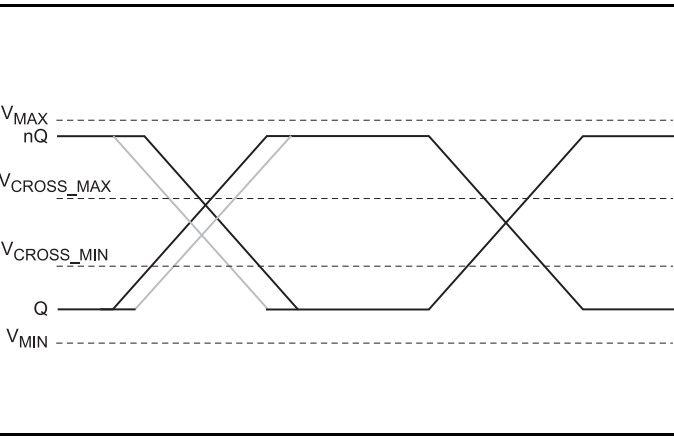
3.3V Core/3.3V HCSL Output Load AC Test Circuit



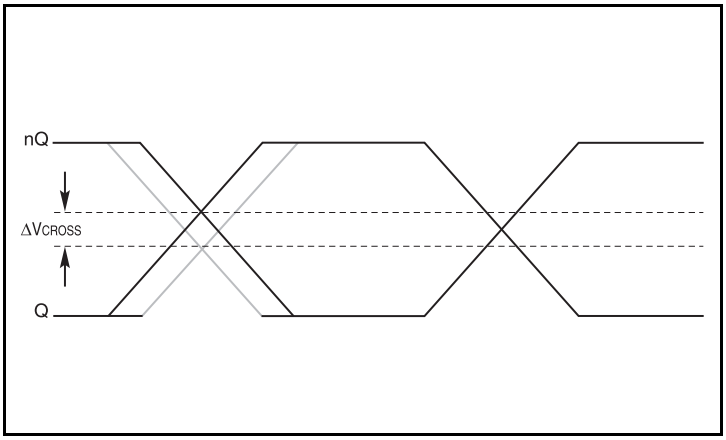
Differential Input Level



Differential Measurement Points for Duty Cycle/Period

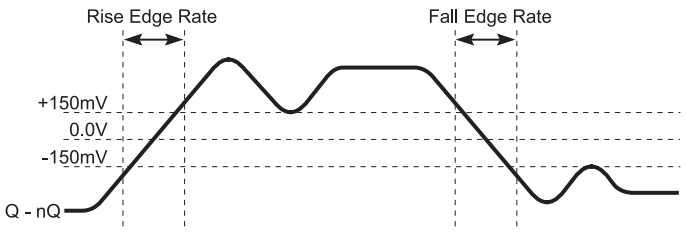


Single-ended Measurement Points for Absolute Cross Point/Swing

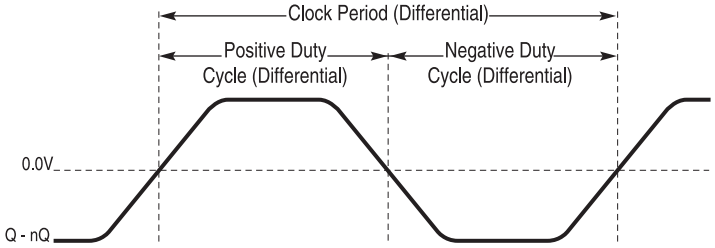


Single-ended Measurement Points for Delta Cross Point

Parameter Measurement Continued...



Differential Measurement Points for Rise/Fall Time Edge Rate



Differential Measurement Points for Ringback

Applications Information

Differential Clock Input Interface

The 8INT31H800A differential clock input CLK_IN/nCLK_IN accepts HCSL, LVPECL, LVHSTL and other types of differential signal. The differential input signal must meet both V_{swing} (amplitude) and V_{com} (DC offset) input requirement. The CLK_IN and nCLK_IN of this part is high input impedance without internal built-in termination. The termination requirement will depend on the driver type. Please consult with the vendor of the driver component to confirm the driver termination requirement. Figure 2A to Figure 2E show interface examples for the CLK_IN/nCLK_IN input driven by the most common driver types.

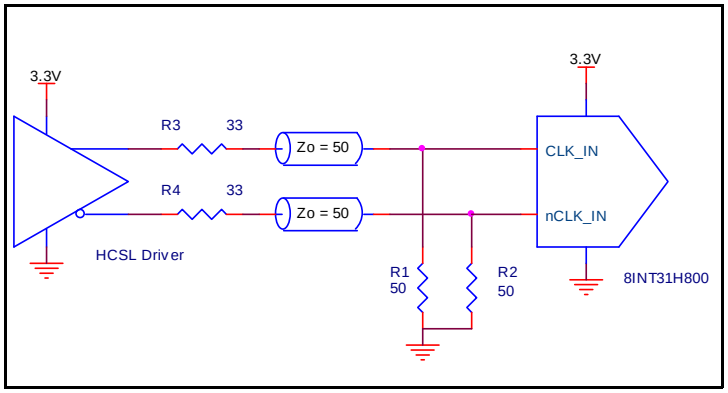


Figure 2A. 8INT31H800A Clock Input Driven by a HCSL Driver Example 1

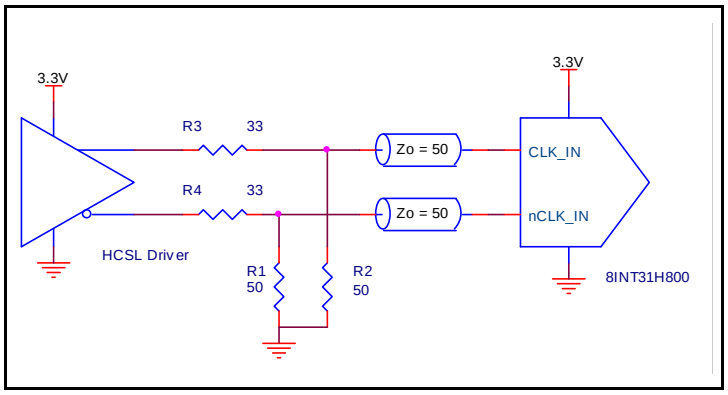


Figure 2B. 8INT31H800A Clock Input Driven by a HCSL Driver Example 2

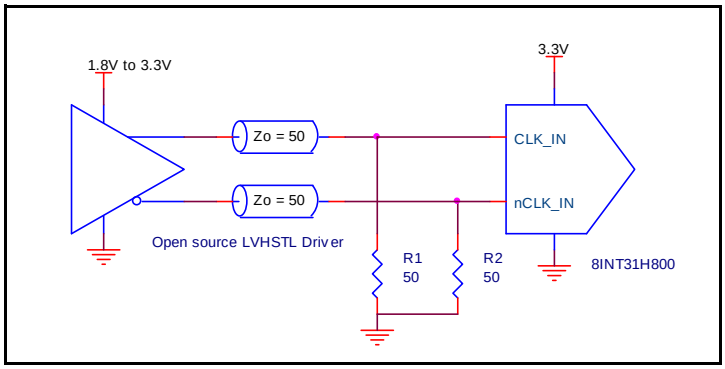


Figure 2C. 8INT31H800A Clock Input Driven by an Open Source LVHSTL Driver

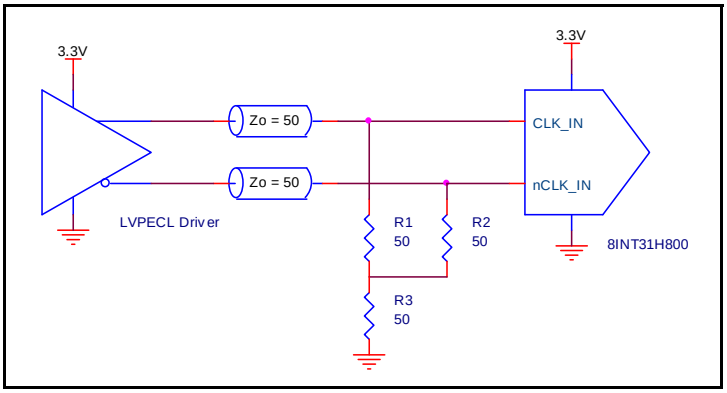


Figure 2D. 8INT31H800A Clock Input M Driven by an LVPECL Driver Example 1

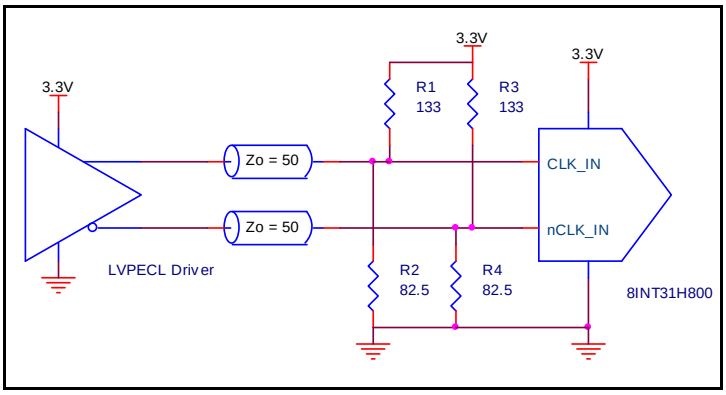


Figure 2E. 8INT31H800A Clock Input Driven by an LVPECL Driver Example 2

Power Considerations

This section provides information on power dissipation and junction temperature for the 8INT31H800A.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8INT31H800A is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for $V_{DD3.3}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

The maximum current at 85°C is as follows:

$I_{DD3.3\_MAX}$ = 195mA

$I_{DDO3.3\_MAX}$ = 30mA

Power $(core)_{MAX} = V_{DD3.3\_MAX} * (I_{DD3.3\_MAX} + I_{DDO3.3\_MAX})$ = 3.465V * 225mA = **779.625mW**

- Power $(Output)_{MAX}$ = 38.82mW/Loaded Output pair
  If all outputs are loaded, the total power is 8 * 38.82mW = 310.56mW

Total Power = 779.625mW + 310.56mW = 1090.18mW

2. Junction Temperature.

Junction temperature, T_J, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_J, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_J is as follows: $T_J = \theta_{JA} * Pd\_total + T_A$

T_J = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 4 below.

Therefore, T_J for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.09W * 33.1°C/W = 121.1°C. This is below the limit of 125°C.

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 4. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

3. Calculations and Equations

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in Figure 3.

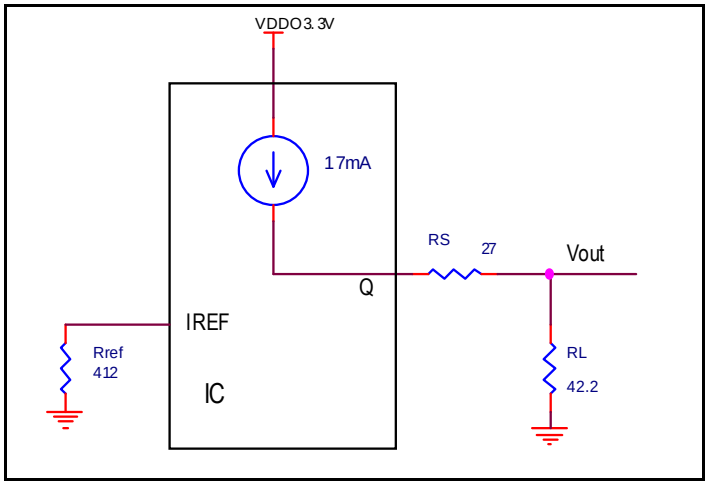


Figure 3. HSCL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 42.5Ω load to ground.

The highest power dissipation occurs when $V_{DDO3.3\_MAX}$.

Power = $(V_{DDO3.3\_MAX} - V_{OUT}) * I_{OUT}$

since $V_{OUT} - I_{OUT} * R_L$.

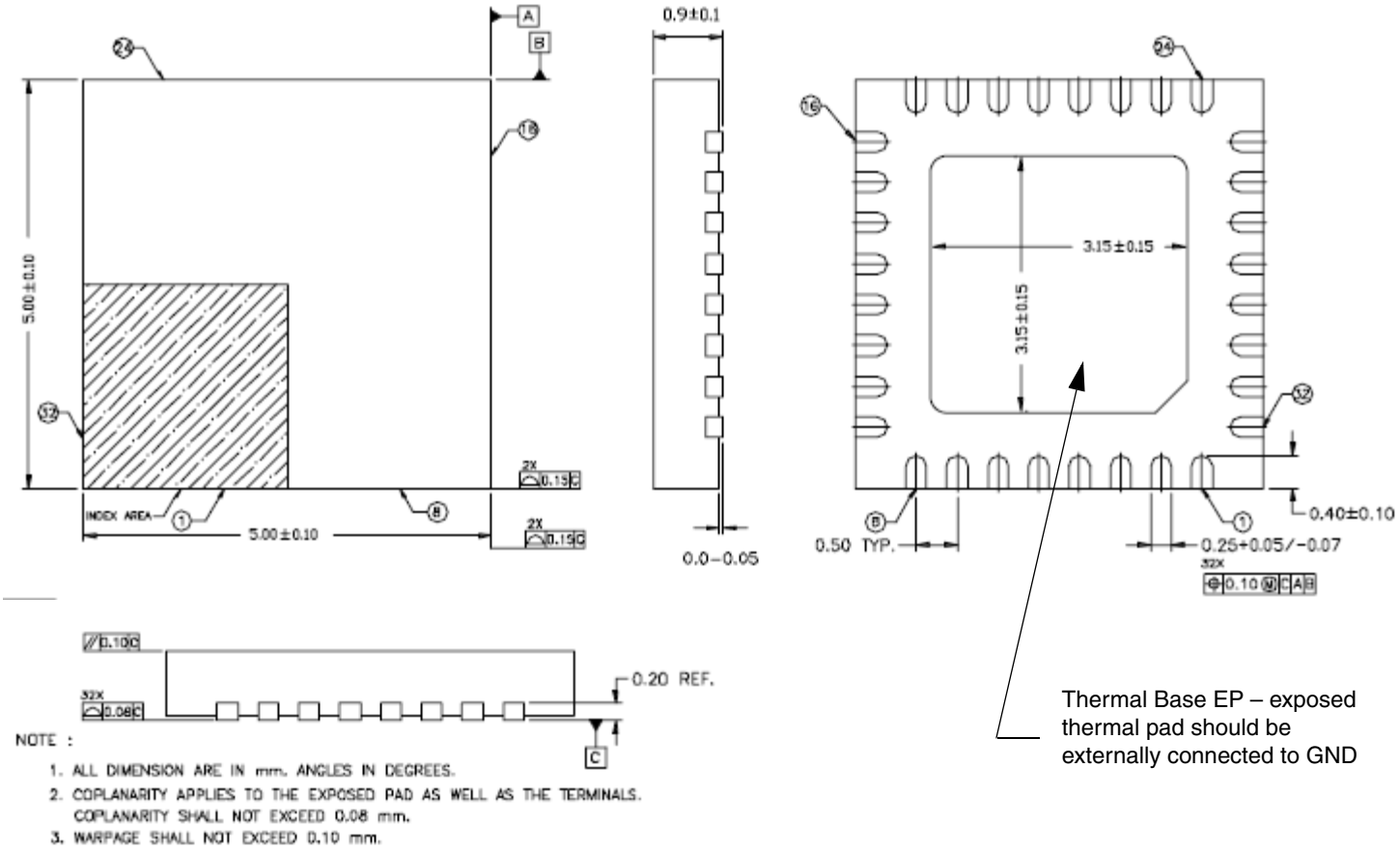
$= (V_{DDO3.3\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * (42.5\Omega + 27\Omega)) * 17mA$

Total Per Dissipation per output pair = 38.82mW

Package Outline and Package Dimensions (32-pin VFQFPN, 0.50mm pitch)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Table 5. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8INT31H800ANLGI	IDT8INT31H800ANLGI	32-pin VFQFN, Lead-Free	Tray	-40°C to 85°C
8INT31H800ANLGI8	IDT8INT31H800ANLGI	32-pin VFQFN, Lead-Free	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
2			Deleted *Confidential label* from footer of datasheet.	12/9/14

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com