INTEGRATED WIRELESS POWER SUPPLY RECEIVER, Qi (WIRELESS POWER CONSORTIUM) COMPLIANT

Check for Samples: bq51011, bq51013

FEATURES

- **Integrated Wireless Power Receiver Solution with a 5V Regulated Supply**
  - **93% Overall Peak AC-DC Efficiency**
  - **Full Synchronous Rectifier**
  - **WPC v1.0 Compliant Communication Control**
  - **Output Voltage Conditioning**
  - **Only IC Required Between RX coil and 5V DC Output Voltage**
- **Dynamic Rectifier Control for Improved Load Transient Response**
- **Supports 20-V Maximum Input**
- **Low-power Dissipative Rectifier Overvoltage Clamp (V_{OVP} = 15V)**
- **Thermal Shutdown**
- **Single NTC/Control Pin for Optimal Safety and I/O Between Host**
- **Stand-alone Digital Controller**
- **1.9 x 3mm DSBG or 4.5 x 3.5mm QFN Package**

APPLICATIONS

- **WPC Compliant Receivers**
- **Cell Phones, Smart Phones**
- **Headsets**
- **Digital Cameras**
- **Portable Media Players**
- **Hand-held Devices**

DESCRIPTION

The bq5101x is an advanced, integrated, receiver IC for wireless power transfer in portable applications. The device provides the AC/DC power conversion while integrating the digital control required to comply with the Qi v1.0 communication protocol. Together with the bq500210 transmitter controller, the bq5101x enables a complete contact-less power transfer system for a wireless power supply solution. By utilizing near-field inductive power transfer, the receiver coil embedded in the portable device receives the power transmitted by the transmitter coil via mutually coupled inductors. The AC signal from the receiver coil is then rectified and regulated to be used as a power supply for down-system electronics. Global feedback is established from the secondary to the transmitter in order to stabilize the power transfer process via back-scatter modulation. This feedback is established by using the Qi v1.0 communication protocol supporting up to 5W applications.

The device integrates a low-impedance full synchronous rectifier, low-dropout regulator, digital control, and accurate voltage and current loops. The entire power stage (rectifier and LDO) utilize low resistive NMOS FET's to ensures high efficiency and low power dissipation.

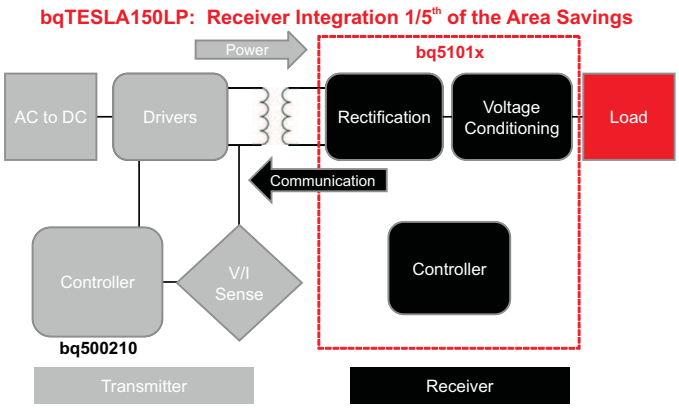


Figure 1. Wireless Power Consortium (WPC or Qi) Inductive Power System

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

Part NO	Marking	Function	Package	Ordering Number (Tape and Reel)	Quantity
bq51013	bq51013	5V Regulated Power Supply	DSBGA-YFF	bq51013YFFR	3000
				bq51013YFFT	250
	WAES		QFN-RHL(1)	bq51013RHLR	3000
				bq51013RHLT	250
bq51011	bq51011	Current Limited Power Supply	DSBGA-YFF	bq51011YFFR	3000
				bq51011YFFT	250

(1) Product Preview

AVAILABLE OPTIONS

Device	Function	V_{AD_OVP}	$V_{RECT-OVP}$	$V_{RECT(REG)}$	$V_{OUT(REG)}$	Communication Current Limit
bq51013	5V Power Supply	none	15V	Dynamic	5V	None
bq51011	5V Current Limited Power Supply		15V	Tracks V_{OUT}	5V	400mA + Dynamic I_{Lim}

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	PIN	VALUES		UNITS
		MIN	MAX	
Input Voltage	AC1, AC2, RECT, COMM1, COMM2, OUT, $\overline{CHG}$	-0.3	20	V
	AD, $\overline{AD\text{-}EN}$	-0.3	30	V
	BOOT1, BOOT2	-0.3	26	V
Input Current	AC1, AC2		1	A(RMS)
Output Current	OUT		1.5	A
Output Sink Current	$\overline{CHG}$		15	mA
	COMM1, COMM2		1	A
Junction temperature, T_J		-40	150	°C
Storage temperature, T_{STG}		-65	150	°C
ESD Rating (HBM) (100pF, 1.5KΩ)	All	2KV		

(1) All voltages are with respect to the VSS terminal, unless otherwise noted.
(2) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		RHL	YFF	UNITS
		20 PiNS	28 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	37.7	58.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	35.5	0.2	
θ_{JB}	Junction-to-board thermal resistance	13.6	9.1	
ψ_{JT}	Junction-to-top characterization parameter	0.5	1.4	
ψ_{JB}	Junction-to-board characterization parameter	13.5	8.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.7	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	PINS	MIN	MAX	UNITS
Input voltage range, V_{IN}	RECT	4	10	V
Input current, I_{IN}	RECT		1.5	A
Output current, I_{OUT}	OUT		1.5	A
Sink current, $I_{\overline{AD\text{-}EN}}$	$\overline{AD\text{-}EN}$		1	mA
COMM sink current, I_{COMM}	COMM		500	mA
Junction Temperature, T_J		0	125	ºC

TYPICAL APPLICATION SCHEMATICS

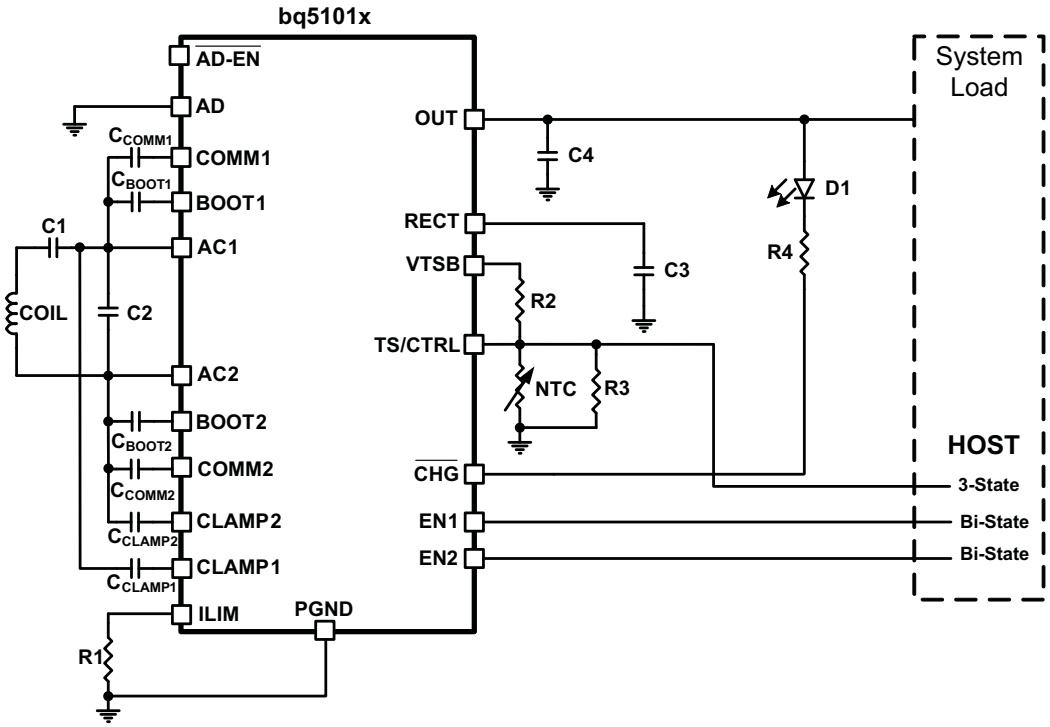


Figure 2. bq5101x Used as a Wireless Power Receiver and Power Supply for System Loads

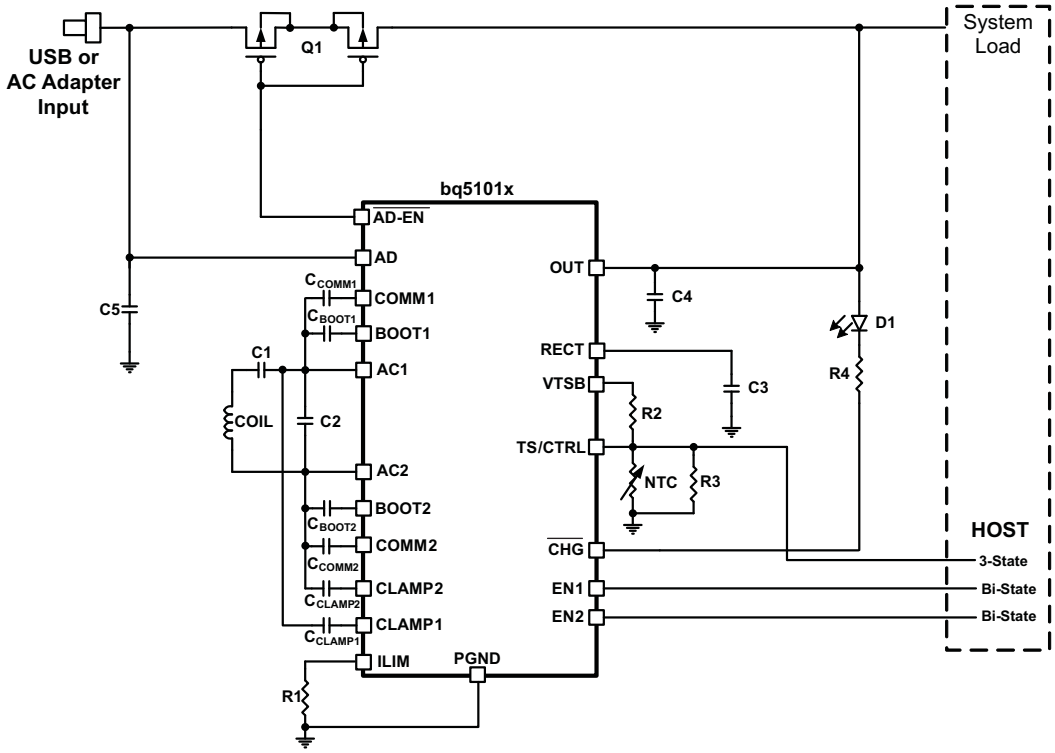


Figure 3. bq5101x Used as a Wireless Power Receiver and Power Supply for System Loads With Adapter Power-Path Multiplexing

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO	Undervoltage lock-out		V_{RECT}: 0V → 3V	2.6	2.7	2.8	V
V_{HYS}	Hysteresis on UVLO		V_{RECT}: 3V → 2V		250		mV
	Hysteresis on OVP		V_{RECT}: 16V → 5V		150		mV
V_{RECT}	Input overvoltage threshold		V_{RECT}: 5V → 16V	14.5	15	15.5	V
$V_{RECT-REG}$ (1)	Dynamic V_{RECT} Threshold 1		I_{LOAD} < 100 mA (I_{LOAD} rising)		7.08		V
	Dynamic V_{RECT} Threshold 2		100 mA < I_{LOAD} < 200 mA (I_{LOAD} rising)		6.28		
	Dynamic V_{RECT} Threshold 3		200 mA < I_{LOAD} < 400 mA (I_{LOAD} rising)		5.53		
	Dynamic V_{RECT} Threshold 4		I_{LOAD} > 400 mA (I_{LOAD} rising)		5.11		
I_{LOAD}	I_{LOAD} Hysteresis for dynamic V_{RECT} thresholds		I_{LOAD} falling		40		mA
$V_{RECT-TRACK}$	Tracking V_{RECT} regulation above V_{OUT}	bq51011	V_{OUT} = 3.5 V, I_{OUT} = K_{ILIM} / R_{ILIM} > 250mA		250		mV
$I_{RECT-REG}$	Percentage of I_{LIM} at which $V_{RECT(REG)}$ begins to track V_{OUT}	bq51011	I_{LOAD} rising		60%		
	Hysteresis percentage of I_{LOAD} at which $V_{RECT(REG)}$ halts tracking VOUT	bq51011	I_{LOAD} falling		20%		
$V_{RECT-DPM}$	Rectifier undervoltage protection, restricts I_{OUT} at $V_{RECT-DPM}$			3	3.1	3.2	V

(1) For the bq51011, $V_{RECT-REG}$ only applies when $V_{RECT-TRACK}$ is not active.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RECT-REV}$	Rectifier reverse voltage protection when a supply is present at V_{OUT}		$V_{RECT-REV} = V_{OUT} - V_{RECT}$, V_{OUT} = 10V		9	8	V
Quiescent Current							
I_{RECT}	Active chip quiescent current consumption from RECT		I_{LOAD} = 0mA, 0°C ≤ T_J ≤ 85°C		8	10	mA
			I_{LOAD} = 300mA, 0°C ≤ T_J ≤ 85°C		2	2.5	mA
I_{OUT}	Quiescent current at the output when wireless power is disabled (Standby)		V_{OUT} = 5V, 0°C ≤ T_J ≤ 85°C		20	35	µA
I_{LIM} Short Circuit							
R_{ILIM}	Highest value of I_{LIM} resistor considered a fault (short). Monitored for I_{OUT} > 100 mA		R_{ILIM}: 200Ω → 50Ω. I_{OUT} latches off, cycle power to reset			120	Ω
t_{DGL}	Deglitch time transition from I_{LIM} short to I_{OUT} disable				1		ms
I_{LIM_SC}	$I_{LIM-SHORT,OK}$ enables the I_{LIM} short comparator when I_{OUT} is greater than this value		I_{LOAD}: 0 → 200mA	90	105	125	mA
I_{OUT}	Maximum output current limit, C_L		Maximum I_{LOAD} that will be delivered for 1 ms when I_{LIM} is shorted			2.4	A
OUTPUT							
$V_{OUT-REG}$	Regulated output voltage		I_{LOAD} = 1000 mA	4.85	4.95	5	V
			I_{LOAD} = 1 mA	4.95	5	5.05	
V_{DO}	Drop-out voltage, RECT to OUT		I_{LOAD} = 1A		110	190	mV
K_{ILIM}	Current programming factor		$R_{LIM} = K_{ILIM} / I_{ILIM}$, I_{LOAD} = 1 A	280	300	320	AΩ
I_{ILIM}	Current limit programming range					1500	mA
V_{OUT_SC}	OUT pin short-circuit detection/pre-charge threshold	bq51011	V_{OUT}: 3 V → 0.5 V, no deglitch	0.7	0.8	0.9	V
	V_{OUT_SC} hysteresis	bq51011	V_{OUT}: 0.5 V → 3 V		100		mV
I_{COMM} (2)	Current limit during WPC communication	bq51011	$I_{LOAD} = I_{ILIM}$	365	390	420	mA
I_{OUT_SC}	Source current to OUT pin during short-circuit detection	bq51011	V_{OUT} = 0V, 0°C ≤ T_J ≤ 85°C		15	25	mA
TS / CTRL							
V_{TS}	TS Bias Voltage		$I_{TS-Bias}$ < 100µA (periodically driven see t_{TS}/CTRL-Meas)	2.1	2.2	2.3	V
I_{TS}	TS-Bias Short circuit protection		$V_{TS-Bias}$ = 0V	1		3	mA
V_{COLD}	Rising threshold		V_{TS}: 50% → 60%	54	56	58	%$V_{TS-Bias}$
	Falling hysteresis		V_{TS}: 60% → 50%		1		
V_{HOT}	Falling threshold		V_{TS}: 20% → 15%	17	18	19	
	Rising hysteresis		V_{TS}: 15% → 20%		1		
V_{CTRL}	CTRL pin threshold for a high		$V_{TS/CTRL}$: 50 → 150mV	80	100	130	mV
	CTRL pin threshold for a low		$V_{TS/CTRL}$: 150 → 50mV	50	80	100	mV
$t_{TS/CTRL}$	Time VTS-Bias is active when TS measurements occur		Synchronous to the communication period		24		ms
t_{TS}	Deglitch time for all TS comparators				10		ms
THERMAL PROTECTION							
T_J	Thermal shutdown temperature				155		°C
	Thermal shutdown hysteresis				20		°C

(2) Dynamic communication current limit enables the 400mA current limit only when the output current is equal to the programmed current limit (I_{ILIM}) for the bq51011.

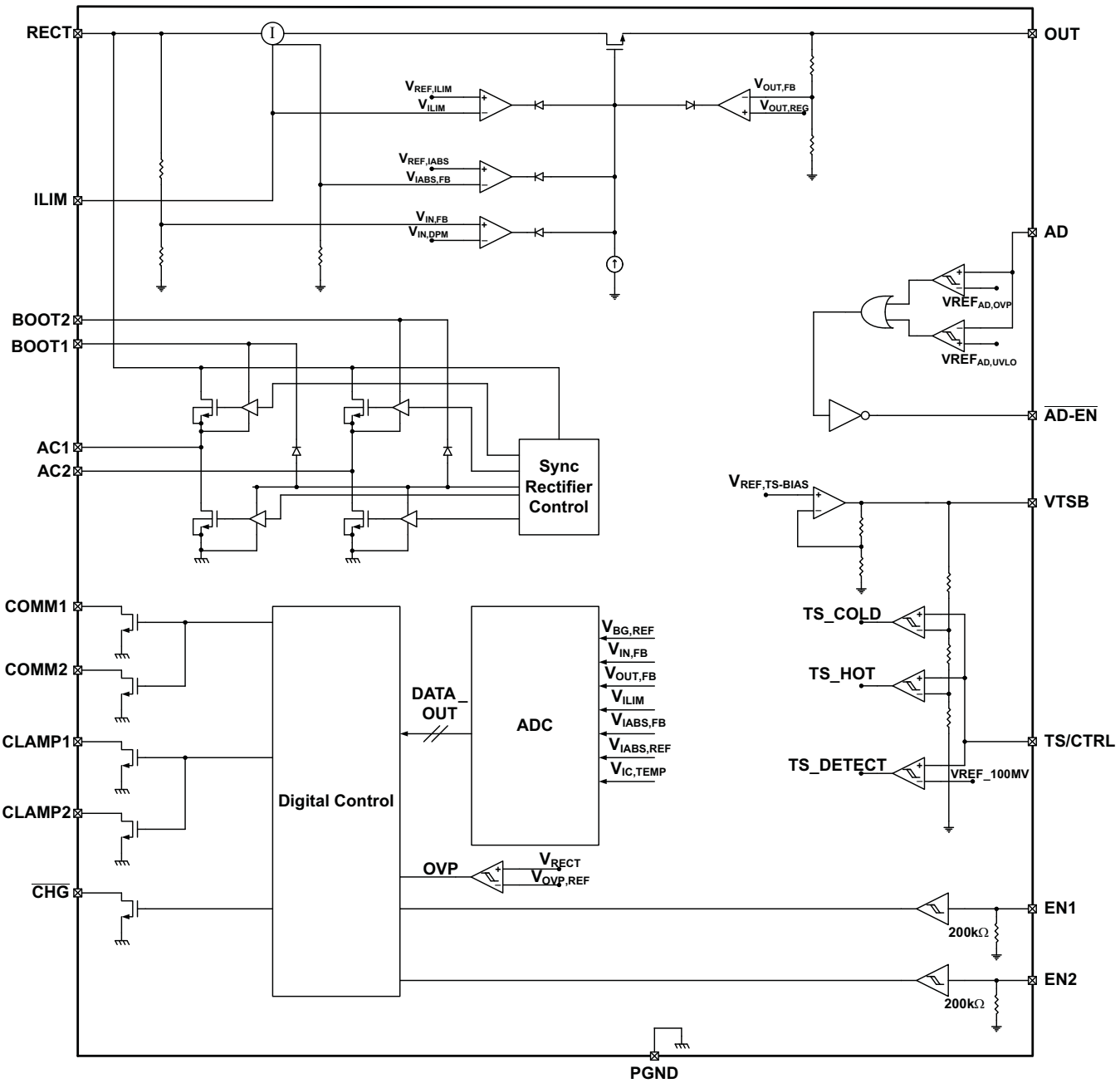
ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

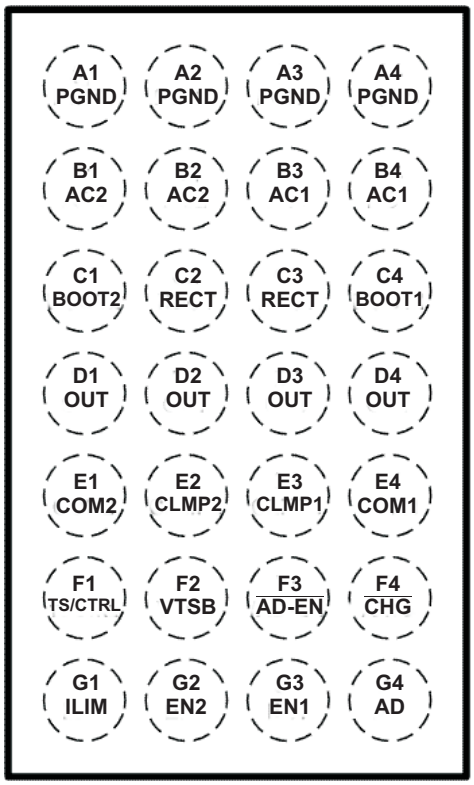
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOGIC LEVELS ON $\overline{CH}$						
V_{OL}	Open drain $\overline{CHG}$ pin	I_{SINK} = 5mA			500	mV
I_{OFF}	$\overline{CHG}$ leakage current when disabled	$V_{\overline{CHG}}$ = 20 V, 0°C ≤ T_J ≤ 85°C			1	µA
COMM PIN						
$R_{DS(ON)}$	Comm1 and Comm2	V_{RECT} = 4V		1.5		Ω
f_{COMM}	Signaling frequency on COMM pin			2.00		Kb/s
I_{OFF}	Comm pin leakage current	V_{COMM1} = 20V, V_{COMM2} = 20V			1	µA
CLAMP PIN						
$R_{DS(ON)}$	Clamp1 and Clamp2			0.5		Ω
Adapter Enable						
$V_{\overline{AD-EN}}$	V_{AD} Rising threshold voltage. EN-UVLO	V_{AD} 0 → 5 V	3.5	3.6	3.8	V
	$V_{\overline{AD-EN}}$ hysteresis, EN-HYS	V_{AD} 5 → 0 V		400		mV
I_{AD}	Input leakage current	V_{RECT} = 0V, V_{AD} = 5V, 0°C ≤ T_J ≤ 85°C			55	µA
R_{AD}	Pull-up resistance from $\overline{AD-EN}$ to OUT when adapter mode is disabled and V_{OUT} > V_{AD}, EN-OUT	V_{AD} = 0, V_{OUT} = 5		200	350	Ω
V_{AD}	Voltage difference between V_{AD} and $V_{\overline{AD-EN}}$ when adapter mode is enabled, EN-ON	V_{AD} = 5V, 0°C ≤ T_J ≤ 85°C	3	4.5	5	V
		V_{AD} = 9V, 0°C ≤ T_J ≤ 85°C	3	6	7	
Synchronous Rectifier						
I_{OUT}	I_{OUT} at which the synchronous rectifier enters half synchronous mode, SYNC_EN	I_{LOAD} 300 → 200mA	200	225	250	mA
	Hysteresis for $I_{OUT,RECT-EN}$ (full-synchronous mode enabled)	I_{LOAD} 200 → 300mA		40		mA
$V_{HS-DIODE}$	High-side diode drop when the rectifier is in half synchronous mode	$I_{AC-VRECT}$ = 250mA		0.7		V
EN1 and EN2						
V_{IL}	Input low threshold for EN1 and EN2				0.4	V
V_{IH}	Input high threshold for EN1 and EN2		1.3			V
R_{PD}	EN1 and EN2 pull down resistance			200		kΩ
ADC						
V_{RECT}	Rectified power measurement	0W – 5W of rectified power		±6%		

DEVICE INFORMATION

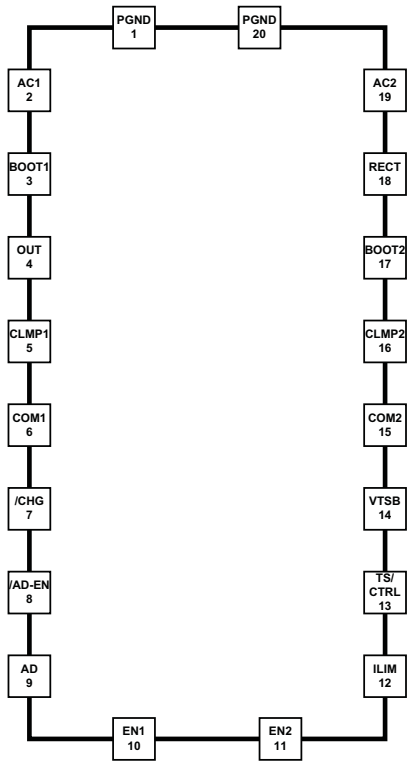
SIMPLIFIED BLOCK DIAGRAM



YFF Package
(TOP VIEW)



RHL Package
(TOP VIEW)



PIN FUNCTIONS

NAME	YFF	RHL	I/O	DESCRIPTION
AC1	B3, B4	2	I	AC input power from receiver coil antenna.
AC2	B1, B2	19	I	
BOOT1	C4	3	O	Bootstrap capacitors for driving the high-side FETs of the synchronous rectifier. Connect a 10nF ceramic capacitor from BOOT1 to AC1 and from BOOT2 to AC2.
BOOT2	C1	17	O	
RECT	C2, C3	18	O	Filter capacitor for the internal synchronous rectifier. Connect a ceramic capacitor to PGND. Depending on the power levels, the value may be 4.7µF to 22µF.
OUT	D1, D2, D3, D4	4	O	Output pin, delivers power to the load.
COM1	E4	6	O	Open-drain output used to communicate with primary by varying reflected impedance. Connect through a capacitor to either AC1 or AC2 for capacitive load modulation (COM2 must be connected to the alternate AC1 or AC2 pin). For resistive modulation connect COM1 and COM2 to RECT via a single resistor; connect through separate capacitors for capacitive load modulation.
COM2	E1	15	O	Open-drain output used to communicate with primary by varying reflected impedance. Connect through a capacitor to either AC1 or AC2 for capacitive load modulation (COM1 must be connected to the alternate AC1 or AC2 pin). For resistive modulation connect COM1 and COM2 to RECT via a single resistor; connect through separate capacitors for capacitive load modulation.
CLMP2, CLMP1	E2, E3	5 16	O	Open drain FETs which are utilized for a non-power dissipative over-voltage AC clamp protection. When the RECT voltage goes above 15 V, both switches will be turned on and the capacitors will act as a low impedance to protect the IC from damage. If used, CLMP1 is required to be connected to AC1, and CLMP2 is required to be connected to AC2 via 0.47µF capacitors.
PGND	A1, A2, A3, A4	1, 20		Power ground

PIN FUNCTIONS (continued)

NAME	YFF	RHL	I/O	DESCRIPTION
ILIM	G1	12	I/O	Programming pin for the over current limit. Connect external resistor to V_{SS}. Size R_{ILIM} with the following equation: $R_{ILIM} = 300 / I_{(max)}$ where $I_{(max)}$ is the desired current limit for the power supply.
AD	G4	9	I	Connect this pin to the wired adapter input. When a voltage is applied to this pin wireless charging is disabled and $\overline{\text{AD-EN}}$ is driven low. Connect to GND through a 1µF capacitor. If unused, capacitor is not required and should be grounded directly.
$\overline{\text{AD-EN}}$	F3	8	O	Push-pull driver for external PFET connecting AD and OUT. This node is pulled to the higher of OUT and AD when turning off the external FET. This voltage tracks approximately 4V below AD when voltage is present at AD and provides a regulated VSG bias for the external FET. Float this pin if unused.
TS/CTRL	F1	13	I	Must be connected to ground and pulled up to VTSB via two series resistors. If an NTC function is not desired, size R2 to be twice that of R3. As a CTRL pin pull to ground to send End Power/Temperature Fault message to the transmitter, pull-up to send End Power/Termination message to the transmitter.
EN1	G3	10	I	Inputs that allow user to enable/disable wireless and wired charging <EN1 EN2> <00> wireless charging is enabled unless the AD voltage is > 3.6 V. <01> AD mode is disabled, wireless charging enabled. <10> $\overline{\text{AD-EN}}$ pulled low, wireless charging disabled. <11> wired and wireless charging disabled.
EN2	G2	11	I	
VTSB	F2	14	O	2.2V LDO that periodically biases the TS/CTRL resistor network. Connect to TS/CTRL via a resistor
$\overline{\text{CHG}}$	F4	7	O	Open-drain output – active when output current is being delivered to the load (i.e. when the output of the supply is enabled).

TYPICAL CHARACTERISTICS

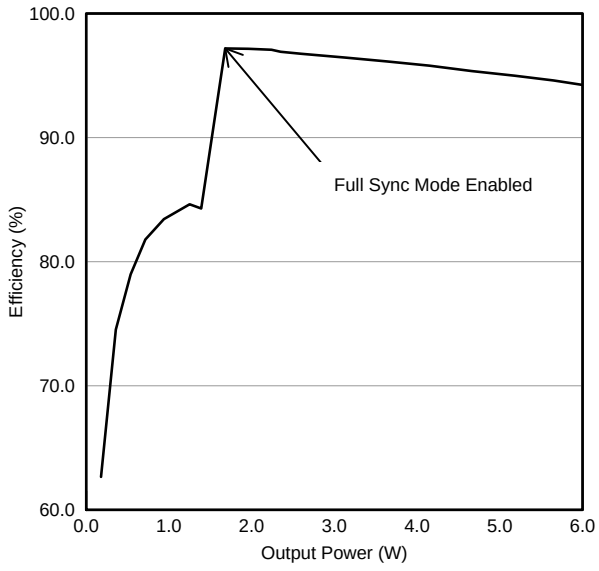


Figure 4. Rectifier Efficiency

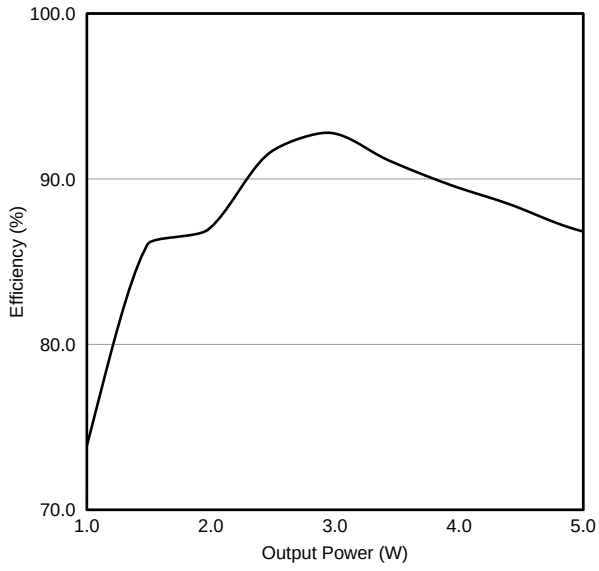


Figure 5. IC Efficiency from AC Input to DC Output

TYPICAL CHARACTERISTICS (continued)

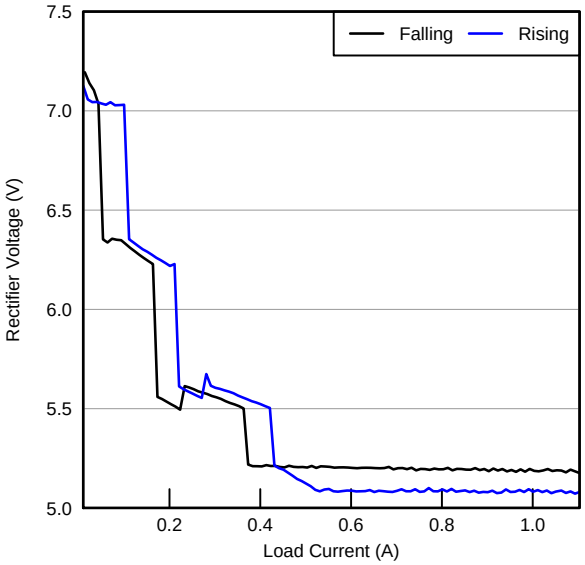


Figure 6. V_{RECT} vs. I_{LOAD}

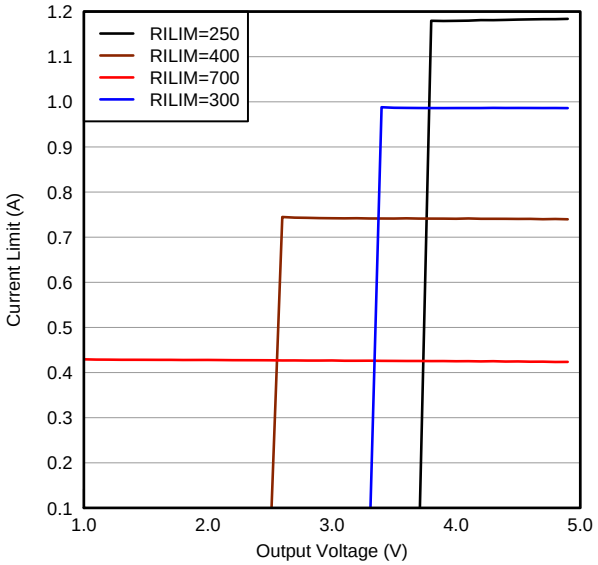


Figure 7. V_{OUT} Sweep (I-V Curve)(1)

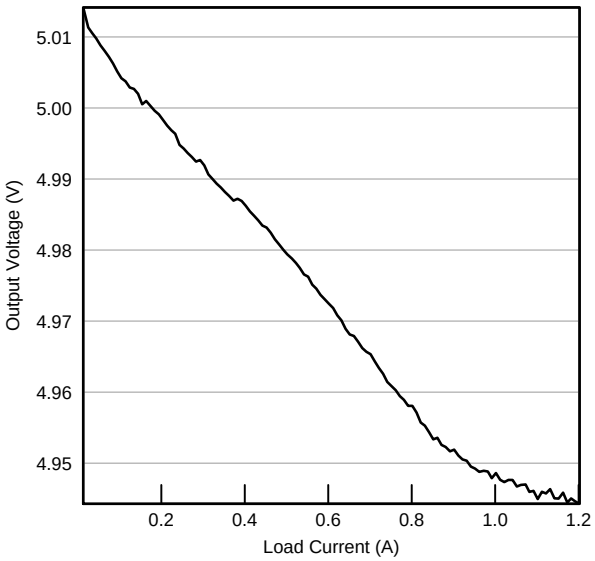


Figure 8. I_{LOAD} Sweep (I-V Curve)

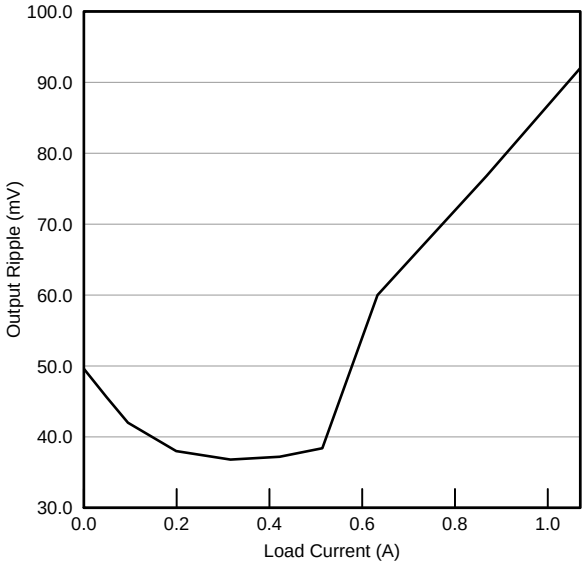


Figure 9. Output Ripple vs. I_{LOAD} (C_{OUT} = 1µF)

TYPICAL CHARACTERISTICS (continued)

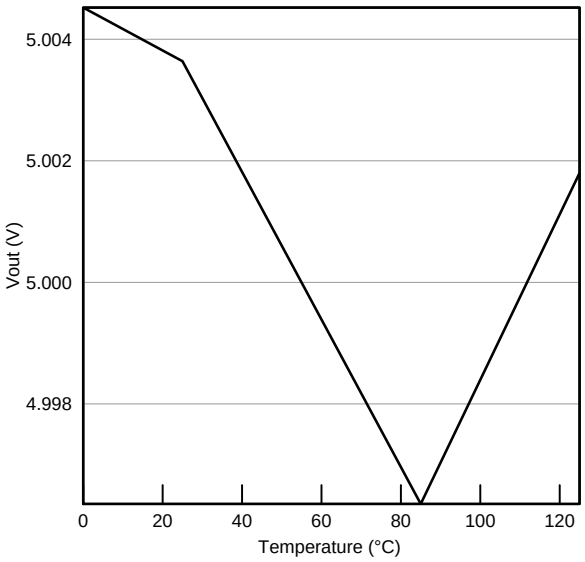


Figure 10. V_{OUT} vs Temperature

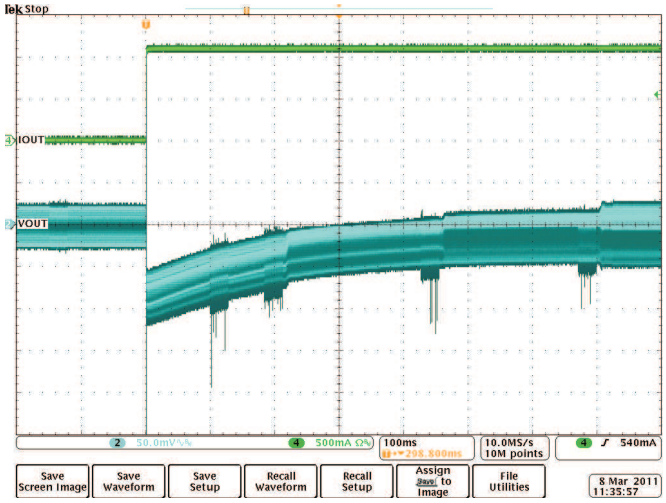


Figure 11. 1A Instantaneous Load Step(2)

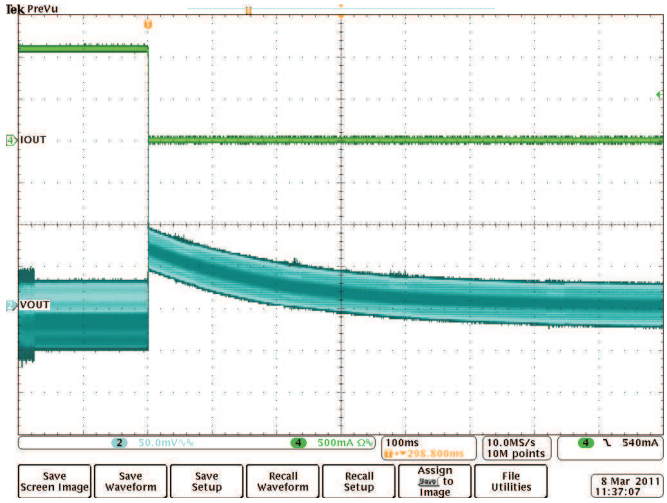


Figure 12. 1A Instantaneous Load Dump(2)

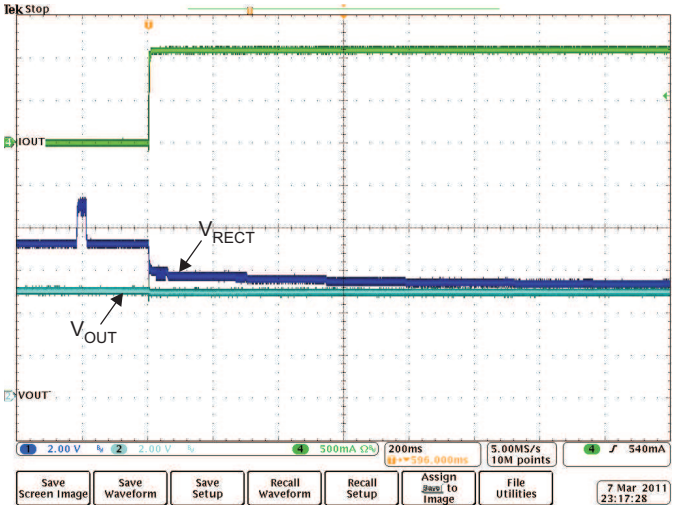


Figure 13. 1A Load Step Full System Response

TYPICAL CHARACTERISTICS (continued)

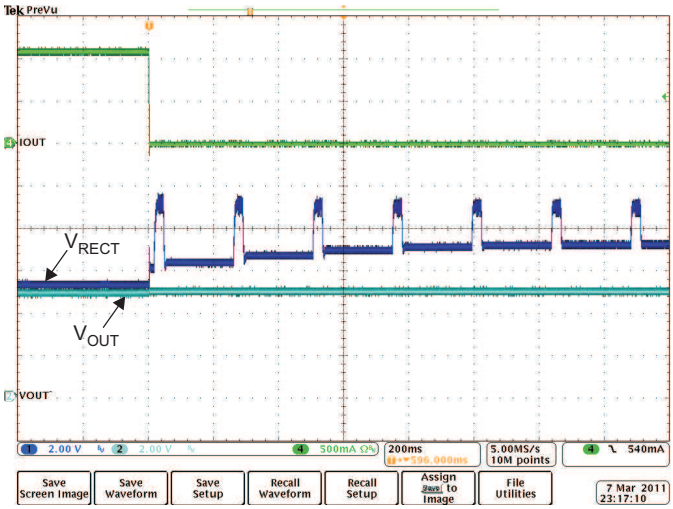


Figure 14. 1A Load Dump Full System Response

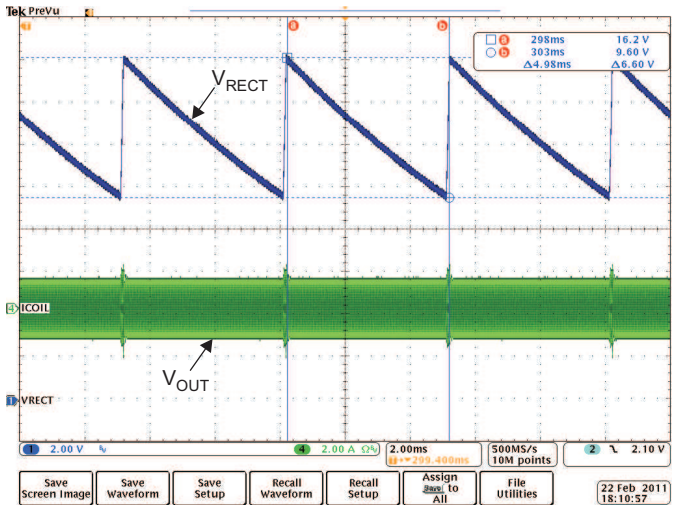


Figure 15. Rectifier Overvoltage Clamp (f_{op} = 110kHz)

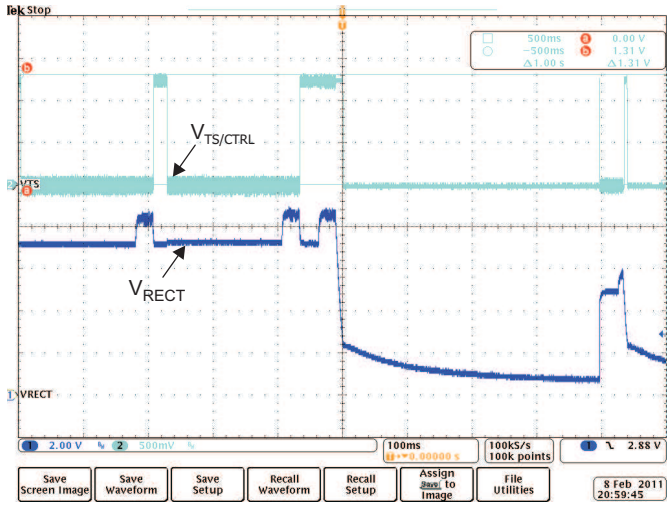


Figure 16. TS Fault

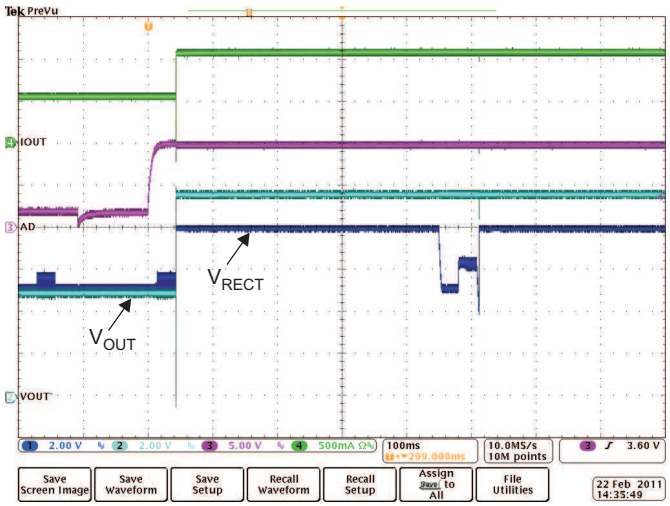


Figure 17. Adapter Insertion (V_{AD} = 10V)

TYPICAL CHARACTERISTICS (continued)

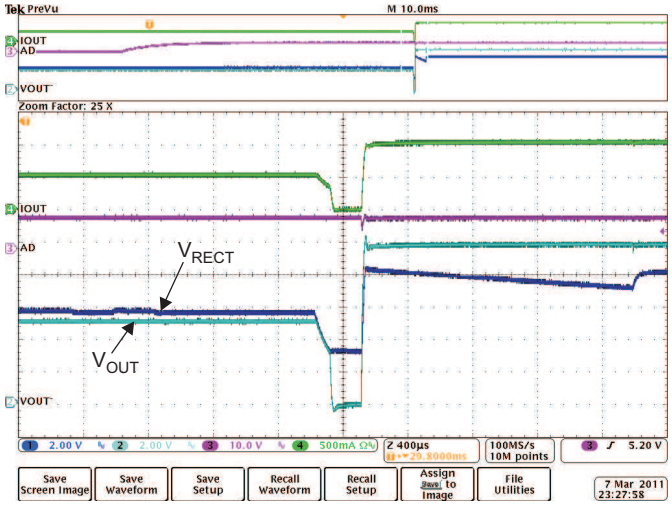


Figure 18. Adapter Insertion (V_{AD} = 10V) Illustrating Break-Before-Make Operation

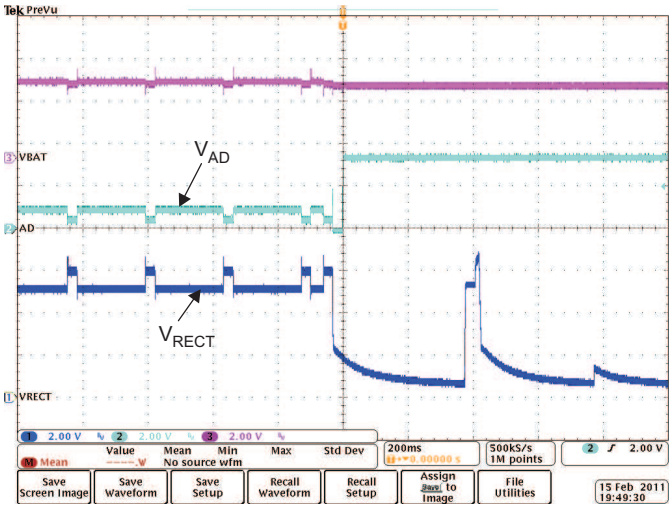


Figure 19. On the Go Enabled (V_{OTG} = 3.5V)(3)

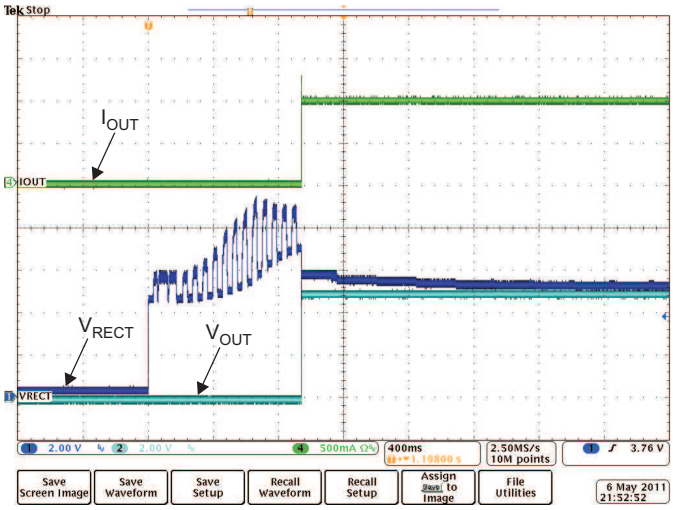


Figure 20. bq51013 Typical Startup with a 1A System Load

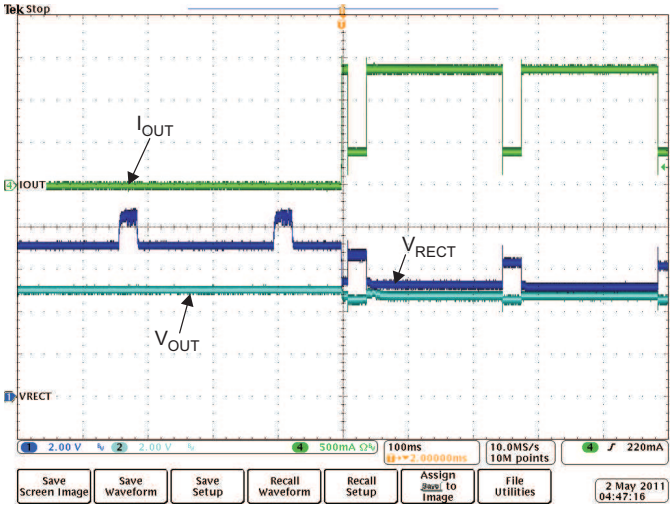


Figure 21. bq51011 Step Response with V_{OUT} = 4.8V and I_{LOAD} = I_{ILIM}

TYPICAL CHARACTERISTICS (continued)

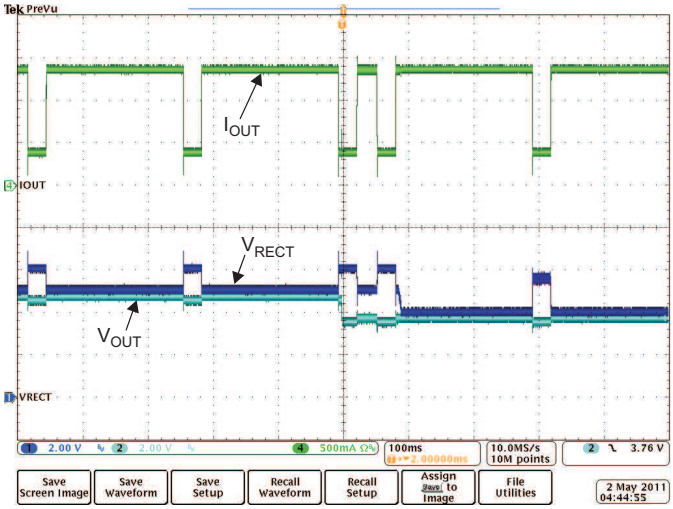


Figure 22. bq51011 Output Voltage Transition (V_{OUT} = 4.8V -> 3.5V) Illustrating $V_{RECT-TRACK}$

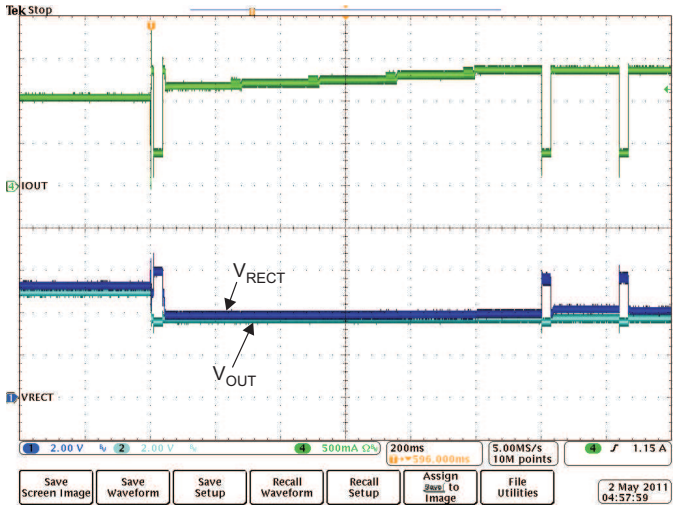


Figure 23. bq51011 Output Current Transition (I_{LOAD} < I_{ILIM} ≥ I_{LOAD} = I_{ILIM}) Illustrating Dynamic Communication Current Limit

(1) Curves illustrates the resulting I_{LIM} current by sweeping the output voltage at different R_{ILIM} settings. ILIM current collapses due to the increasing power dissipation as the voltage at the output is decreased—thermal shutdown is occurring.

(2) Total droop experienced at the output is dependent on receiver coil design. The output impedance must be low enough at that particular operating frequency in order to not collapse the rectifier below 5V.

(3) On the go mode is enabled by driving EN1 high. In this test the external PMOS is connected between the output of the bq5101x IC and the AD pin, therefore any voltage source on the output is supplied to the AD pin.

PRINCIPLE OF OPERATION

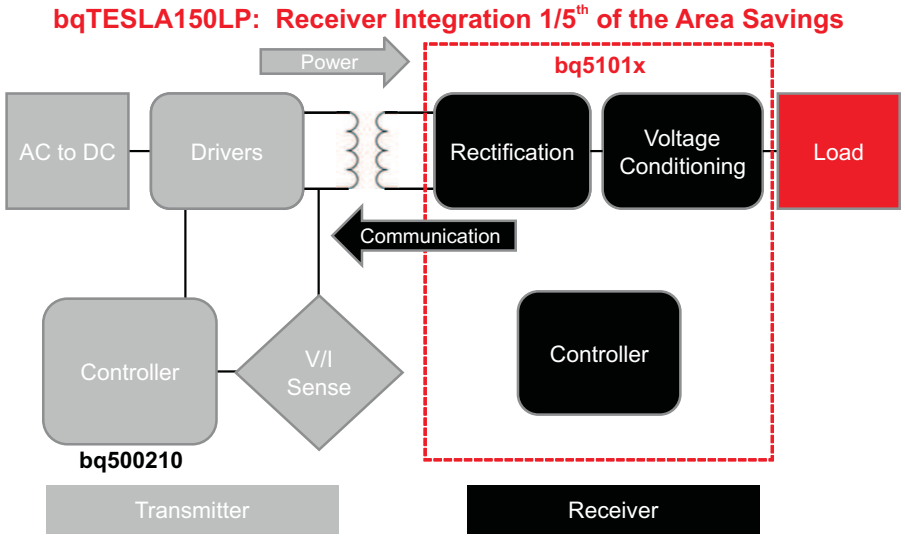


Figure 24. WPC Wireless Power System Indicating the Functional Integration of the bq5101x

A Brief Description of the Wireless System:

A wireless system consists of a charging pad (transmitter or primary) and the secondary-side equipment (receiver or secondary). There are coils in the charging pad and in the secondary equipment which are magnetically coupled to each other when the equipment is placed on the portable device. Power is then transferred from the transmitter to the receiver via coupled inductors (e.g. an air-core transformer). Controlling the amount of power transferred is achieved by sending feedback (error signal) communication to the primary (e.g. to increase or decrease power).

The receiver communicates with the transmitter by changing the load seen by the transmitter. This load variation results in a change in the transmitter coil current, which is measured and interpreted by a processor in the charging pad. The communication is digital - packets are transferred from the receiver to the transmitter. Differential Bi-phase encoding is used for the packets. The bit rate is 2-kbps.

Various types of communication packets have been defined. These include identification and authentication packets, error packets, control packets, end power packets, and power usage packets.

The transmitter coil stays powered off most of the time. It occasionally wakes up to see if a receiver is present. When a receiver authenticates itself to the transmitter, the transmiter will remain powered on. The receiver maintains full control over the power transfer using communication packets.

Using the bq5101x as a Wireless Power Supply: (See Figure 3)

Figure 3 is the schematic of a system which uses the bq5101x as power supply while power multiplexing the wired (adapter) port.

When the system shown in Figure 3 is placed on the charging pad, the receiver coil is inductively coupled to the magnetic flux generated by the coil in the charging pad which consequently induces a voltage in the receiver coil. The internal synchronous rectifier feeds this voltage to the RECT pin which has the filter capacitor C3.

The bq5101x identifies and authenticates itself to the primary using the COM pins by switching on and off the COM FETs and hence switching in and out C_{COMM}. If the authentication is successful, the transmitter will remain powered on. The bq5101x measures the voltage at the RECT pin, calculates the difference between the actual voltage and the desired voltage $V_{RECT-REG}$, (~7V for the bq51013 at no load) and sends back error packets to the primary. This process goes on until the input voltage settles at V_{IN-REG}. During a load transient, the dynamic rectifier algorithm will set the targets specified by $V_{RECT-REG}$ thresholds 1, 2, 3, and 4. This algorithm enhances the transient response of the power supply.

During power-up, the LDO is held off until the $V_{RECT-REG}$ threshold 1 converges. The voltage control loop ensures that the output voltage is maintained at $V_{OUT-REG}$ (~5V for the bq51013) to power the system. The bq5101x meanwhile continues to monitor the input voltage, and maintains sending error packets to the primary every 250ms. If a large transient occurs, the feedback to the primary speeds up to every 32ms in order to converge on an operating point in less time.

Input Overvoltage

If the input voltage suddenly increases in potential (e.g. a change in position of the equipment on the charging pad), the voltage-control loop inside the bq5101x becomes active, and prevents the output from going beyond $V_{OUT-REG}$. The receiver then starts sending back error packets to the transmitter every 30ms until the input voltage comes back to the $V_{RECT-REG}$ target, and then maintains the error communication every 250ms.

If the input voltage increases in potential beyond V_{OVP}, the IC switches off the LDO and communicates to the primary to bring the voltage back to $V_{RECT\ -REG}$. In addition, a proprietary voltage protection circuit is activated by means of C_{CLAMP1} and C_{CLAMP2} that protects the IC from voltages beyond the maximum rating of the IC (e.g. 20V).

Adapter Enable Functionality and Enable1/Enable2 Control

Figure 3 is an example application that shows the bq5101x used as a wireless power receiver that can power mutliplex between wired or wireless power for the down-system electronics. In the default operating mode pins EN1 and EN2 are low, which activates the adapter enable functionality. In this mode, if an adapter is not present the AD pin will be low, and $\overline{\text{AD-EN}}$ pin will be pulled to the higher of the OUT and AD pins so that the PMOS between OUT and AD will be turned off. If an adapter is plugged in and the voltage at the AD pin goes above 3.6 V then wireless charging is disabled and the $\overline{\text{AD-EN}}$ pin will be pulled approximately 4 V below the AD pin to connect AD to the secondary charger. The difference between AD and AD-EN is regulated to a maximum of 7V to ensure the V_{GS} of the external PMOS is protected.

The EN1 and EN2 pins include internal 200kΩ pull-down resistors, so that if these pins are not connected bq5101x defaults to $\overline{\text{AD-EN}}$ control mode. However, these pins can be pulled high to enable other operating modes as described in Table 1:

Table 1.

EN1	EN2	Result
0	0	Adapter control enabled. If adapter is present then secondary charger will be powered by adapter, otherwise wireless charging will be enabled when wireless power is available.
0	1	Adapter is disabled. Wireless charging will be enabled when wireless power is present.
1	0	$\overline{\text{AD-EN}}$ is pulled low, whether or not adapter voltage is present. This feature can be used, e.g., for USB OTG applications.
1	1	Adapter and wireless charging are disabled, i.e., power will never be delivered by the OUT pin in this mode.

As described in Table 1, pulling EN2 high disables the adapter mode and only allows wireless charging. In this mode the adapter voltage will always be blocked from the OUT pin. An application example where this mode is useful is when USB power is present at AD, but the USB is in suspend mode so that no power can be taken from the USB supply. Pulling EN1 high enables the off-chip PMOS regardless of the presence of a voltage. This function can be used in USB OTG mode to allow a charger connected to the OUT pin to power the AD pin. Finally, pulling both EN1 and EN2 high disables both wired and wireless charging.

NOTE

It is required to connect a back-to-back PMOS between AD and OUT so that voltage is blocked in both directions. Also, when AD mode is enabled no load can be pulled from the RECT pin as this could cause an internal device overvoltage in bq5101x.

End Power Transfer Packet (WPC Header 0x02)

The WPC allows for a special command for the receiver to terminate power transfer from the trasmitter termed End Power Transfer (EPT) packet. Table 2 specifies the v1.0 Reasons columb and their responding data field value. The Condition column corresponds to the values sent by the bq5101x for a given reason.

Table 2.

Reason	Value	Condition
Unknown	0x00	AD > 3.6V
Charge Complete	0x01	TS/CTRL = 1, or EN1 = 1, or <EN1 EN2> = <11>
Internal Fault	0x02	T_J > 150°C or R_{ILIM} < 100Ω
Over Temperature	0x03	TS < V_{HOT}, TS > V_{COLD}, or TS/CTRL < 100mV
Over Voltage	0x04	Not Sent
Over Current	0x05	Not Sent
Battery Failure	0x06	Not Sent
Reconfigure	0x07	Not Sent
No Response	0x08	VRECT target doesn't converge

Status Outputs

bq5101x has one status output, $\overline{\text{CHG}}$. This output is an open-drain NMOS device that is rated to 20V. The open-drain FET connected to the $\overline{\text{CHG}}$ pin will be turned on whenever the output of the power supply is enabled. Please note, the output of the power supply will not be enabled if the $V_{RECT-REG}$ does not converge at the no-load target voltage.

Communication

bq5101x provides two identical, integrated communication FETs which are connected to the pins COMM1 and COMM2. These FETs are used for modulating the secondary load current which allows bq5101x to communicate error control and configuration information to the transmitter. Figure 25 below shows how the COMM pins can be used for resistive load modulation. Each COMM pin can handle at most a 24Ω communication resistor. Therefore, if a COMM resistor between 12Ω and 24Ω is required COM1 and COM2 pins must be connected in parallel. bq5101x does not support a COMM resistor less than 12Ω.

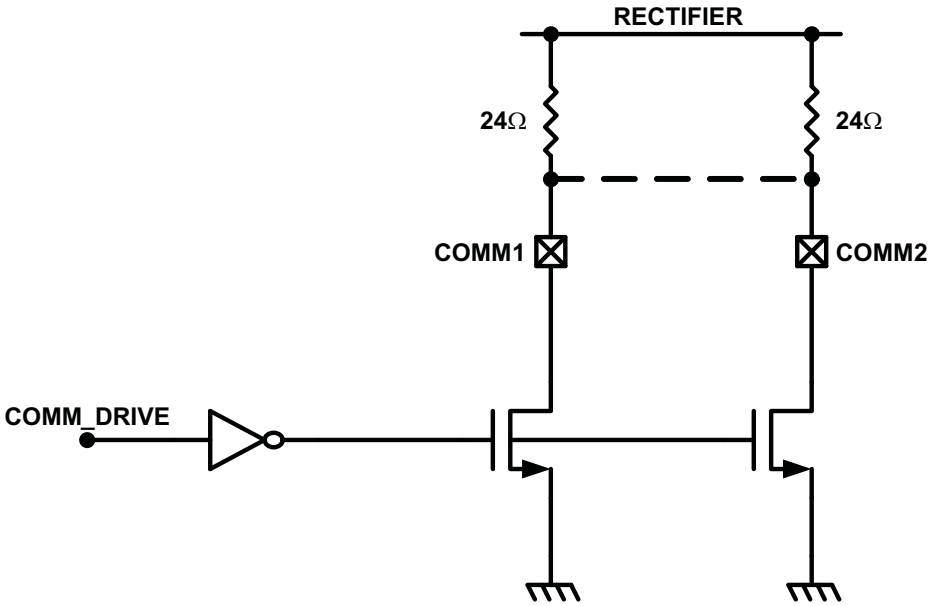


Figure 25. Resistive Load Modulation

In addition to resistive load modulation, the bq5101x is also capable of capacitive load modulation as shown in Figure 26 below. In this case, a capacitor is connected from COMM1 to AC1 and from COMM2 to AC2. When the COMM switches are closed there is effectively a 22nF capacitor connected between AC1 and AC2. Connecting a capacitor in between AC1 and AC2 modulates the impedance seen by the coil, which will be reflected in the primary as a change in current.

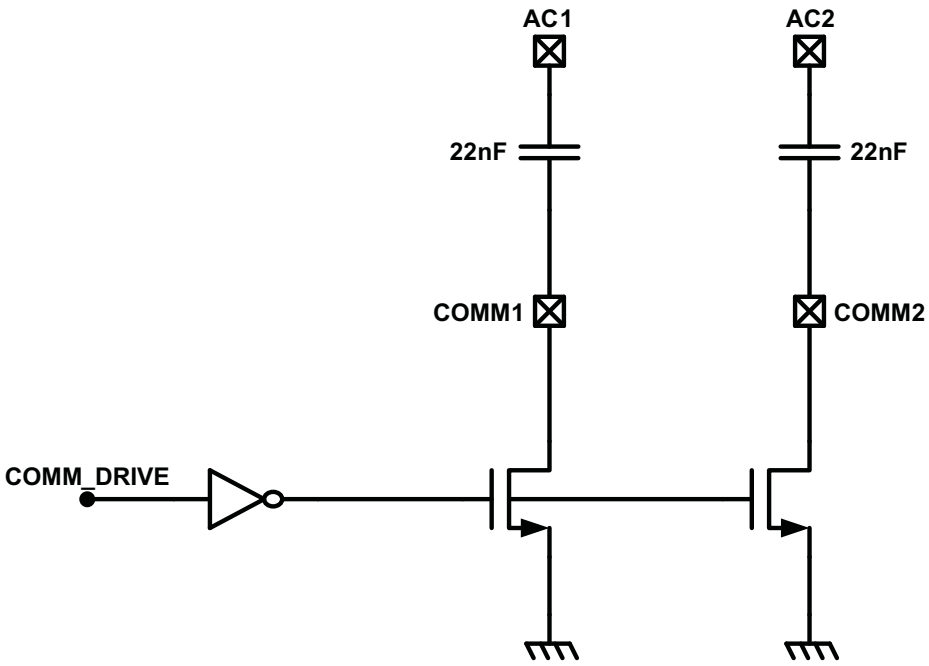


Figure 26. Capacitive Load Modulation

Synchronous Rectification

The bq5101x provides an integrated, self-driven synchronous rectifier that enables high-efficiency AC to DC power conversion. The rectifier consists of an all NMOS H-Bridge driver where the backgates of the diodes are configured to be the rectifier when the synchronous rectifier is disabled. During the initial startup of the WPC system the synchronous rectifier is not enabled. At this operating point, the DC rectifier voltage is provided by the diode rectifier. Once V_{RECT} is greater than UVLO, half synchronous mode will be enabled until the load current surpasses 250mA. Above 250mA the synchronous rectifier will stay enabled until the load current drops back below 250mA where half synchronous mode will be enabled instead.

Rectifier Tracking Mode (Fold-Back)

The bq51011 is a 5V power supply intended to run efficiently in current limit. In order to optimize the efficiency and power dissipation, the rectifier must track the output voltage within 250mV. This feature is termed $V_{RECT-TRACK}$ where the bq51011 monitors the status of the programmed current limit and the output voltage value. When the output current breaches the current limit of the power supply the controller sets the rectifier target voltage to the output voltage plus 250mV. This feature is illustrated in Figure 22. When the output current is equal to the current limit and the output voltage is transitioned from 4.8V to 3.5V the rectifier voltage will follow the transition. This is possible via the WPC system control loop where the bq51011 communicates to the Tx to adjust the operating point. This feature ensures that the internal LDO is always running near dropout for optimized efficiency when the output current is equal to the current limit of the power supply

Communication Current Limit (Comm. I_{LIM})

The bq51011 employs a 400mA current limit during the time it takes to send a communication packet to the Tx. This feature adds robustness to communication link between the Tx and Rx when the rectifier is in fold-back mode. Communication can be compromised while in fold-back mode because of less headroom (gain) across the internal LDO. When the current limit is reduced at a fixed operating frequency, the rectifier voltage increases (see Figure 22 where the output current reduces from the power supply current limit). This will increase the headroom across the LDO adding more gain between the output and the rectifier; therefore, increasing immunity to communication failure.

Dynamic Communication Current Limit (Dynamic I_{LIM})

The bq51011 employs the dynamic communication current limit feature in order to enable the communication current limit only when the power supply is operating in current limit mode ($I_{OUT} = I_{ILIM}$). This is illustrated in Figure 23 where the output current is transitioned from $I_{OUT} < I_{ILIM}$ to $I_{OUT} = I_{ILIM}$. This allows for systems to startup without the current limit enabled in order to provide better system performance (e.g. during a dead battery condition). The current limit is used during rectifier tracking mode to ensure stability of the communication back to the WPC transmitter. This adds robustness to the communication link.

Temperature Sense Resistor Network (TS)

bq5101x includes a ratiometric external temperature sense function. The temperature sense function has two ratiometric thresholds which represent a hot and cold condition. An external temperature sensor is recommended in order to provide safe operating conditions for the receiver product. This pin is best utilized for monitoring the surface that can be exposed to the end user (e.g. place the NTC resistor closest to the user).

Figure 27 allows for any NTC resistor to be used with the given V_{HOT} and V_{COLD} thresholds.

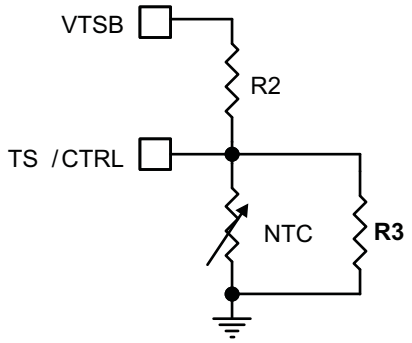


Figure 27. NTC Circuit Used for Safe Operation of the Wireless Receiver Power Supply

The resistors R2 and R3 can be solved by resolving the system of equations at the desired temperature thresholds. The two equations are:

$$\%V_{COLD} = \frac{\left(\frac{R3\ R_{NTC}|_{TCOLD}}{R3 + R_{NTC}|_{TCOLD}}\right)}{\left(\frac{R3\ R_{NTC}|_{TCOLD}}{R3 + R_{NTC}|_{TCOLD}}\right) + R2} \times 100 \quad (1)$$

$$\%V_{HOT} = \frac{\left(\frac{R3\ R_{NTC}|_{THOT}}{R3 + R_{NTC}|_{THOT}}\right)}{\left(\frac{R3\ R_{NTC}|_{THOT}}{R3 + R_{NTC}|_{THOT}}\right) + R2} \times 100 \quad (2)$$

Where:

$$R_{NTC}|_{TCOLD} = R_O e^{\beta\left(1/T_{COLD} - 1/T_O\right)}$$

$$R_{NTC}|_{THOT} = R_O e^{\beta\left(1/T_{HOT} - 1/T_O\right)} \quad (3)$$

where, T_{COLD} and T_{HOT} are the desired temperature thresholds in degrees Kelvin. Ro is the nominal resistance and β is the temperature coefficient of the NTC resistor. An example solution for an NTC resistor with R_O = 10KΩ and β = 4500 is:

- R2 = 7.81kΩ

- R3 = 13.98kΩ

where:

- T_{COLD} = 0°C
- T_{HOT} = 60°C
- β = 4500
- R_O = 10kΩ

The plot of the percent V_{TSB} vs. temperature is shown in Figure 28:

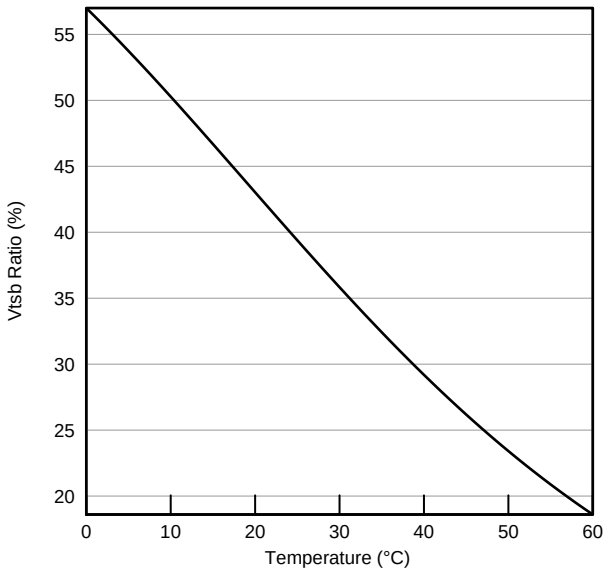


Figure 28. Example Solution for an NTC resistor with R_O = 10KΩ and β = 4500

Figure 29 illustrates the periodic biasing scheme used for measuring the TS state. The TS_READ signal enables the TS bias voltage for 24ms. During this period the TS comparators are read (each comparator has a 10 ms deglitch) and appropriate action is taken based on the temperature measurement. After this 24ms period has elapsed, the TS_READ signal goes low, which causes the TS-Bias pin to become high impedance. During the next 35ms (priority packet period) or 235ms (standard packet period), the TS voltage is monitored and compared to 100mV. If the TS voltage is greater than 100mV then a secondary device is driving the TS/CTRL pin and a CTRL = '1' is detected.

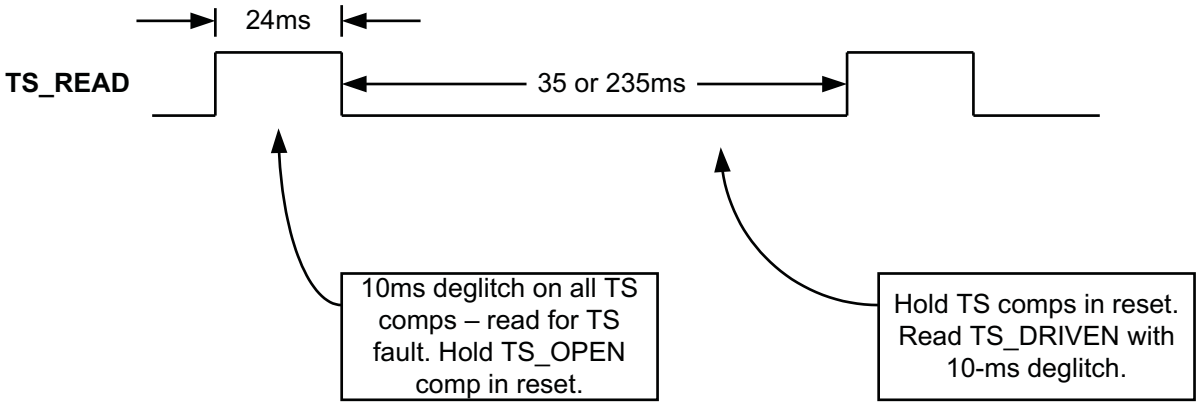


Figure 29. Timing Diagram for TS Detection Circuit

Thermal Protection

The bq5101x includes a thermal shutdown protection. If the die temperature reaches T_J(OFF), the LDO is shut off to prevent any further power dissipation.

Series and Parallel Resonant Capacitor Selection

Shown in Figure 2, the capacitors C1 (series) and C2 (parallel) make up the dual resonant circuit with the receiver coil. These two capacitors must be sized correctly per the WPC v1.0 specification. Figure 30 illustrates the equivalent circuit of the dual resonant circuit:

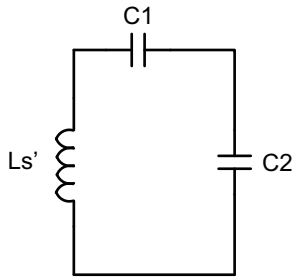


Figure 30. Dual Resonant Circuit with the Receiver Coil

Section 4.2 (Power Receiver Design Requirements) in volume 1 of the WPC v1.0 specification highlights in detail the sizing requirements. To summarize, the receiver designer will be required take inductance measurements with a fixed test fixture. The test fixture is shown in Figure 31:

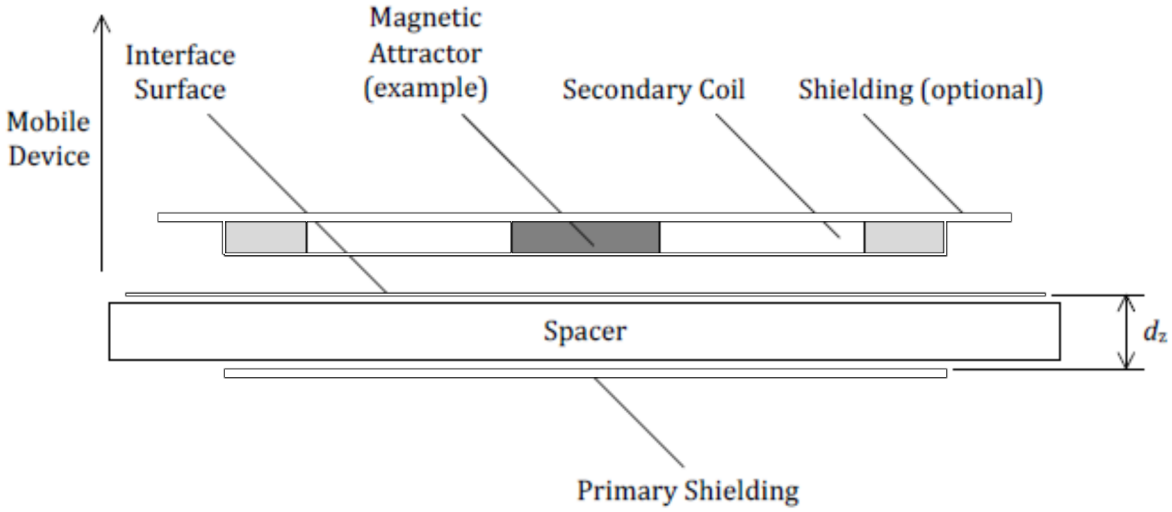


Figure 31. WPC v1.0 Receiver Coil Test Fixture for the Inductance Measurement Ls'
(copied from System Description Wireless Power Transfer, volume 1: Low Power, Part 1 Interface Definition, Version 1.0.1, Figure 4-4)

The primary shield is to be 50mm x 50mm x 1mm of Ferrite material PC44 from TDK Corp. The gap d_Z is to be 3.4mm. The receiver coil, as it will be placed in the final system (e.g. the back cover and battery must be included if the system calls for this), is to be placed on top of this surface and the inductance is to be measured at 1-V RMS and a frequency of 100 kHz. This measurement is termed Ls'. The same measurement is to be repeated without the test fixture shown in Figure 9. This measurement is termed Ls or the free-space inductance. Each capacitor can then be calculated using Equation 4:

$$C1 = \left[\left(f_S \times 2\pi \right)^2 \times L_S^{'} \right]^{-1}$$

$$C2 = \left[\left(f_D \times 2\pi \right)^2 \times L_S - \frac{1}{C1} \right]^{-1} \quad (4)$$

Where f_S is 100 kHz +5/-10% and f_D is 1 MHz ±10%. C1 must be chosen first prior to calculating C2.

The quality factor must be greater than 77 and can be determined by Equation 5:

$$Q = \frac{2\pi \times f_D \times L_S}{R} \quad (5)$$

where R is the DC resistance of the receiver coil. All other constants are defined above.

Receiver Coil Load-Line Analysis

When choosing a receiver coil, it is recommend to analyze the transformer characteristics between the primary coil and receiver coil via load-line analysis. This will capture two important conditions in the WPC system:

1. Operating point characteristics in the closed loop of the WPC system.
2. Instantaneous transient response prior to the convergence of the new operating point.

An example test configuration for conducting this analysis is shown in Figure 32:

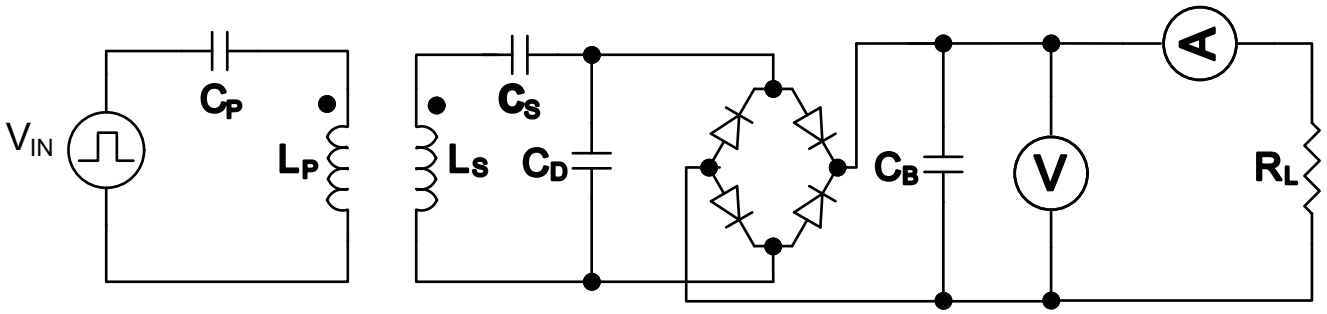


Figure 32. Load-Line Analysis Test Bench

Where:

- V_{IN} is a square-wave power source that should have a peak-to-peak operation of 19V.
- C_P is the primary series resonant capacitor (i.e. 100nF for Type A1 coil).
- L_P is the primary coil of interest (i.e. Type A1).
- L_S is the secondary coil of interest.
- C_S is the series resonant capacitor chosen for the receiver coil under test.
- C_D is the parallel resonant capacitor chosen for the receiver coil under test.
- C_B is the bulk capacitor of the diode bridge (voltage rating should be at least 25V and capacitance value of at least 10µF)
- V is a Kelvin connected voltage meter
- A is a series ammeter
- R_L is the load of interest

It is recommended that the diode bridge be constructed of Schottky diodes.

The test procedure is as follows

- Supply a 19V AC signal to L_P starting at a frequency of 210kHz
- Measure the resulting rectified voltage from no load to the expected full load
- Repeat the above steps for lower frequencies (stopping at 110kHz)

An example load-line analysis for the Vishay IWAS-4832FF-50 receiver coil is shown in Figure 33:

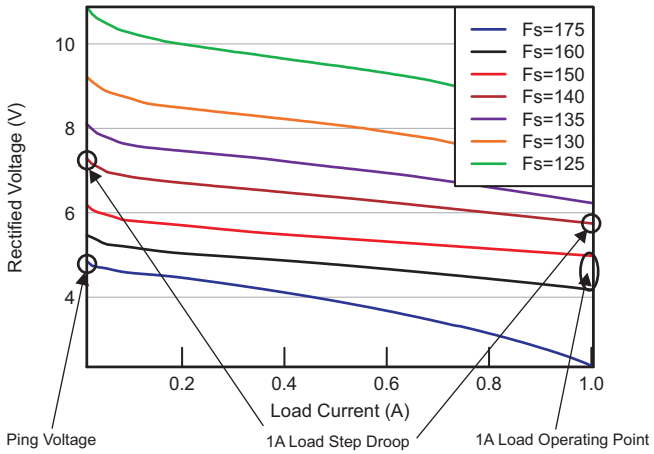


Figure 33. Vishay IWAS-4832FF-50 Load-Line Results

What this plot conveys about the operating point is that a specific load and rectifier target condition consequently results in a specific operating frequency (for the type A1 TX). For example, at 1A the dynamic rectifier target is 5.15V. Therefore, the operating frequency will be between 150kHz and 160kHz in the above example. This is an acceptable operating point. If the operating point ever falls outside the WPC frequency range (110kHz – 205kHz), the system will never converge and will become unstable.

In regards to transient analysis, there are two major points of interest:

1. Rectifier voltage at the ping frequency (175kHz).
2. Rectifier voltage droop from no load to full load at the constant operating point.

In this example, the ping voltage will be approximately 5V. This is above the UVLO of the bq5101x and; therefore, startup in the WPC system can be ensured. If the voltage is near or below the UVLO at this frequency, then startup in the WPC system may not occur.

If the max load step is 1A, the droop in this example will be approximately 1V with a voltage at 1A of approximately 5.5V (140kHz load-line). To analyze the droop locate the load-line that starts at 7V at no-load. Follow this load-line to the max load expected and take the difference between the 7V no-load voltage and the full-load voltage at that constant frequency. Ensure that the full-load voltage at this constant frequency is above 5V. If it descends below 5V, the output of the power supply will also droop to this level. This type of transient response analysis is necessary due to the slow feedback response of the WPC system. This simulates the step response prior to the WPC system adjusting the operating point.

NOTE

Coupling between the primary and secondary coils will worsen with misalignment of the secondary coil. Therefore, it is recommended to re-analyze the load-lines at multiple misalignments to determine where, in planar space, the receiver will discontinue operation.

REVISION HISTORY

Changes from Original (April 2011) to Revision A **Page**

- Added device numbers bq51010 and bq51011 1
- Added Figure 20 through Figure 23 9
- Added section - Rectifier Tracking Mode (Fold-Back) 19
- Added section - Communication Current Limit (Comm. I_{LIM} 19
- Added section - Dynamic Communication Current Limit (Dynamic I_{LIM}) 20

Changes from Revision A (May 2011) to Revision B **Page**

- Changed text in the DESCRIPTION From: Together with the bq500110 To: Together with the bq500210 1
- Changed Figure 1 1
- Changed Figure 24 14

Changes from Revision B (August 2011) to Revision C **Page**

- Deleted device number bq51010 1

Changes from Revision C (April 2012) to Revision D **Page**

- Corrected the pin number and pin name for E2 and E3. CLMP2 = E2, CLMP1 = E3 8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ51011YFFR	NRND	DSBGA	YFF	28	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51011	
BQ51011YFFT	NRND	DSBGA	YFF	28	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51011	
BQ51013YFFR	NRND	DSBGA	YFF	28	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51013	
BQ51013YFFT	NRND	DSBGA	YFF	28	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51013	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

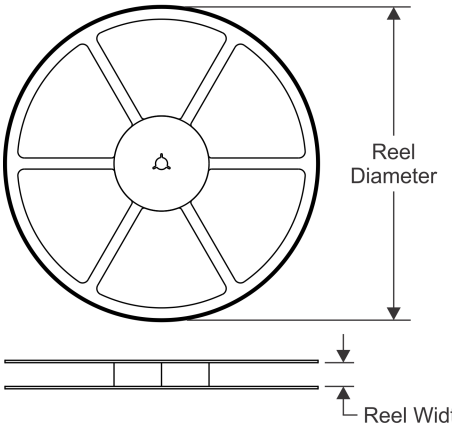
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

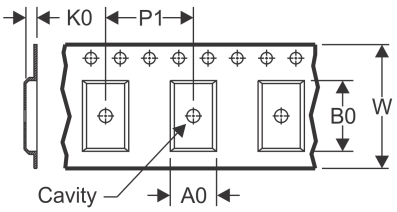
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

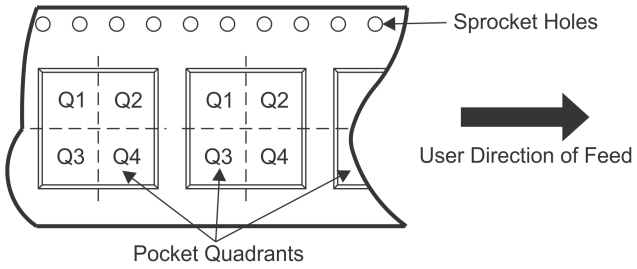


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

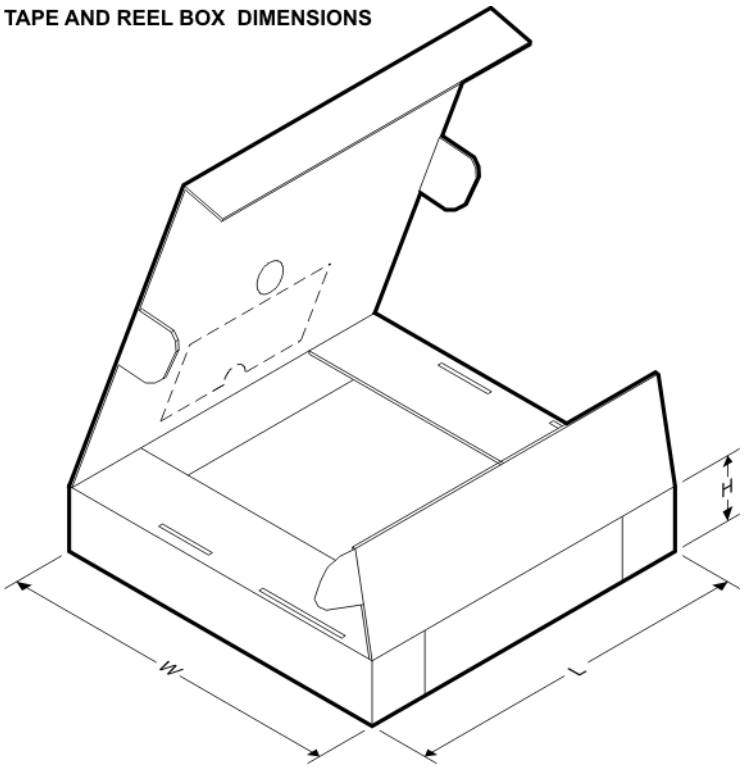
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ51011YFFR	DSBGA	YFF	28	3000	180.0	8.4	2.01	3.14	0.81	4.0	8.0	Q1
BQ51011YFFT	DSBGA	YFF	28	250	180.0	8.4	2.01	3.14	0.81	4.0	8.0	Q1
BQ51013YFFR	DSBGA	YFF	28	3000	180.0	8.4	2.01	3.14	0.81	4.0	8.0	Q1
BQ51013YFFT	DSBGA	YFF	28	250	180.0	8.4	2.01	3.14	0.81	4.0	8.0	Q1

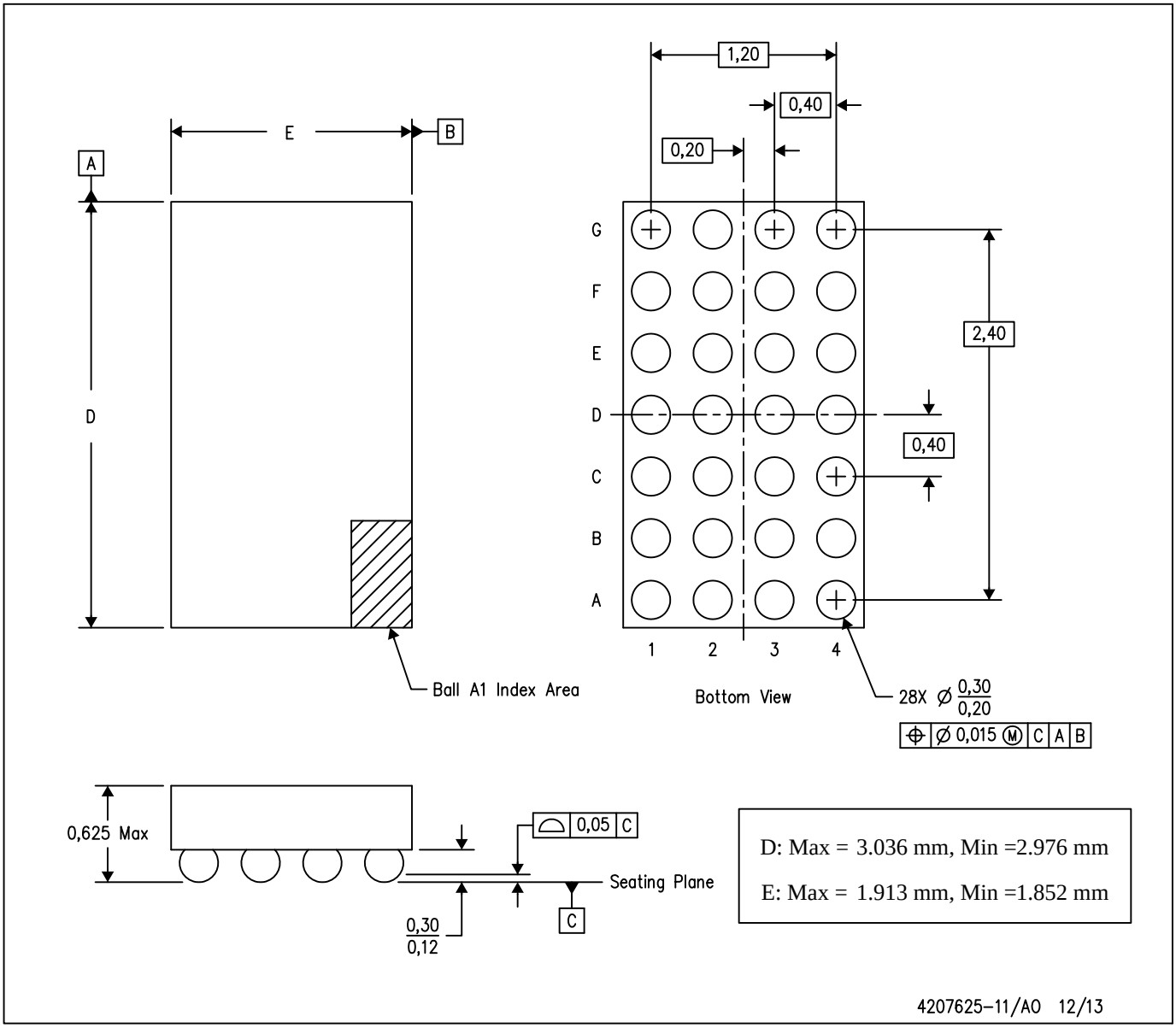
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ51011YFFR	DSBGA	YFF	28	3000	182.0	182.0	20.0
BQ51011YFFT	DSBGA	YFF	28	250	182.0	182.0	20.0
BQ51013YFFR	DSBGA	YFF	28	3000	182.0	182.0	20.0
BQ51013YFFT	DSBGA	YFF	28	250	182.0	182.0	20.0

YFF (R–XBGA–N28) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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