PD69210/PD69220

PoE PSE Controller Datasheet

Introduction

The Microchip Generation 6 family of PSE controllers include the PD69210 and PD69220 devices. The PD69210 and PD69220 have an identical feature set and differ only in physical pinout. The PD69210 and PD69220 are based on the Microchip SAM D21 family. The PD69210 or PD69220 are recommended for all new designs.

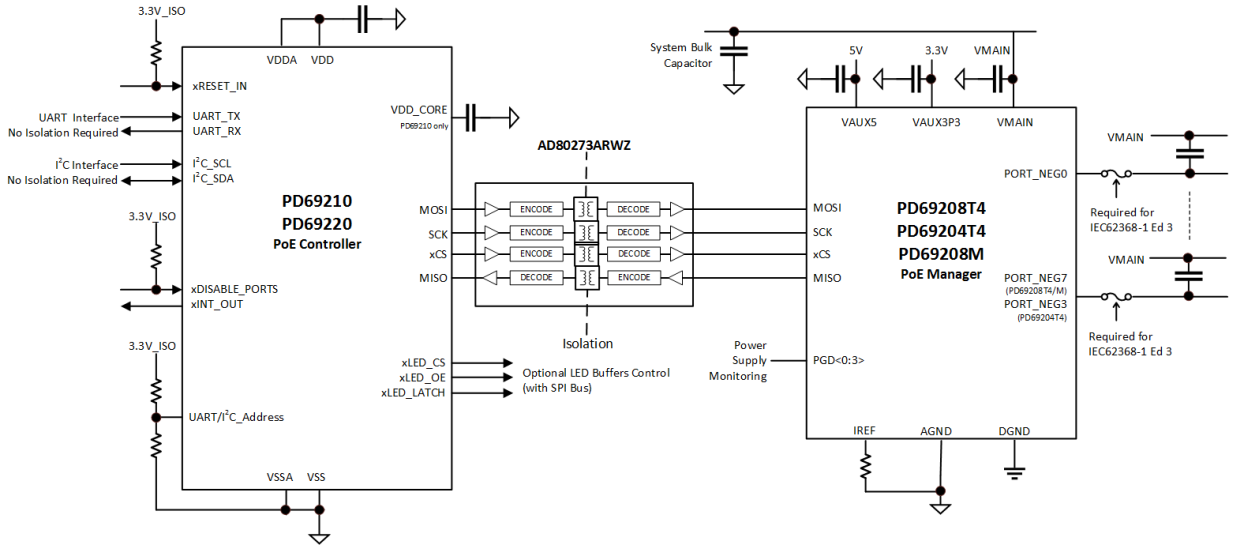
The PD69210 or PD69220 controllers when paired with the Microchip PD69208T4, PD69204T4, or PD69208M managers are part of a Power over Ethernet Power Supplying Equipment (PSE) system. This system enables designers to integrate enhanced mode PoE capabilities, as specified in IEEE 802.3af, IEEE 802.3at, IEEE 802.3bt, and PoH standards, into an Ethernet switch. The PD69210 and PD69220 will support up to 48 4-pair or 2-pair logical ports.

Both controllers are available in a 32-pin, 5 mm × 5 mm QFN package.

Typical PoE Application

The following figure shows the typical PoE application of Microchip Generation 6 devices.

Figure 1. Typical PoE Application



Consult Microchip AN3361 Designing an IEEE 802.3af/802.3at/802.3bt-Compliant PD69208 48-Port PoE System.

Features Matrix

Feature	Description	PD69210	PD69220
Support IEEE 802.3af/at		Y	Y
Support IEEE 802.3bt		Y	Y
Support HDBaseT (POH)		Y	Y
Port control matrix	Port matrix control enables to ascribe each physical port in the system to a logical port.	2p/4p	2p/4p
Logical ports	A logical port can be built from 2×physical ports or 1×physical port.	48	48
Max 2-pair power		45 W	45 W
Power management	The system supports three power management modes: Class (LLDP), Dynamic, and Static.	Per port	Per port
Power good	Used to select the system power bank to be applied to the specific PoE manager.	Y	Y
Port power limit	Configurable port power limit; when a port exceeds the limit, it is automatically disconnected.	Y	Y
Interrupt pin	Interrupt out from PoE controller indicating events such as port on, port off, port fault, PoE device fault, voltage out of range, and more.	Y	Y
Disable port pin	Shuts down all of the PoE ports in the system.	Y	Y
System OK indication	System validity indication. Provides a digital output signal to the host or to control an LED to indicate system status. When the system is OK pin state is low.	Y	Y
Legacy (reduced capacitance) detection	Enables detection and powering of pre-standard devices (PDs).	Per port	Per port
LED stream	A direct SPI interface to an external LED stream.	Y	Y
Fast PoE	Ability of a system to quickly boot and power up ports without waiting for the host setting.	Y	Y
Perpetual PoE	Ability of a PoE system to maintain PoE power while upgrading host firmware or host is in reset.	Y	Y
Communication	Communication interface with host.	I^2C or UART	I^2C or UART
Communications protocol	Compatible with previous generations controllers.	Y	Y
Pin-compatible with PD69200	Able to use on a PCB that was designed for the PD69200. For I^2C and UART programming information, see section UART or I^2C Address Selection.	N	Y
MSL1 and RoHS		Y	Y

Table of Contents

1. Architecture

The following figures show the simplified hardware architecture and firmware architecture of the PoE system based on the PD69210 and PD69220 controllers and PD69208T4, PD69204T4, and PD69208M managers.

Figure 1-1. Simplified Hardware Architecture

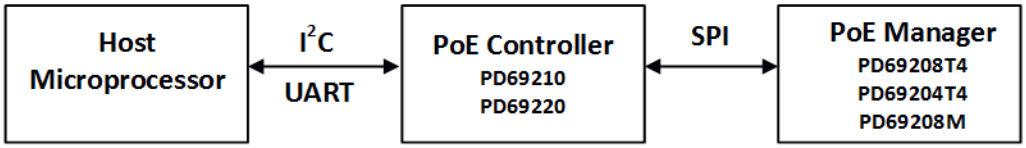
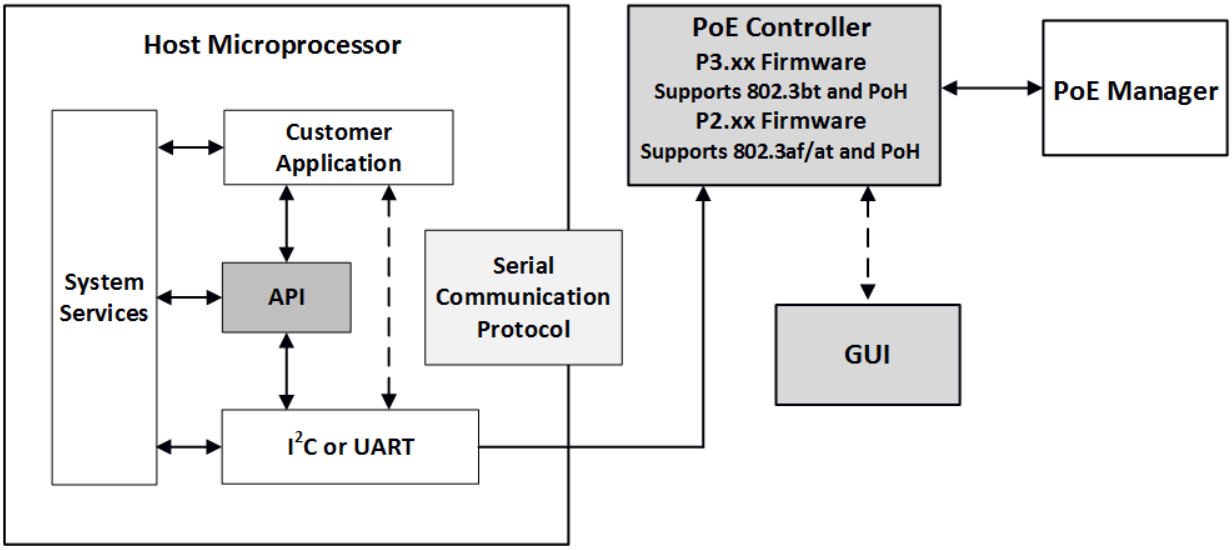


Figure 1-2. Simplified Firmware Architecture



- Dark grey boxes indicate Microchip-supplied firmware.
- Light grey boxes indicate Microchip-provided documentation.
- White boxes are user-supplied.

1.1 Firmware

- Firmware is pre-programmed in PD69210 and PD69220. Firmware version is identifiable via the IC Ordering Part Number.
- Firmware is vendor-agnostic with regards to choice of the host controller.
- May be operated standalone or with I^2C or UART communication to host.
- Default profiles are coded into the firmware. Microchip offers a Configuration Tool for profile modification.
- Firmware is field-upgradeable via the I^2C or UART link.

1.2 Communication

Communication between the host application and the controller's firmware may be done via a 15-byte protocol. Customers may use a Microchip-provided API. Microchip provides a Serial Communication Protocol Guide.

1.3 GUI

This is a diagnostic tool for control of the Microchip PSE emulating or bypassing the host processor.

1.4 Software Library

Firmware (without the boot section), GUI, and API are available on Microchip's Software Library.

1.5 SPI Communication

PD69208T4, PD69204T4, and PD69208M managers use SPI communication in SPI slave mode to communicate with the various controllers. Each manager has an address determined by ADDR0–ADDR3 pins. Each controller can support up to 12 ICs at addresses 0–11. The actual frequency between PD692x0 ICs is 1 MHz.

The following table lists the SPI communication packet structure.

Table 1-1. SPI Communication—Packet Structure

Control Byte Selects PD69208T4 According to Address	R/W Bit	Internal Register Address	Number of Words (Read Access Only)	Data Written to IC (Write Access Only) Read from IC (Read Access Only)
8 bits	R(0)/W(1)	8 bits	8 bits	16 bits

For more information about the SPI interface, see the PD69208T4, PD69204T4, and PD69208M Manager Datasheet.

1.6 UART

A pull-up resistor is required on the UART communication line. For more information, see AN3361 Designing an IEEE 802.3af/at/bt PoE System Based on PD692x0/PD69208.

UART communications configuration:

- Bits per second: 19,200 bps
- Data bits: 8
- Parity: None Stop bits: 1
- Flow control: None

1.7 I^2C

The PD692x0 requires the host to support I^2C clock stretch.

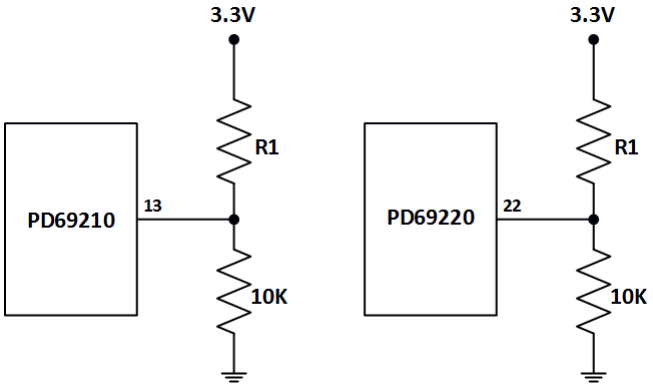
I^2C communication configuration:

- Address: 7 bits
- Clock stretch: Host should support
- Transaction: 15 bytes or 1 byte

1.8 UART or I²C Address Selection

The choice of UART or I²C interface between the host CPU is made by applying a specific voltage level to pin #13 (I2C_ADDR_MEAS) on the PD69210, or by applying a specific voltage level to pin #22 (I2C_ADDR_MEAS) on the PD69220. Additionally, the specific I²C address is also set by this voltage level. In all cases, the voltage is set via an external resistor divider as shown in the following figure.

Figure 1-3. I²C Address Selection



The specific Value of R to choose UART or I²C and to set the address is given in the following tables for PD69210 and PD69220.

Table 1-2. I²C Address Selection

I2C Address (Hexadecimal)	R1- KΩ (1%)
UART	N.C.
0x4	147
0x8	86.6
0xC	57.6
0x10	43.2
0x14	34
0x18	26.7
0x1C	22.1
0x20	18.2
0x24	15.4
0x28	13
0x2C	11
0x30	9.31
0x34	7.87
0x38	6.49
0x3C	5.49

2. Electrical Specifications

The following sections describe the electrical specifications for the PD69210 and PD69220 devices.

2.1 Electrical Characteristics

For a complete list of electrical characteristics, see Microchip SAM21 Family Datasheet.

Table 2-1. General Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power supply voltage		3.0	3.3	3.63	V
V_{DDA}	Power supply voltage		3.0	3.3	3.63	V
T_A	Temperature range		–40	25	85	°C
T_J	Junction temperature				100	°C

2.2 Immunity

Table 2-2. Immunity

Symbol	Parameter	Conditions	Min	Max	Units
ESD	ESD rating	HBM[1]	–2000	+2000	V
		CDM[2]	–500	+500	V

1. ESD HBM complies with JESD22 Class 2 standard.
2. ESD CDM complies with JESD22 Class 1 standard.

2.3 Absolute Maximum Ratings

Stresses beyond those listed in this section may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2-3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Power supply voltage	0	3.8	V
V_{PIN}	Pin voltage with respect to GND and VDD	GND – 0.6 V	VDD + 0.6 V	V
Lead soldering temperature (40 s, reflow)			260	°C
Storage temperature		–60	150	°C

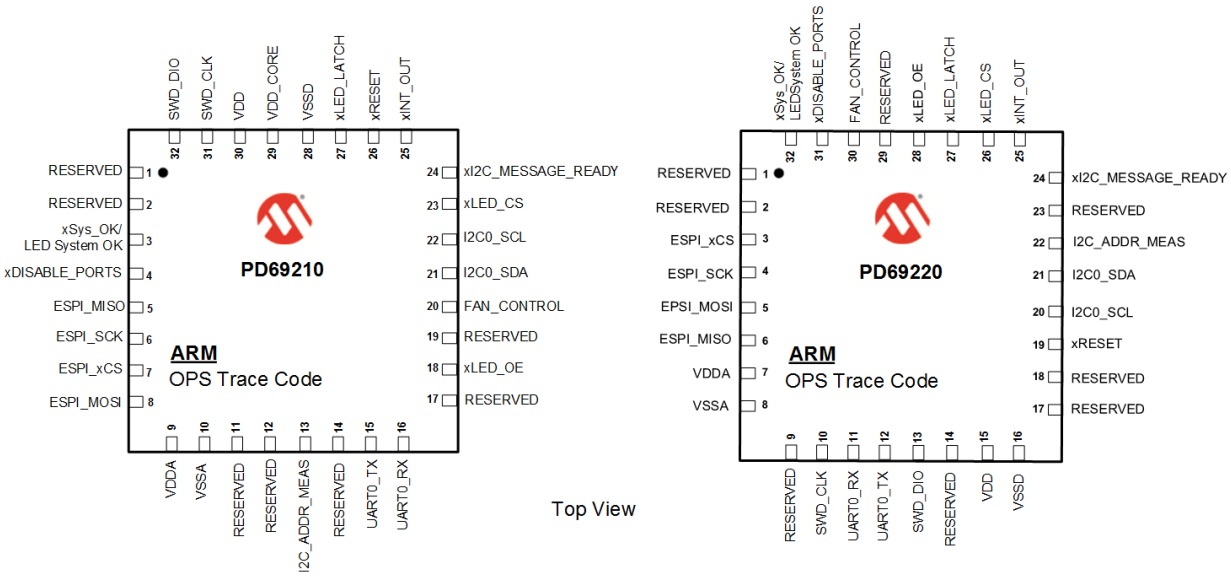
3. Pins

The PD69210 and PD69220 controller each has 32 pins, which are described in this section.

3.1 Pin Diagrams

The following figures represent the top view of PD69210 and PD69220 devices.

Figure 3-1. PD69210 and PD69220 Pin Diagram



Note: For definitions about markings in the pinout diagram, see Ordering Information.

3.2 Pin Descriptions

The following table describes the functional pin descriptions of the PD69210 and PD69220 devices.

Table 3-1. Pin Descriptions

PD69210 Pin	PD69220 Pin	Designation	Type	Description
1	1	Reserved	OUT	Reserved UART. Leave open.
2	2	Reserved	IN	Reserved UART. Pull up to 3.3 V via 10 kΩ.
3	32	xSys_OK/LED System OK	OUT	System validity indication. The behavior of this output is controlled by individual software mask. (Active Low)
4	31	xDISABLE_PORTS	IN	Disable all PoE ports. When this input is asserted low, the controller shuts down all PoE ports in the system. See AN3361 for pin connection requirements. (Active Low)
5	6	ESPI_MISO	IN	ESPI bus to PoE manager. SPI master in, slave out. SPI packets are received on this line.

.....continued

PD69210 Pin	PD69220 Pin	Designation	Type	Description
6	4	ESPI_SCK	OUT	ESPI bus to PoE manager. SPI clock output to PD6920x, and LED stream clock output, set to 1 MHz.
7	3	ESPI_xCS	OUT	ESPI bus to PoE manager. SPI chip select. Pull-up required. See AN3361 for pin connection requirements. (Active Low)
8	5	ESPI_MOSI	OUT	ESPI bus from PoE manager. SPI master out, slave in. SPI packets are received on this line.
9	7	VDDA	Supply	Main Supply 3.3 V.
10	8	VSSA	GND	Ground.
11	14	Reserved	Analog_IN	Reserved Analog_IN. Connect to 3.3 V or GND through 10 kΩ.
-	9, 29	Reserved	Analog_IN	Reserved Analog_IN. Connect to 3.3 V.
12, 19	-	Reserved		Reserved. Leave open.
13	22	I2C_ADDR_MEAS	Analog_IN	Analog input to determine I^2C address or UART operation.
14	23	Reserved		Connect to GND.
15	12	UART0_TX	OUT	UART transmit to host. 15-byte protocol reply/ telemetry is transmitted on this line. The baud rate is set to 19,200 bps.
16	11	UART0_RX	IN	UART receive from a host. 15-byte protocol commands are received on this line. The baud rate is set to 19,200 bps. Pull-up is required. See AN3361 for details.
17	18	Reserved	Oscillator	Reserved. Oscillator output. Leave open.
	17	Reserved	Oscillator	Reserved. Oscillator output. Leave open.
18	28	xLED_OE	OUT	Output enable signal for the LED stream. (Active Low)
20	30	FAN_CONTROL	OUT	Logic out that may be used to control a fan driver. (Active High)
21	21	I2C0_SDA	IN/OUT	I^2C bidirectional data. 15-byte protocol messages are transmitted on this line. Pull-up required, see AN3361 for details.
22	20	I2C0_SCL	IN/OUT	I^2C clock from the host master. Speed is limited to 400 KHz. Clock stretch required. Pull-up required, see AN3361 for details.
23	26	xLED_CS	OUT	Chip select signal for LED stream. (Active Low)

.....continued

PD69210 Pin	PD69220 Pin	Designation	Type	Description
24	24	xI2C_MESSAGE_READY	OUT	I^2C message ready for reading by the host. Controller asserts this line low when it has an answer to the host. Therefore, the host can poll this line and initiate I^2C read cycle only when the message is ready. After the host reads the data from the controller, this pin is asserted to high. (Active Low)
25	25	xINT_OUT	OUT	Interrupt output indication. This line is asserted low when a pre-configured event is in progress. (Active Low)
26	19	xRESET	IN/OUT	Host Reset input (Active Low). Controller can generate self-reset. In this case, the xRESET pin is driven low by the controller for 100 µs. See AN3361 for pin connection requirements.
27	27	xLED_LATCH[2]	OUT	Latch signal for LED stream. (Active Low)
28	16	VSSD	GND	Ground.
29	-	VDD_CORE	Power	1.2 V core voltage connect 1 µF capacitor to VSSD.
30	15	VDD	Supply	Main 3.3 V supply.
31	10	SWD_CLK		PD69210 use a 1 kΩ pull-up to 3.3 V. PD69220 leave open or use 1k pull-up.
32	13	SWD_DIO		Leave open.
ePAD	ePAD	ePAD		Connect to VSSA. Must have sufficient copper mass to ensure adequate thermal performance.

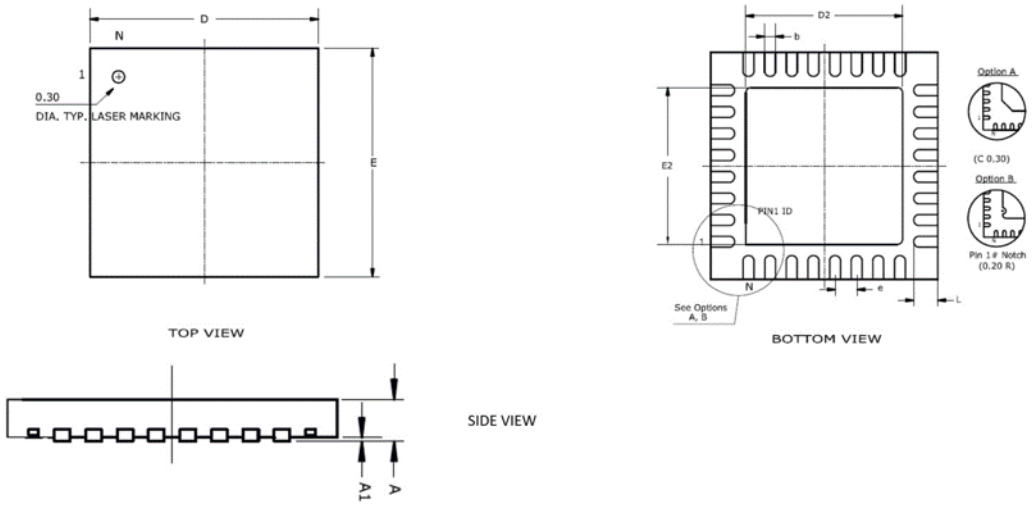
4. Package Information

This section provides the package information for the PD69210 and PD69220 devices.

4.1 PD69210 Package Outline Drawing

The following figure shows the package drawing of PD69210 device.

Figure 4-1. PD69210 Package Outline Drawing (32 Pin QFN 5 mm × 5 mm)



The following table lists the dimensions and measurements of the PD69210 package.

Table 4-1. PD69210 Package Outline Dimensions and Measurements

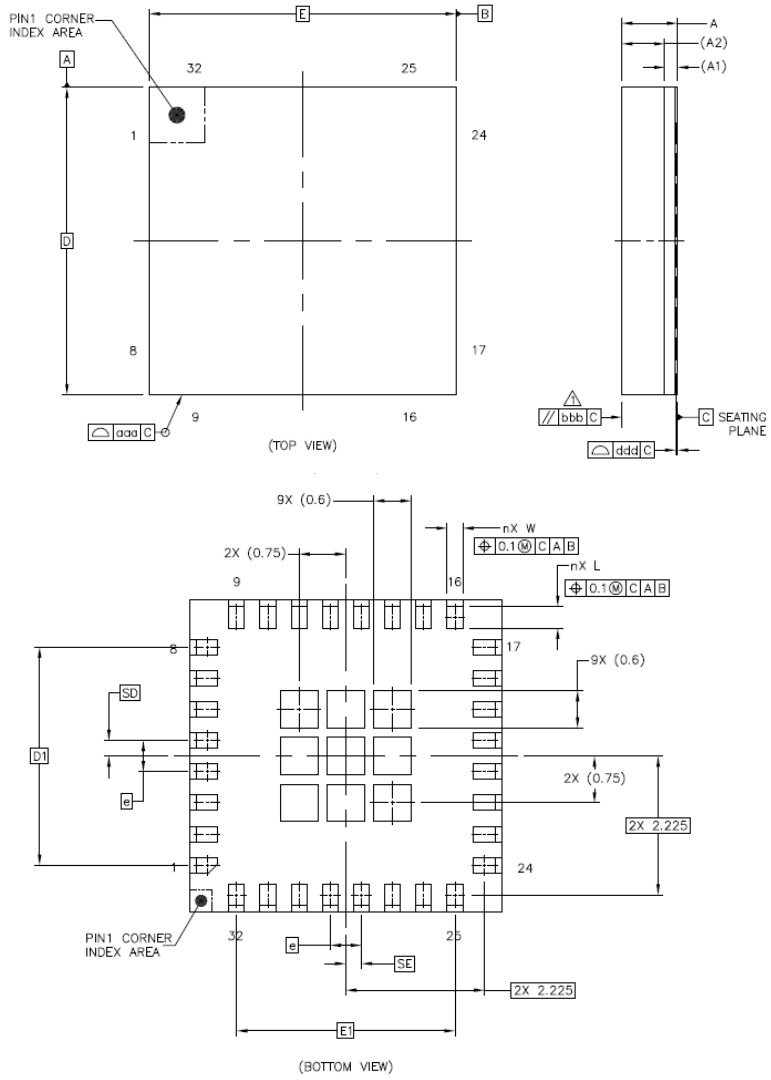
Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	3.50	3.70	0.138	0.147
E2	3.50	3.70	0.138	0.147
D	5.00 BSC		0.197 BSC	
E	5.00 BSC		0.197 BSC	

Note: Dimensions do not include protrusions; they should not exceed 0.155 mm (0.006 in.) on any side. Lead dimension should not include solder coverage. Dimensions are in millimeters and inches for reference.

4.2 PD69220 Package Outline Drawing

The following figure shows the package outline drawing of the PD69220 device.

Figure 4-2. PD69220 Package Outline Drawing (32-Pin LGA 5 mm × 5 mm)



The following table lists the dimensions and measurements of the PD69220 package.

Table 4-2. PD69220 Package Outline Dimensions and Measurements

Dimension	Millimeters		
	Min	Typ	Max
A			1
A1		0.21	
A2		0.7	
D		5	
E		5	

.....continued			
Dimension	**Millimeters**		
	Min	**Typ**	**Max**
W	0.2	0.25	0.3
L	0.30	0.35	0.4
e		0.5	
n		32	
D1		3.5	
E1		3.5	
SD		0.25	
SE		0.25	

4.3 Thermal Specifications

The following table lists the thermal specifications of the PD69210 and PD69220.

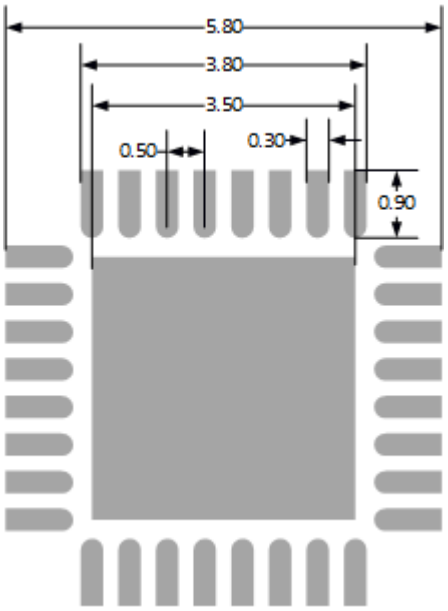
Table 4-3. Thermal Specifications

Thermal Resistance	Device	Typ	Units	Description
θ_{JA}	PD69210	40.9	°C/W	Junction-to-ambient thermal resistance.
θ_{JC}	PD69210	15.2	°C/W	Junction-to-case thermal resistance.
θ_{JA}	PD69220	65.0	°C/W	Junction-to-ambient thermal resistance.
θ_{JC}	PD69220	21.5	°C/W	Junction-to-case thermal resistance.

4.4 Recommended PCB Layout

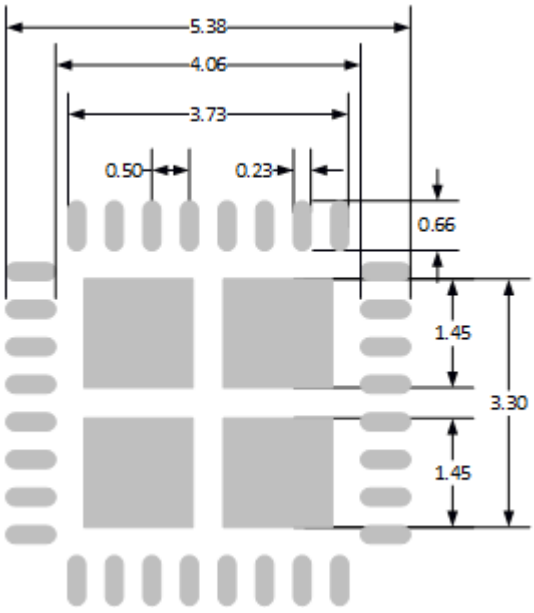
The following figures show the recommended PCB layout pattern for the 32-pin QFN 5 mm × 5 mm PD69210 and for the 32-pin LGA 5 mm × 5 mm PD69220. Units are in mm.

Figure 4-3. PD69210 and PD69220 Top-Layer Copper PCB Layout



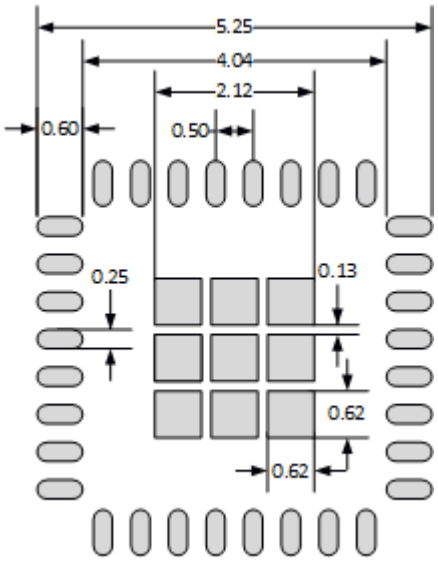
The recommended solder paste stencil for the PD69220 is different than the recommended stencil for PD69200.

Figure 4-4. PD69210 Top-Layer Solder Paste and Vias PCB Layout for Thermal Pad Array



Note: The contract manufacturer has latitude to modify the solder paste stencil for manufacturability reasons. The solder paste stencil covers 65% to 80% of the thermal pad and must not allow solder to be applied to the thermal vias under the QFN package using any method they deem appropriate. Any design should be subject to system validation and qualification prior to commitment to mass production of field deployment. Use a 5 mil stencil.

Figure 4-5. PD69220 Top-Layer Solder Paste and Vias PCB Layout for Thermal Pad Array



Note: The contract manufacturer has latitude to modify the solder paste stencil for manufacturability reasons. The solder paste stencil covers 65% to 80% of the thermal pad and must not allow solder to be applied to the thermal vias under the QFN package using any method they deem appropriate. Any design should be subject to system validation and qualification prior to commitment to mass production of field deployment. Use a 5 mil stencil.

The PD69220 may be used on a PCB that was designed for the PD69200, that is the top layer copper for the two devices is identical. However, the recommended solder paste stencil for the PD69220 is different than the recommended stencil for PD69200. The recommended solder paste stencil for the PD69200 is identical to the PD69210 as shown in figure PD69210 Top-Layer Solder Paste and Vias PCB Layout for Thermal Pad Array. For more information, see the PD69200 Datasheet.

4.5 Recommended Solder Reflow Information

RoHS 6/6

Pb-free 100% Matte Tin Finish

Package Peak Temperature for Solder Reflow (40 s maximum exposure)—260 °C (0 °C, –5 °C)

Table 4-4. Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (TS_{max} to Tp)	3 °C/second max	3 °C/second max
Preheat		
Temperature min (TS_{min})	100 °C	150 °C
Temperature max (TS_{max})	150 °C	200 °C
Time (ts_{min} to ts_{max})	60 s to 120 s	60 s to 180 s
Time Maintained		
Temperature (T_L)	183 °C	217 °C
Time (t_L)	60 s to 150 s	60 s to 150 s
Peak classification temperature (TP)	210 °C to 235 °C	240 °C to 255 °C

.....continued		
Profile Feature	**Sn-Pb Eutectic Assembly**	**Pb-Free Assembly**
Time within 5 °C of actual peak temperature (tp)	10 s to 30 s	20 s to 40 s
Ramp-down rate	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max

Figure 4-6. Classification Reflow Profiles

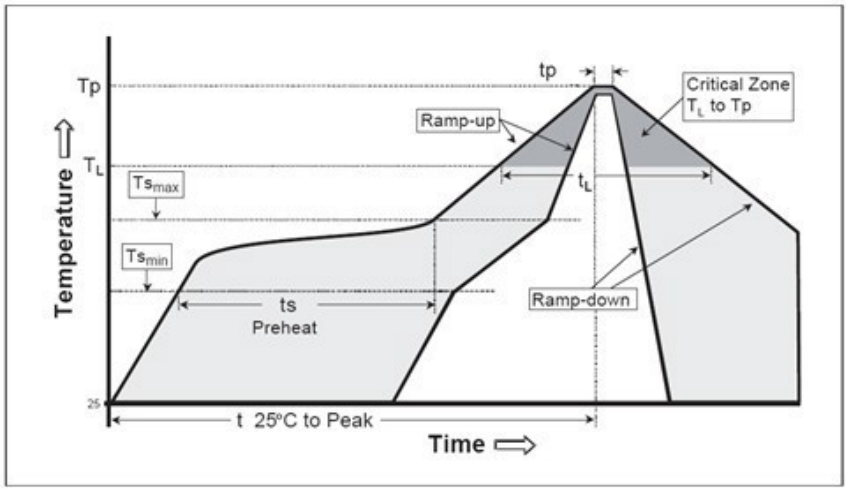


Table 4-5. Pb-Free Process—Package Classification Reflow Temperatures

Package Thickness	Volume <350 mm^3	Volume 350–2000 mm^3	Volume >2000 mm^3
Less than 1.6 mm[1]	260 + 0 °C	260 + 0 °C	260 + 0 °C
1.6 mm to 2.5 mm[1]	260 + 0 °C	250 + 0 °C	245 + 0 °C
Greater than or equal to 2.5 mm[1]	250 + 0 °C	245 + 0 °C	245 + 0 °C

1. Tolerance: The device manufacturer or supplier should assure process compatibility up to and including the stated classification temperature, meaning that the Peak reflow temperature is +0 °C. For example, 260 °C to 0 °C, at the rated MSL value.

Note: Exceeding the ratings that are mentioned in the preceding table might cause damage to the device.

4.6 Reference Documents

- IEEE Std 802.3-2018 Clause 33 Power over Ethernet over 2-Pair and Clause 145 Power over Ethernet
- PD69210 Communication Protocol User Guide
- AN3361 Designing an IEEE 802.3af/at/bt PoE System Based on PD692x0/PD69208.
- PD69208T4, PD69204T4, and PD69208M PoE PSE Manager Datasheet
- PD69200 PoE PSE Controller Datasheet

5. Ordering Information

The following table lists the part ordering information for PD69210 and PD69220 devices.

Table 5-1. Ordering Information

Part Number	Package	Packaging Type	Temperature	Part Marking	Tray Marking
PD69210D[1]VVVV[2]SS[3]	Plastic QFN 5 mm × 5 mm (32 lead)	Tray	–40 °C to 85 °C	Microchip Logo PD69210 ARM Logo YY[4] WW[5] NNN[6]	PD69210D-VVVVSS PD-OOOOGabb[7] YYWW
PD69210D[1]VVVV[2]SS[3]-TR	Plastic QFN 5 mm × 5 mm (32 lead)	Tape and reel	–40 °C to 85 °C	Microchip Logo PD69210 ARM Logo YY[4] WW[5] NNN[6]	
PD69220D[1]VVVV[2]SS[3]	Plastic QFN Laminated[8] 5 mm × 5 mm (32 lead)	Tray	–40 °C to 85 °C	Microchip Logo PD69220 ARM Logo YY[4] WW[5] NNN[6]	PD69220D-VVVVSS PD-OOOOGabb[7] YYWW
PD69220D[1]VVVV[2]SS[3]-TR	Plastic QFN Laminated[8] 5 mm × 5 mm (32 lead)	Tape and reel	–40 °C to 85 °C	Microchip Logo PD69220 ARM Logo YY[4] WW[5] NNN[6]	

1. D is detection method.
   - C= IEEE 802.3 and pre-standard
   - R= IEEE 802.3 only
2. VVVV is firmware revision.
3. SS is firmware parameters options.
4. Year code (last two digits of calendar year).
5. Week code (week of January 1 is week 01).
6. Alphanumeric trace code.
7. Operational part number.
8. Laminated QFN is also called a Land Grid Array (LGA).

The firmware release note has all required information about how to specify the choice of VVVV and SS. Find the Firmware Release Notes in the Microchip Software Libraries, and register to My Microchip account to access the release notes.

Note: The package meets RoHS, Pb-free of the European Council to minimize the environmental impact of electrical equipment.

Note: Initial burning of controller's firmware is performed in the factory. Firmware upgrades can be performed by users using the communication interface. For more information, see TN-140 (Catalog Number: 06-0024-081).

6. Revision History

Revision	Date	Section	Description
A	03/2020		This is the initial issue of this document. The PD69220 PoE PSE controller is a new product offering and has not been previously described in any other document. The PD69210 PoE PSE controller was previously described in the following documents: • PD69208T4 and PD69210 Datasheet (Revision 3 September 2019 Document Number PD-000357193) • PD69204T4 and PD69210 Datasheet (Revision 3 September 2019 Document Number PD-000359832) • PD69208M and PD69210 Datasheet (Revision 3 September 2019 Document Number PD-000359833)

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