FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00025-0v01-E

Memory FRAM

4 M (256 K × 16) Bit

MB85RE4M2T

■ DESCRIPTIONS

The MB85RE4M2T is an FRAM (Ferroelectric Random Access Memory) chip consisting of 262,144 words × 16 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MB85RE4M2T is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85RE4M2T can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E2PROM. The MB85RE4M2T uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM. The MB85RE4M2T provides a RESET function which initializes all data in FRAM memory array to “0”.

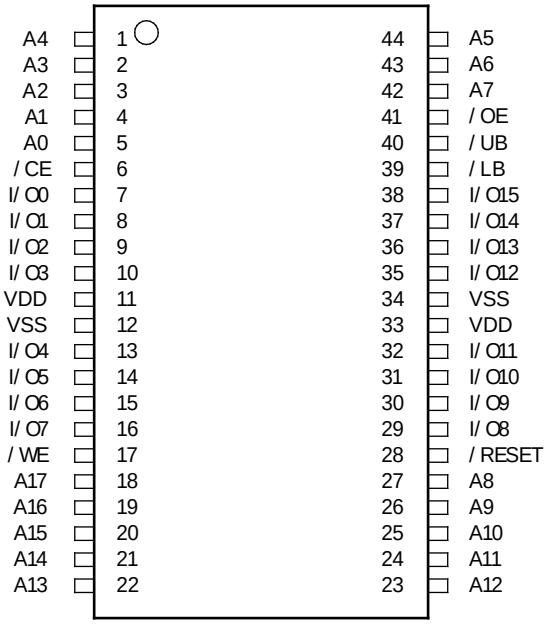
■ FEATURES

- Bit configuration : 262,144 words × 16 bits
- LB and UB data byte control : Available Configuration of 524,288 words × 8 bits
- Read/write endurance : 10^{13} times / 16 bits
- Data retention : 10 years (+ 85 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low power operation : Operating power supply current 20 mA (Max)
  Standby current 150 μA (Max)
- Operation ambient temperature range : − 40 °C to + 85 °C
- Package : 44-pin plastic TSOP (FPT-44P-M34)
  RoHS compliant

2013.11

■ PIN ASSIGNMENTS

(TOP VIEW)

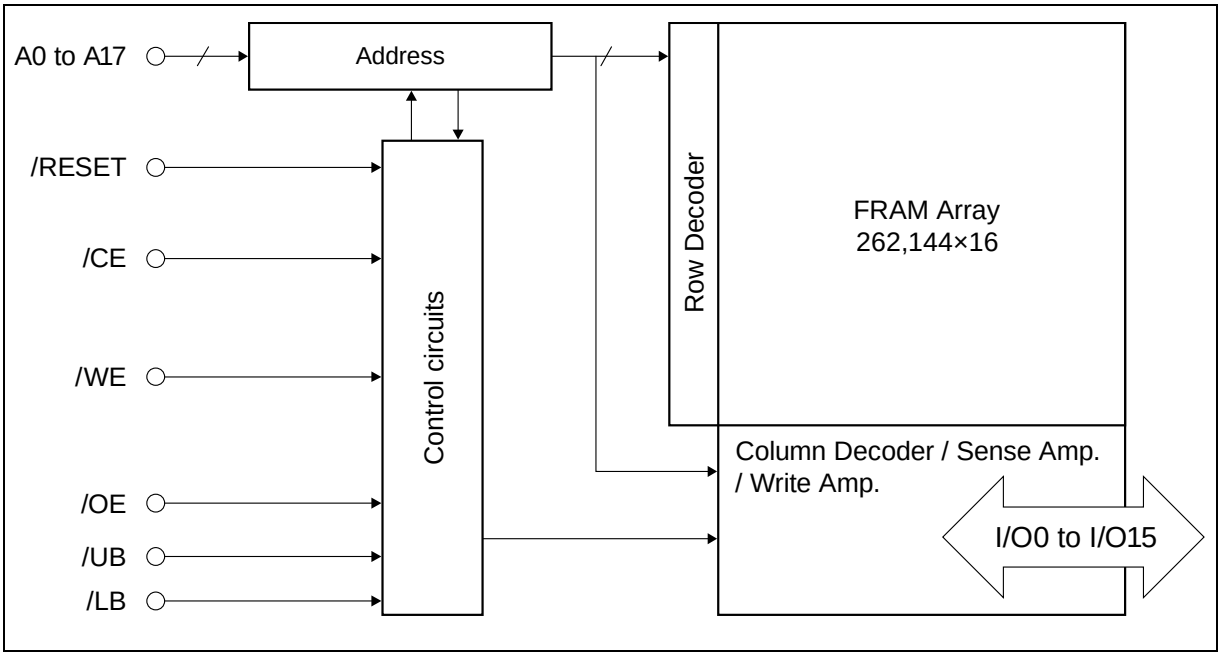


FPT - 44P - M34

■ PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 5, 18 to 22, 23 to 27, 42 to 44	A0 to A17	Address Input pins Select 262,144 words in FRAM memory array by 18 Address Input pins. When these address inputs are changed during /CE equals to “L” level, reading operation of data selected in the address after transition will start.
7 to 10, 13 to 16, 29 to 32, 35 to 38	I/O0 to I/O15	Data Input/Output pins These are 16 bits bidirectional pins for reading and writing.
6	/CE	Chip Enable Input pin In case the /CE equals to “L” level and /RESET equals to “H” level, device is activated and enables to start memory access. In writing operation, input data from I/O pins are latched at the rising edge of /CE and written to FRAM memory array.
17	/WE	Write Enable Input pin Writing operation starts at the falling edge of /WE. Input data from I/O pins are latched at the rising edge of /WE and written to FRAM memory array.
41	/OE	Output Enable Input pin When the /OE is “L” level, valid data are output to data bus. When the /OE is “H” level, all I/O pins become high impedance (High-Z) state.
28	/RESET	Reset Mode Input pin When the /RESET becomes to “L” level, all data in FRAM memory array are initialized to “0” through a RESET mode. During reading and writing operation, /RESET pin shall be hold “H” level.
39, 40	/LB, /UB	Lower/Upper byte Control Input pins In case /LB or /UB equals to “L” level, it enables reading/writing operation of I/O0 to I/O7 or I/O8 to I/O15 respectively. In case /LB and /UB equal to “H” level, all I/O pins become High-Z state.
11, 33	VDD	Supply Voltage pins Connect all two pins to the power supply.
12, 34	VSS	Ground pins Connect all two pins to ground.

■ BLOCK DIAGRAM



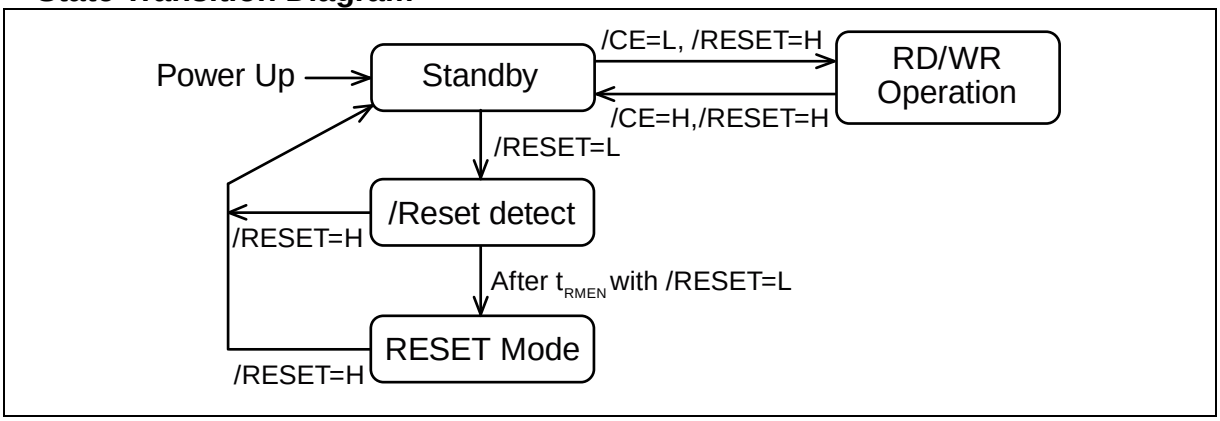
■ FUNCTIONAL TRUTH TABLE

Operation Mode	/CE	/WE	/OE	A0 to A17	/RESET
Reset	×	×	×	×	L
Standby	H	×	×	×	H
Read	↓	H	L	H or L	H
Address Access Read	L	H	L	↑ or ↓	H
Write(/CE Control)*1	↓	L	×	H or L	H
Write(/WE Control)*1*2	L	↓	×	H or L	H
Address Access Write*1*3	L	↓	×	↑ or ↓	H
Pre-charge	↑	×	×	×	H

Note: H= “H” level, L= “L” level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑

*1: In writing cycle, input data is latched at early rising edge of /CE or /WE.
*2: In writing sequence of /WE control, there exists time with data output of reading cycle at the falling edge of /CE.
*3: In writing sequence of Address Access Write, there exists time with data output of reading cycle at the address transition.

■ State Transition Diagram



■ FUNCTIONAL TRUTH TABLE OF BYTE CONTROL

Operation Mode	/WE	/OE	/LB	/UB	I/O0 to I/O7	I/O8 to I/O15
Read(Without Output)	H	H	×	×	Hi-Z	Hi-Z
	H	×	H	H	Hi-Z	Hi-Z
Read(I/O8 to I/O15)	H	L	H	L	Hi-Z	Output
Read(I/O0 to I/O7)			L	H	Output	Hi-Z
Read(I/O0 to I/O15)			L	L	Output	Output
Write(I/O8 to I/O15)	↑	×	H	L	×	Input
Write(I/O0 to I/O7)			L	H	Input	×
Write(I/O0 to I/O15)			L	L	Input	Input

Note: H= “H” level, L= “L” level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑
Hi-Z= High Impedance

In case the byte reading or writing are not selected, /LB and /UB pins shall be connected to GND pin.

■ ABABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V_{DD}	− 0.5	+ 4.0	V
Input Pin Voltage*	V_{IN}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Output Pin Voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Operation Ambient Temperature	T_A	− 40	+ 85	°C
Storage Temperature	Tstg	− 55	+ 125	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage*	V_{DD}	1.8	3.3	3.6	V
High Level Input Voltage*	V_{IH}	V_{DD} × 0.8	—	V_{DD} + 0.3	V
Low Level Input Voltage*	V_{IL}	− 0.3	—	V_{DD} × 0.2	V
Operation Ambient Temperature	T_A	− 40	—	+ 85	°C

*: All voltages are referenced to VSS (ground 0 V).

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = 0V to V_{DD}	—	—	5	µA
Output Leakage Current	$\|I_{LO}\|$	V_{OUT} = 0V to V_{DD} /CE = V_{IH} or /OE = V_{IH}	—	—	5	µA
Operating Power Supply Current*1	I_{DD}	/CE = 0.2 V, I_{out} = 0 mA	—	TBD	20	mA
Standby Current	I_{SB}	/RESET ≥ V_{DD} − 0.2V /CE, /WE, /OE ≥ V_{DD} − 0.2V /LB, /UB ≥ V_{DD} − 0.2V Others ≥ V_{DD} − 0.2V or ≤ 0.2V	—	TBD	150	µA
Reset Current	I_{RR}	/RESET = V_{SS} /CE, /WE, /OE ≥ V_{DD} − 0.2V /LB, /UB ≥ V_{DD} − 0.2V Others ≥ V_{DD} − 0.2V or ≤ 0.2V	—	TBD	20	mA
High Level Output Voltage	V_{OH1}	V_{DD} = 2.7V to 3.6V I_{OH} = − 1.0mA	V_{DD} × 0.8	—	—	V
	V_{OH2}	V_{DD} = 1.8V to 2.7V I_{OH} = − 100µA	V_{DD} − 0.2	—	—	
Low Level Output Voltage	V_{OL1}	V_{DD} = 2.7V to 3.6V I_{OL} = 2.0mA	—	—	0.4	V
	V_{OL2}	V_{DD} = 1.8V to 2.7V I_{OL} = 150µA	—	—	0.2	

*1: During the measurement of I_{DD}, all Address and I/O were taken to only change once per active cycle.
Iout : output current

2. AC Characteristics

▪ AC Test Conditions

Power Supply Voltage : 1.8 V to 3.6 V
Operation Ambient Temperature : − 40 °C to + 85 °C
Input Voltage Amplitude : 0 V to V_{DD}
Input Rising Time : 3 ns
Input Falling Time : 3 ns
Input Evaluation Level : $V_{DD}/2$
Output Evaluation Level : $V_{DD}/2$
Output Load Capacitance : 30 pF

(1) Read Cycle

Parameter	Symbol	Value (V_{DD}=1.8V to 2.7V)		Value (V_{DD}=2.7V to 3.6V)		Unit
		Min	Max	Min	Max	
Read Cycle time	t_{RC}	TBD	—	150	—	ns
/CE Access Time	t_{CE}	—	TBD	—	75	ns
Address Access Time	t_{AA}	—	TBD	—	150	ns
/OE Output Data Hold time	t_{OH}	0	—	0	—	ns
Output Data Hold time	t_{OAH}	20	—	20	—	ns
/CE Active Time	t_{CA}	TBD	—	75	—	ns
Pre-charge Time	t_{PC}	TBD	—	75	—	ns
/LB, /UB Access Time	t_{BA}	—	TBD	—	20	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Hold Time	t_{AH}	TBD	—	75	—	ns
/OE Access Time	t_{OE}	—	TBD	—	20	ns
/CE Output Floating Time	t_{HZ}	—	TBD	—	10	ns
/OE Output Floating Time	t_{OHZ}	—	TBD	—	10	ns
/LB, /UB Output Floating Time	t_{BHZ}	—	TBD	—	10	ns
Address Transition Time	t_{AX}	—	TBD	—	10	ns

(2) Write Cycle

Parameter	Symbol	Value (V_{DD}=1.8V to 2.7V)		Value (V_{DD}=2.7V to 3.6V)		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	TBD	—	150	—	ns
/CE Active Time	t_{CA}	TBD	—	75	—	ns
/CE↓ to /WE↑ Time	t_{CW}	TBD	—	75	—	ns
Pre-charge Time	t_{PC}	TBD	—	75	—	ns
Write Pulse Width	t_{WP}	20	—	20	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Hold Time	t_{AH}	TBD	—	75	—	ns
/WE↓ to /CE↑ Time	t_{WLC}	TBD	—	25	—	ns
/UB↓ or /LB↓ to /CE↑ Time	t_{BLC}	TBD	—	25	—	ns
Address Transition to /WE↑ Time	t_{AWH}	TBD	—	150	—	ns
/WE↑ to Address Transition Time	t_{WHA}	0	—	0	—	ns
/LB, /UB Setup Time	t_{BS}	2	—	2	—	ns
/LB, /UB Hold Time	t_{BH}	0	—	0	—	ns
Data Setup Time	t_{DS}	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
/WE Output Floating Time	t_{WZ}	—	TBD	—	10	ns
/WE Output Access Time[*1]	t_{WX}	10	—	10	—	ns
Write Setup Time[*1]	t_{WS}	0	—	0	—	ns
Write Hold Time[*1]	t_{WH}	0	—	0	—	ns

*1: Writing operation applies “Write Cycle Timing 1” or “Write Cycle Timing 2” by the relation of /CE and /WE timing. The values of t_{WX}, t_{WS} and t_{WH} are defined by these operations. The conditions of t_{WS} and t_{WH} are not checked at shipping test.

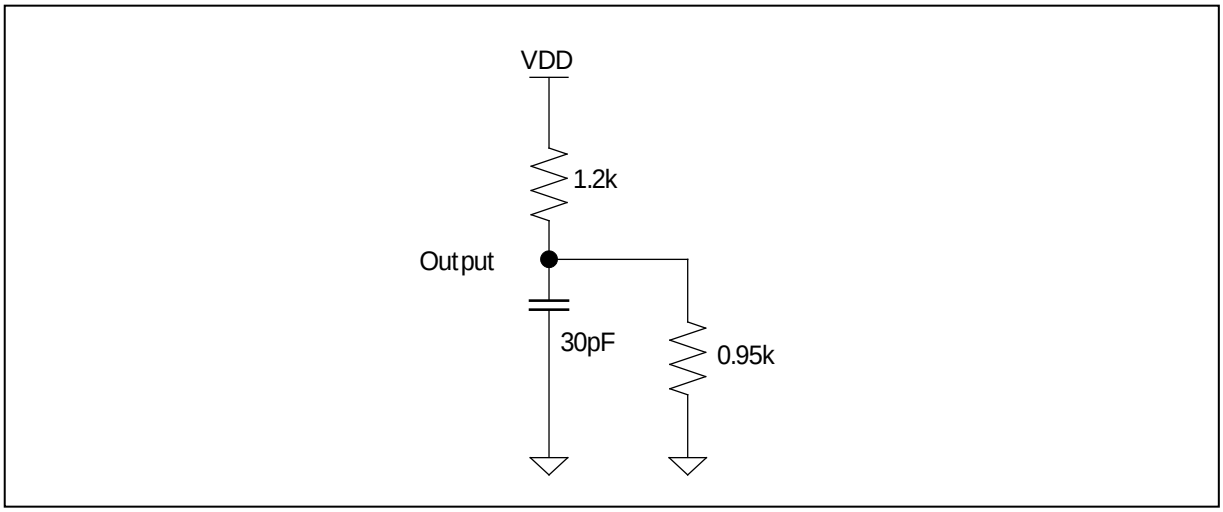
(3) Power ON/OFF Sequence and Reset Cycle

Parameter	Symbol	Value		Unit
		Min	Max	
/CE level hold time for Power ON	t_{PU}	450	—	µs
/CE level hold time for Power OFF	t_{PD}	85	—	ns
Power supply rising time	t_{VR}	50	—	µs/V
Power supply falling time	t_{VF}	100	—	µs/V
Reset mode enable time	t_{RMEN}	100	—	ms
Reset mode time	t_{RMRT}	700	—	ms
Reset mode release time	t_{RMEX}	300	—	µs

3. Pin Capacitance

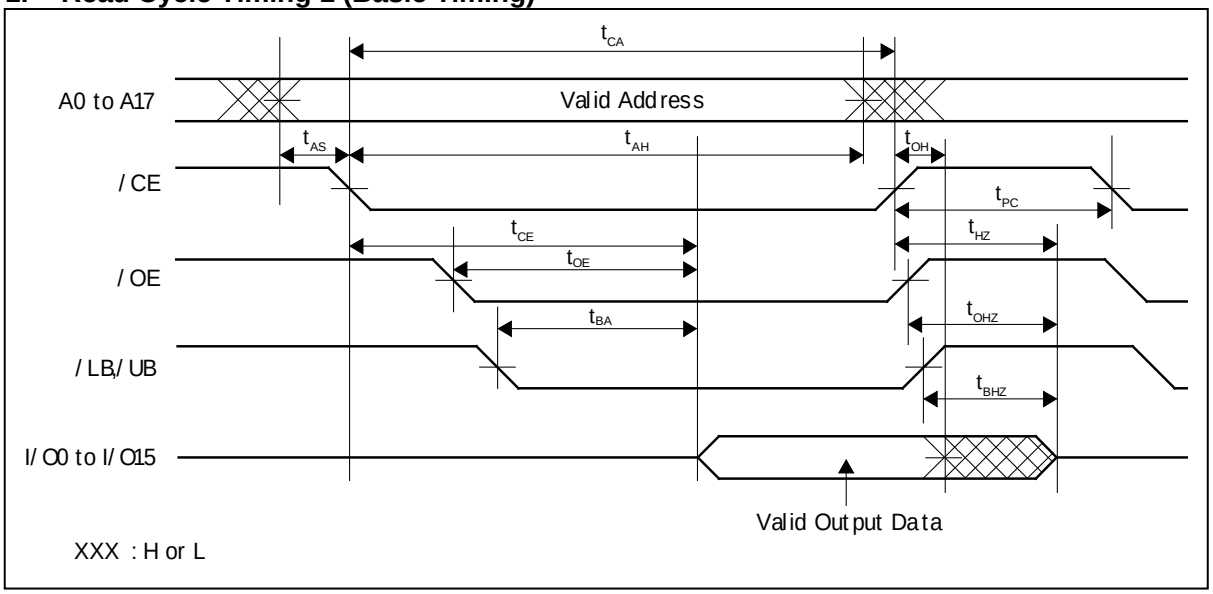
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	V_{DD} = 3.3 V, f = 1 MHz, T_A = + 25 °C	—	—	6	pF
Input/Output Capacitance (I/O pin)	$C_{I/O}$		—	—	8	pF
/RESET Pin Input Capacitance	C_{RR}		—	—	8	pF

■ AC Test Load Circuit

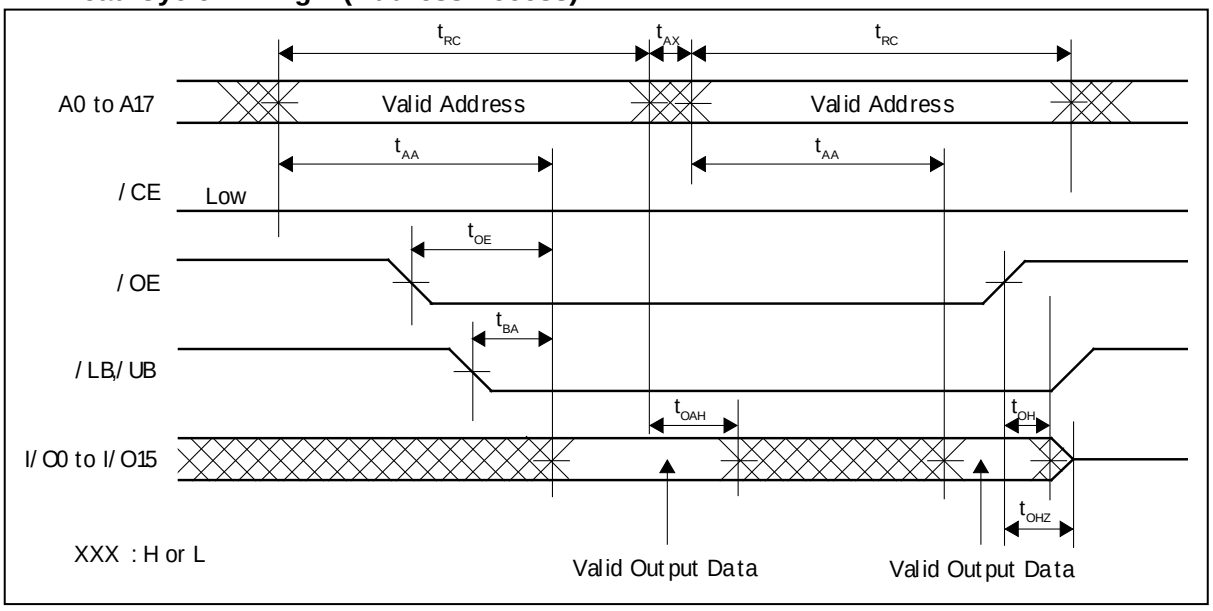


■ TIMING DIAGRAMS

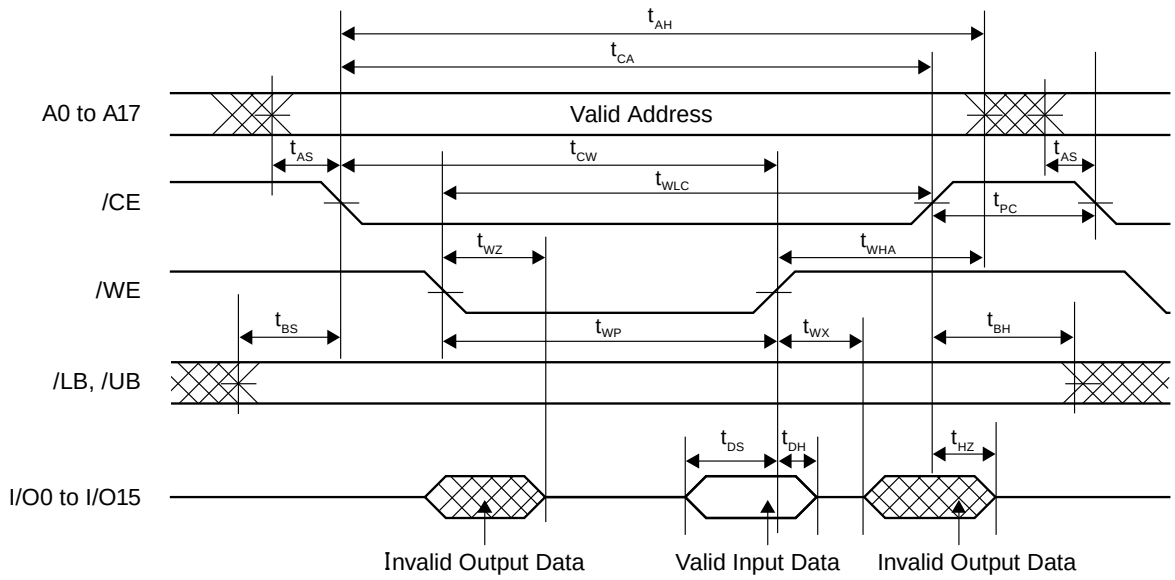
1. Read Cycle Timing 1 (Basic Timing)



2. Read Cycle Timing 2 (Address Access)



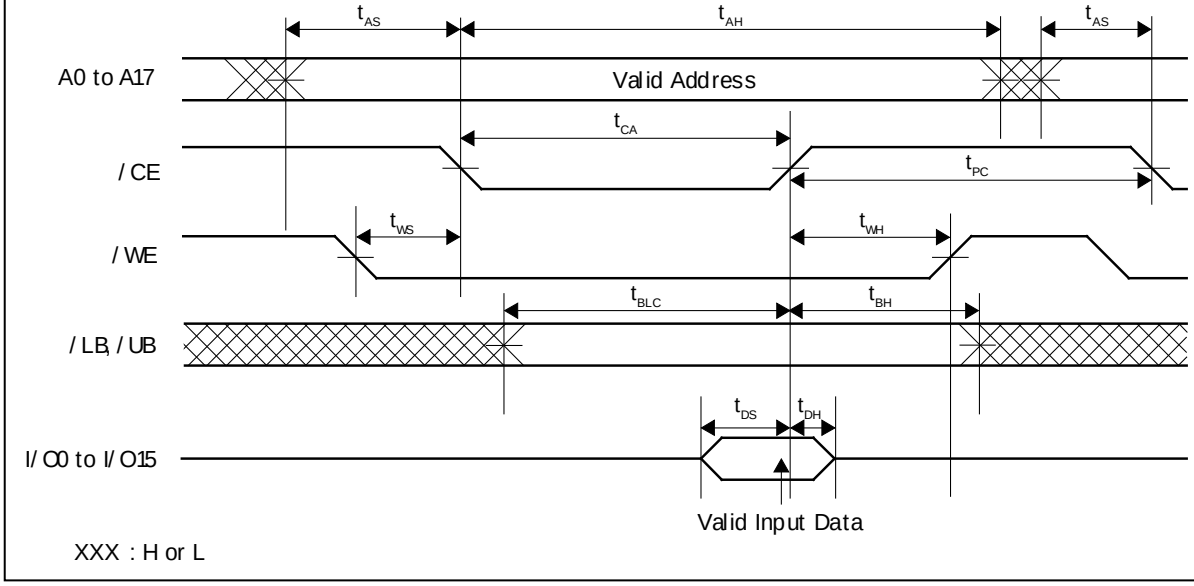
3. Write Cycle Timing 1 (/WE Control)



XXX : H or L

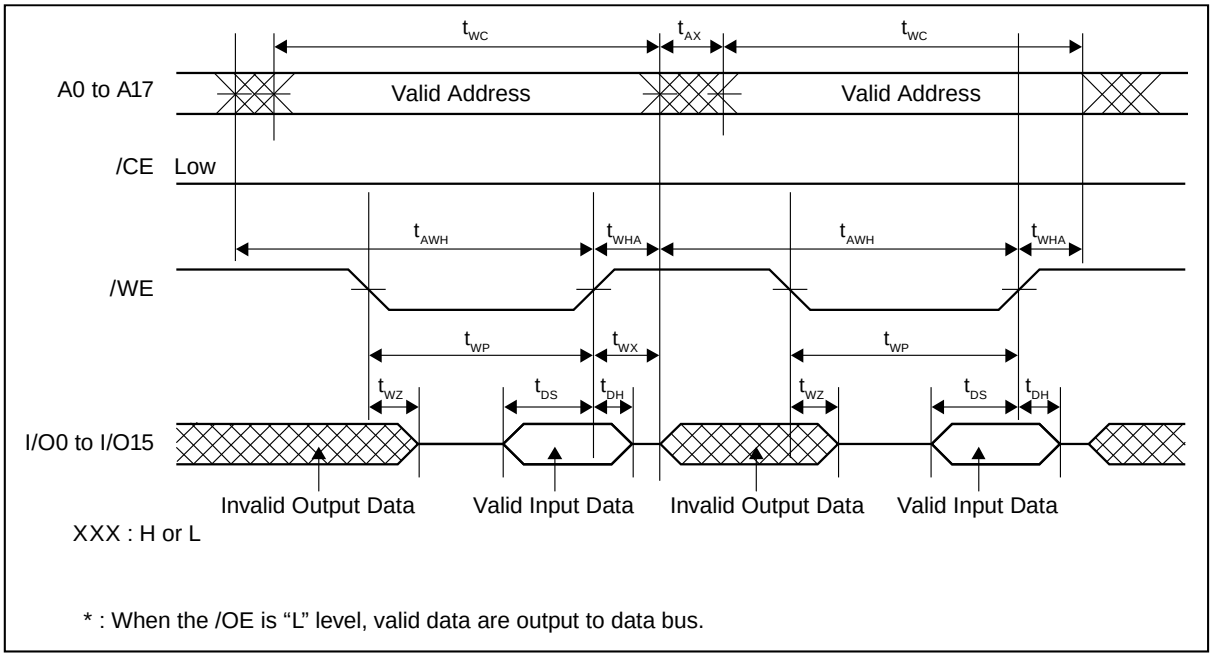
* : When the /OE is “L” level, valid data are output to data bus.

4. Write Cycle Timing 2 (/CE Control)



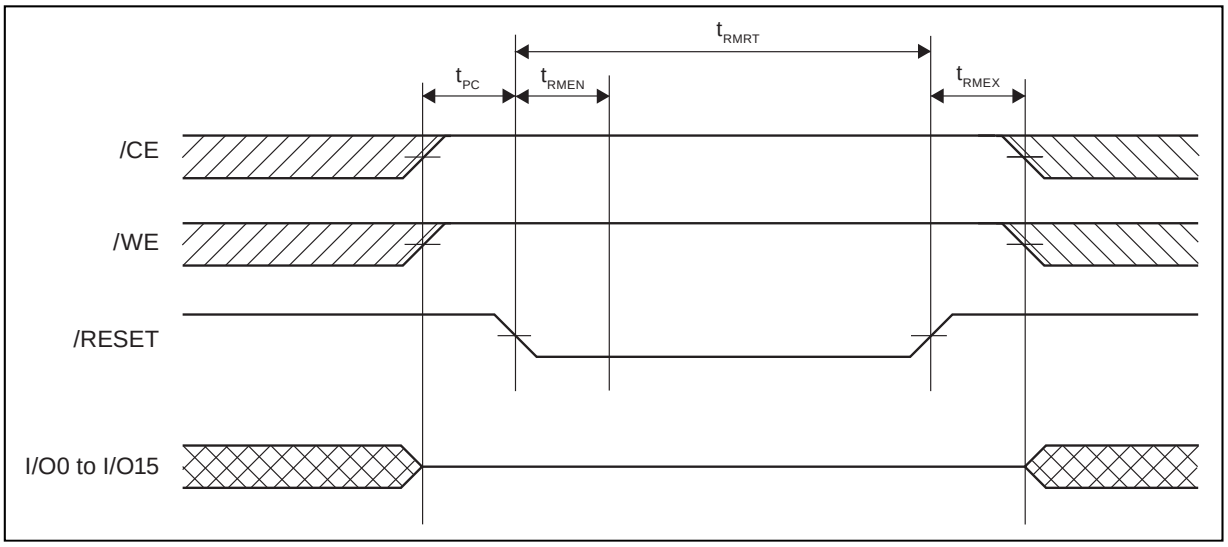
XXX : H or L

5. Write Cycle Timing 3 (Address Access and /WE Control)

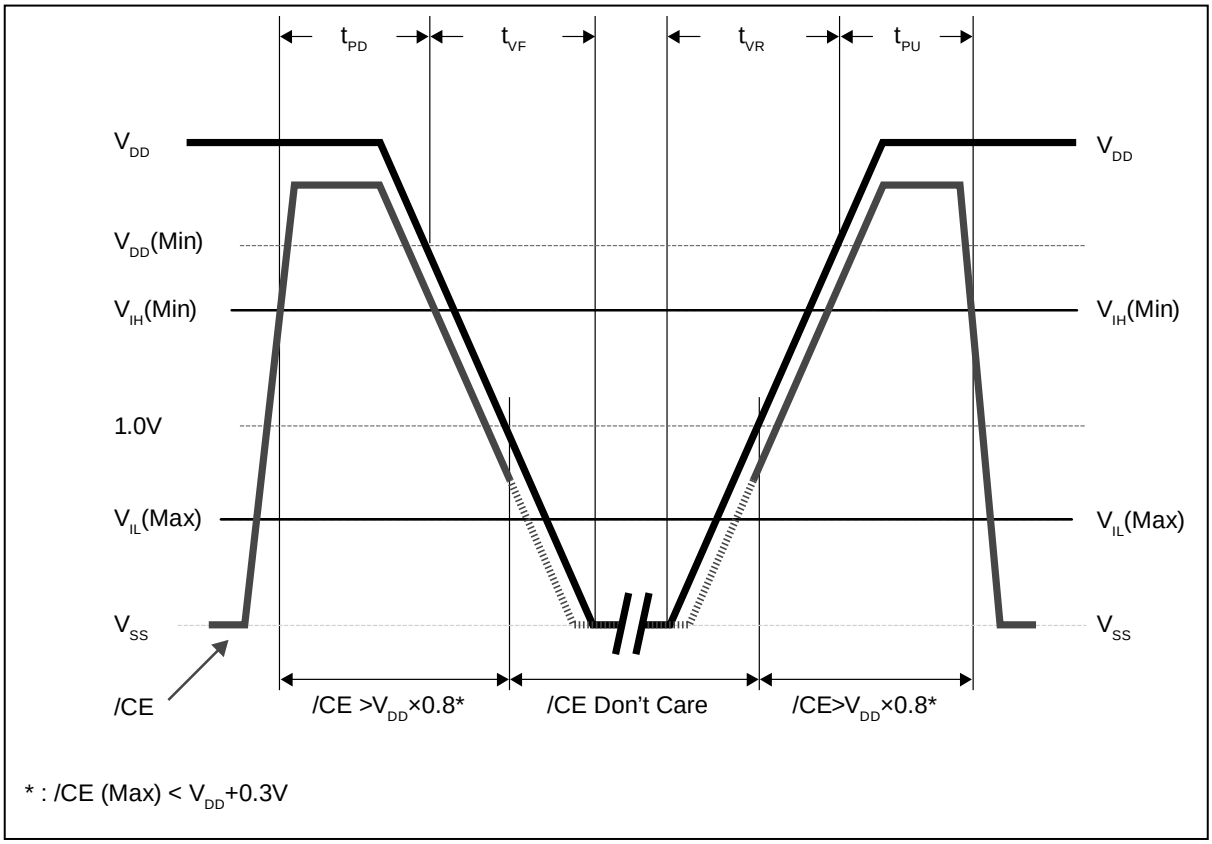


* : When the /OE is “L” level, valid data are output to data bus.

6. Reset Timing



■ POWER ON/OFF SEQUENCE



* : /CE (Max) < V_{DD}+0.3V

■ NOTES ON USE

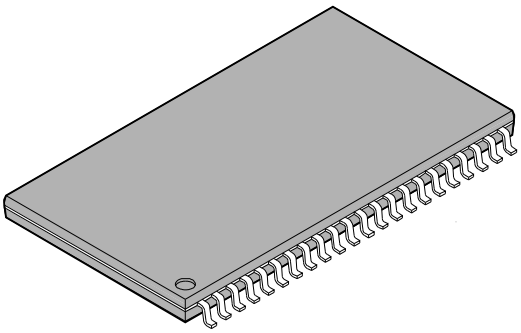
- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.
- VDD pin is required to be rising from 0 V because turning the power on from an intermediate level may cause malfunctions, when the power is turned on.

■ ORDERING INFORMATION

Part Number	Package	Shipping form	Minimum shipping quantity
MB85RE4M2TFN-G-ASE1	44-pin plastic TSOP (FPT-44P-M34)	Tray	—*

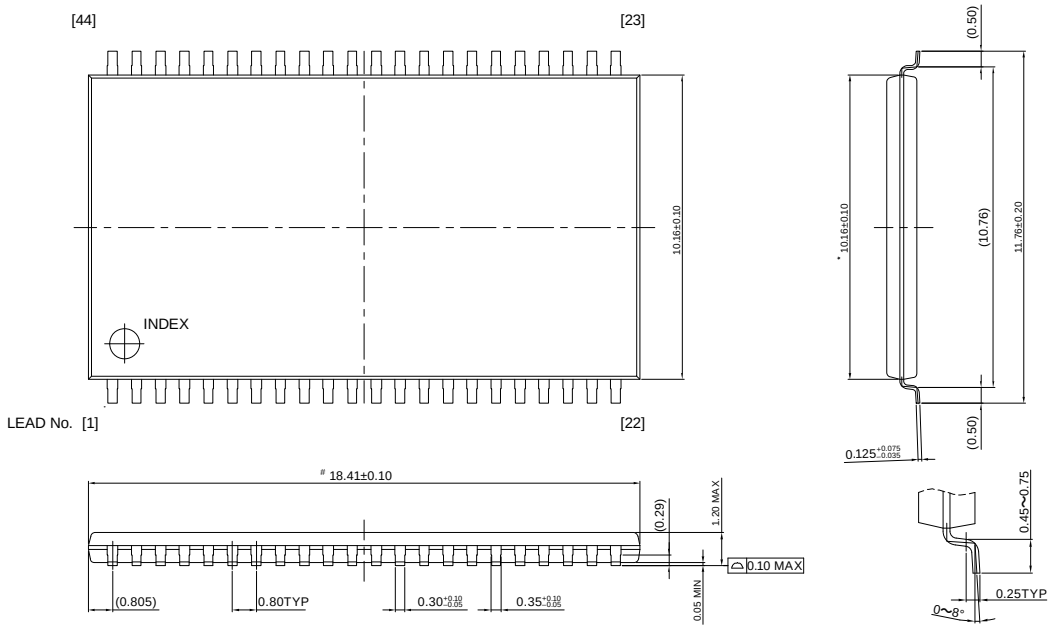
*: Please contact our sales office about minimum shipping quantity.

■ PACKAGE DIMENSIONS

44-pin plastic TSOP		
 (FPT-44P-M34)	Lead pitch	0.8mm
	Package width × package length	10.16 × 18.41mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.2mm
	Weight	TBD

44-pin plastic TSOP
(FPT-44P-M34)

Note 1) # : Resin protrusion.(Each side:+0.15 Max).
Note 2) * : These dimensions do not include resin protrusion.
Note3)Pins width and pins thickness include plating thickness.
Note4)Pins width do not include tie bar cutting remainder.



Dimensions in mm.
Note : The values in parentheses are reference values.

MEMO

MEMO

MEMO

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
902 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://www.fujitsu.com/kr/fsk/

Asia Pacific
FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
30F, Kerry Parkside, 1155 Fang Dian Road,
Pudong District, Shanghai 201204, China
Tel : +86-21-6146-3688 Fax : +86-21-6146-3660
http://cn.fujitsu.com/fss/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
2/F, Green 18 Building, Hong Kong Science Park,
Shatin, N.T., Hong Kong
Tel : +852-2736-3232 Fax : +852-2314-4207
http://cn.fujitsu.com/fsp/

Edited: Corporate Planning Department