Keywords: binary sensor, one-time programming (OTP), 1-Wire

APPLICATION NOTE 5778

MAX14832 CUSTOMER OTP GUIDE

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Abstract: This document is an introduction to the OTP procedure and timing information for the slave device MAX14832 with the 1-Wire® interface, including details on 1-Wire signaling, setup, and protocol, as well as the OTP configuration.

Introduction

This document is an introduction to the one-time programming (OTP) procedure and timing information for the MAX14832 with the 1-Wire® interface.

The register map for the device can be found on the MAX14832 data sheet.

1-Wire product data sheets, together with application notes, design guides, and tutorials can be found on the Maxim website.

Note that the MAX14832 is not fully 1-Wire compliant and supports only standard (15.4kbps) communication.

1-Wire Signaling

The 1-Wire protocol relies on the 1-Wire master for timing in all data transactions. The master initiates timing on a bit by pulling the 1-Wire bus low. Whenever a falling edge occurs, a clock begins counting on the 1-Wire bus and sampling for reads, writes, and other data transactions is based on particular clock intervals.

A normal 1-Wire write from the master begins with a falling edge. If the value to be written is logic 1, the master pulls the bus low then releases the bus within 15µs, allowing the pullup to return the bus to its idle-high state. The slave device (MAX14832) then samples the bus voltage between 15µs and 60µs after the initial falling edge (**Figure 1**). If logic 0 is to be written, the master pulls the bus low for at least 60µs then releases the bus. The MAX14832 samples the bus voltage between 15µs and 60µs (**Figure 2**).

In the case of a 1-Wire read, the master again initiates by pulling the bus low, then releasing it. If the bit being read contains logic 1, the MAX14832 leaves the bus in its idle-high state and the bus voltage is sampled 15µs after the initial falling edge (**Figure 3**). If the bit being read contains logic 0, the MAX14832 holds the line down for at least 15µs and the bus voltage is sampled 15µs after the initial falling edge (**Figure 4**).

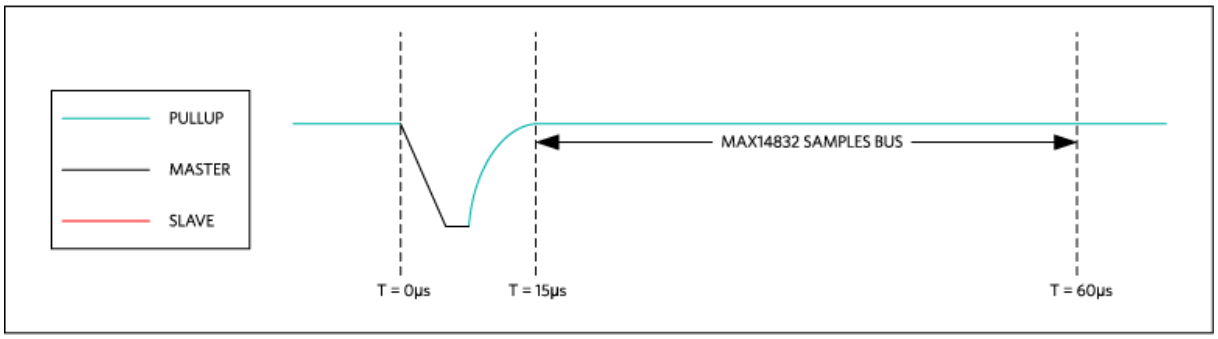

Figure 1. 1-Wire write: Logic 1.

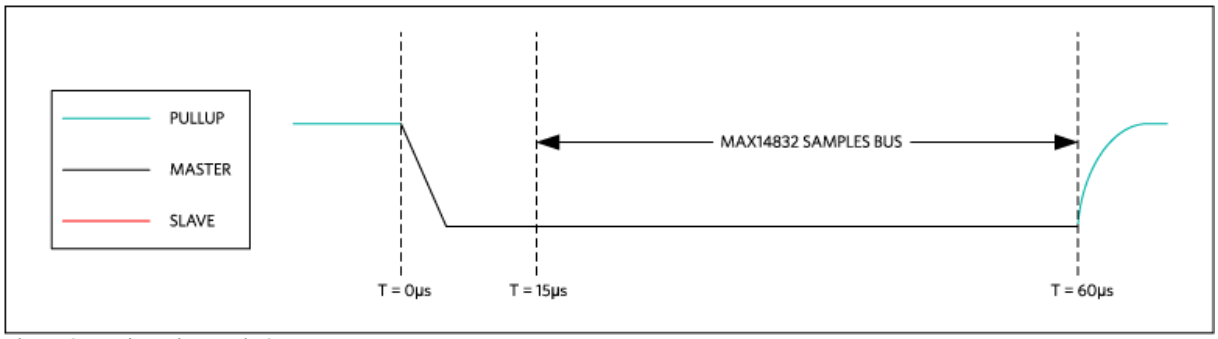

Figure 2. 1-Wire write: Logic 0.

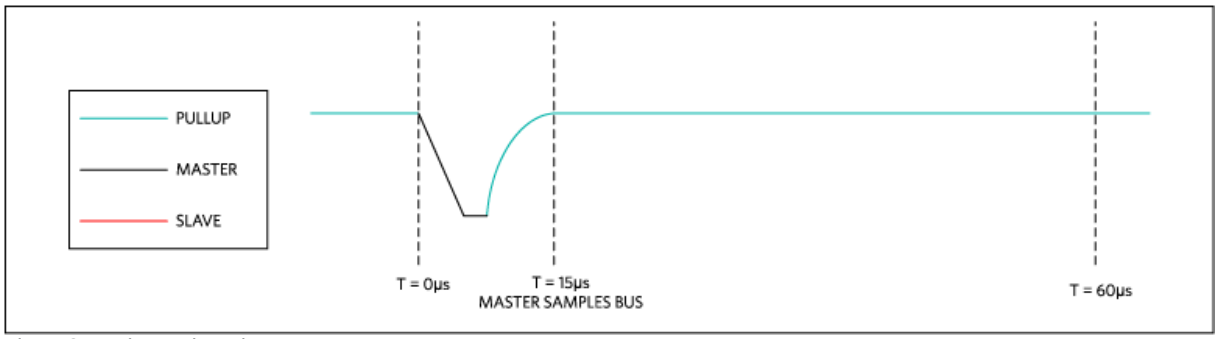

Figure 3. 1-Wire read: Logic 1.

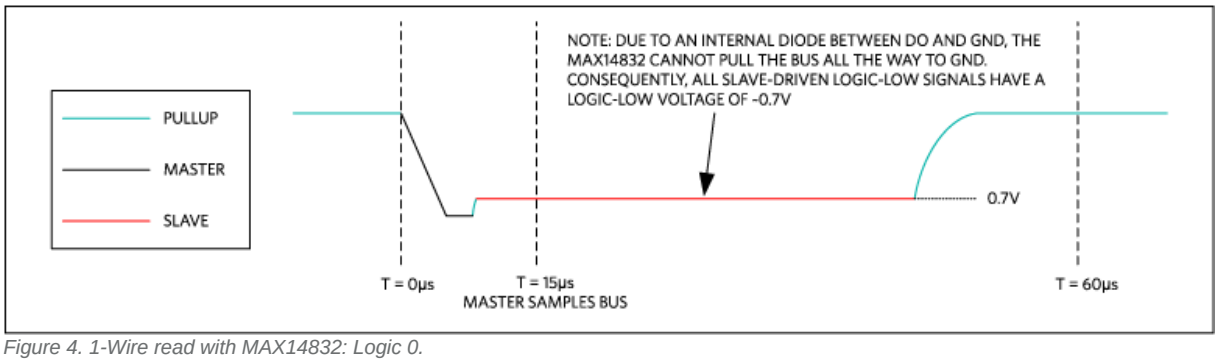

Figure 4. 1-Wire read with MAX14832: Logic 0.

1-Wire Protocol

To communicate with the MAX14832 through the 1-Wire interface (writing/reading registers or sending execution commands) the following protocol is required.

1-Wire Setup Procedure

To accomplish 1-Wire setup two signals are required: RESET and PRESENCE. First, the 1-Wire master sends a RESET pulse then releases the bus, which returns to its idle-high state. A RESET pulse is defined as a low-voltage pulse that is between 480µs and 640µs in duration. This pulse resets the MAX14832 1-Wire block, placing it in a known state. In response to the RESET, the MAX14832 sends a PRESENCE pulse, defined as a low pulse between 60µs and 240µs in duration, to notify the master of its presence on the bus. Specific timing requirements for the pulses are found in **Figure 5**. The scope shot in **Figure 6** shows the RESET and PRESENCE pulses to scale.

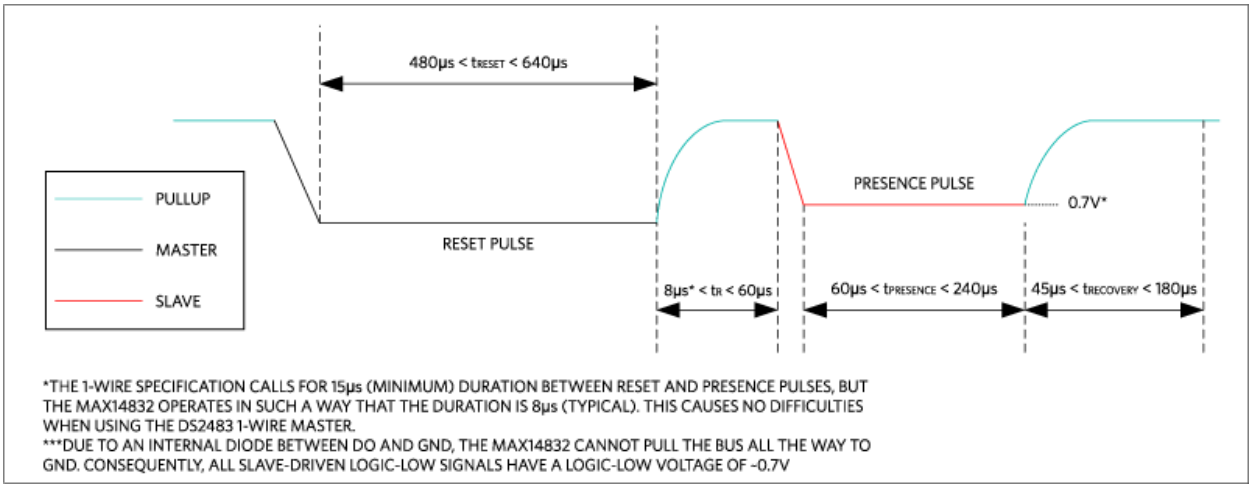

Figure 5. RESET/PRESENCE waveform and timing information.

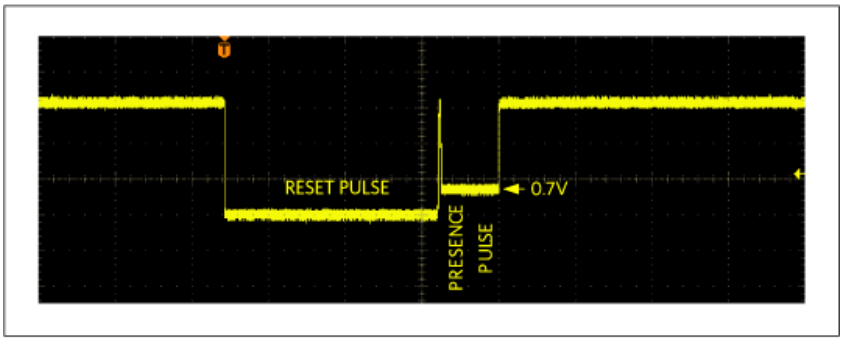

Figure 6. RESET/PRESENCE scope shot.

COMMAND BYTE

Once the 1-Wire setup signals have been sent, the MAX14832 waits for a COMMAND byte. The COMMAND byte, sent according to the timing outlined in Figures 1 and 2, contains information for the MAX14832 about what the master requires (**Figure 7**). The byte always starts with logic 0 as the most significant bit (MSB) to let the MAX14832 know that a command is coming. The second bit tells the MAX14832 whether a write is coming from the master or a read is requested by the master. The remaining bits are register address bits to inform the MAX14832 which register will be read or written to.

Once the COMMAND byte has been sent, the subsequent DATA byte contains the data that will be written to the MAX14832 in the case of a write command or the data read from the MAX14832 in the case of a read command.

COMMAND BYTE							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
START	R/W	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

START: ALWAYS 0. USED BY THE SLAVE (MAX14832) 1-Wire CIRCUIT TO UNDERSTAND WHEN A COMMAND BYTE IS INCOMING.
R/W: 1 = READ FROM SLAVE (MAX14832) IS REQUESTED; 0 = WRITE TO SLAVE (MAX14832) IS COMING.
ADD5—ADD0: REGISTER ADDRESS (ADD5 IS THE MSB AND ADD0 IS THE LSB).

DATA BYTE							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 7. RESET/PRESENCE waveform and timing information.

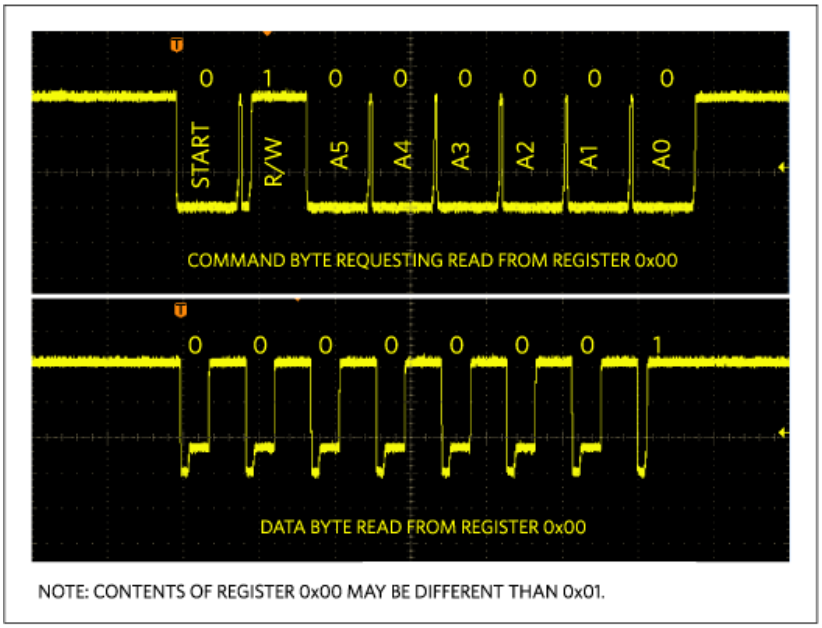

Figure 8. COMMAND and DATA bytes (read register 0x00).

1-Wire Write

If a write is indicated in the COMMAND byte, the 1-Wire master must then send a DATA byte (Figure 7) to the MAX14832 (using the timing specified in Figures 1 and 2). The DATA byte contains the 8 bits of data that will be written to the register addressed in bits 0 to 5 of the COMMAND byte. Once the DATA byte has been sent, the transaction is over. To begin another transaction, another setup sequence with a RESET and PRESENCE pulse is required. Thus, each write transaction includes a RESET and PRESENCE pulse, followed by a COMMAND byte, and finalized with a DATA byte sent to the MAX14832 (**Figure 9**).

1-Wire Read

If a read is indicated by the COMMAND byte, the MAX14832 sends a DATA byte (Figure 7) to the 1-Wire master (using the timing specified in Figures 3 and 4). The DATA byte contains the 8 bits of data that have been read from the register addressed in bits 0 to 5 of the COMMAND byte (**Figure 8**). Once the DATA byte has been received by the master, the transaction is over. To begin another transaction, another setup sequence with a RESET and PRESENCE pulse is required. Thus, each read transaction includes a RESET and PRESENCE pulse, followed by a COMMAND byte, and finalized with a DATA byte sent from the MAX14832 (Figure 9).

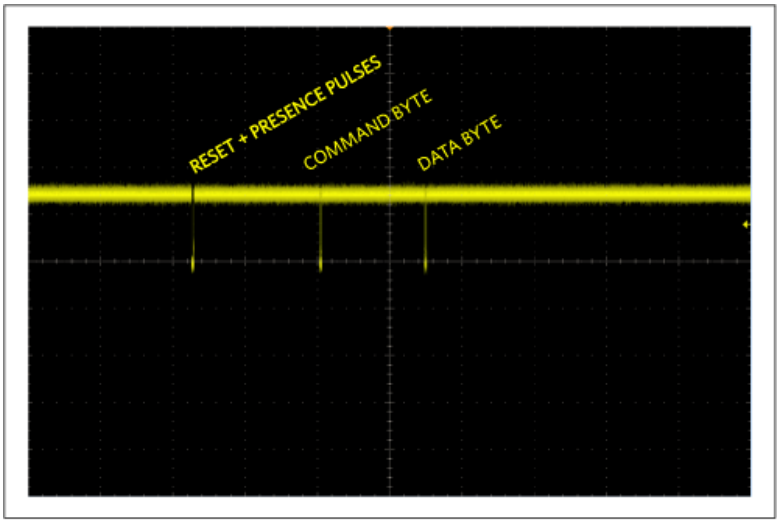

Figure 9. 1-Wire transaction.

One-Time Programming of MAX14832

Programming the MAX14832 is accomplished using the sensor interface pins (V_{CC}, DO, and GND) and the 1-Wire interface protocol as defined above. For additional information on the 1-Wire interface standard, see the 1-Wire tutorial video. Note that the MAX14832 is not fully 1-Wire compliant and is only compatible with the standard (15.6kbps) mode.

During 1-Wire communication, a 220 pullup resistor should be used on the DO line to create a strong pullup, while still allowing the DO to be pulled sufficiently low during an output low state. If a stronger pullup is required, a resistor no less than 100 should be used for reliable 1-Wire communication. To program the MAX14832, follow the procedure outlined in the flow chart below (**Figure 10**).

The procedure requires the user to access OTP mode. To access OTP mode, ensure the die temperature is between 0°C and +85°C. With the voltage supplied to V_{CC} between 3.8V and 4.1V, use the 1-Wire interface to write the OTP Mode Code (0x3C) to the OTPModeEna (0x2A) register (**Figure 11**). This write enables OTP mode, but the device does not yet enter the mode. Finally, write the validation code (0x96) to the OTPModeVal (0x36) register to enter OTP mode (**Figure 12**). At this point, set the voltage at V_{CC} between 12V and 34V to ensure sufficient supply voltage for OTP and continue with the process detailed in Figure 10. During OTP, the supply must be able to source a maximum of 15mA to the MAX14832 to ensure reliable OTP. Table 1 of the MAX14832 data sheet contains the register map for the OTP process.

To exit OTP mode, cycle the power and generate a POR or write any value other than 0x96 to the OTPModeVal (0x36) register.

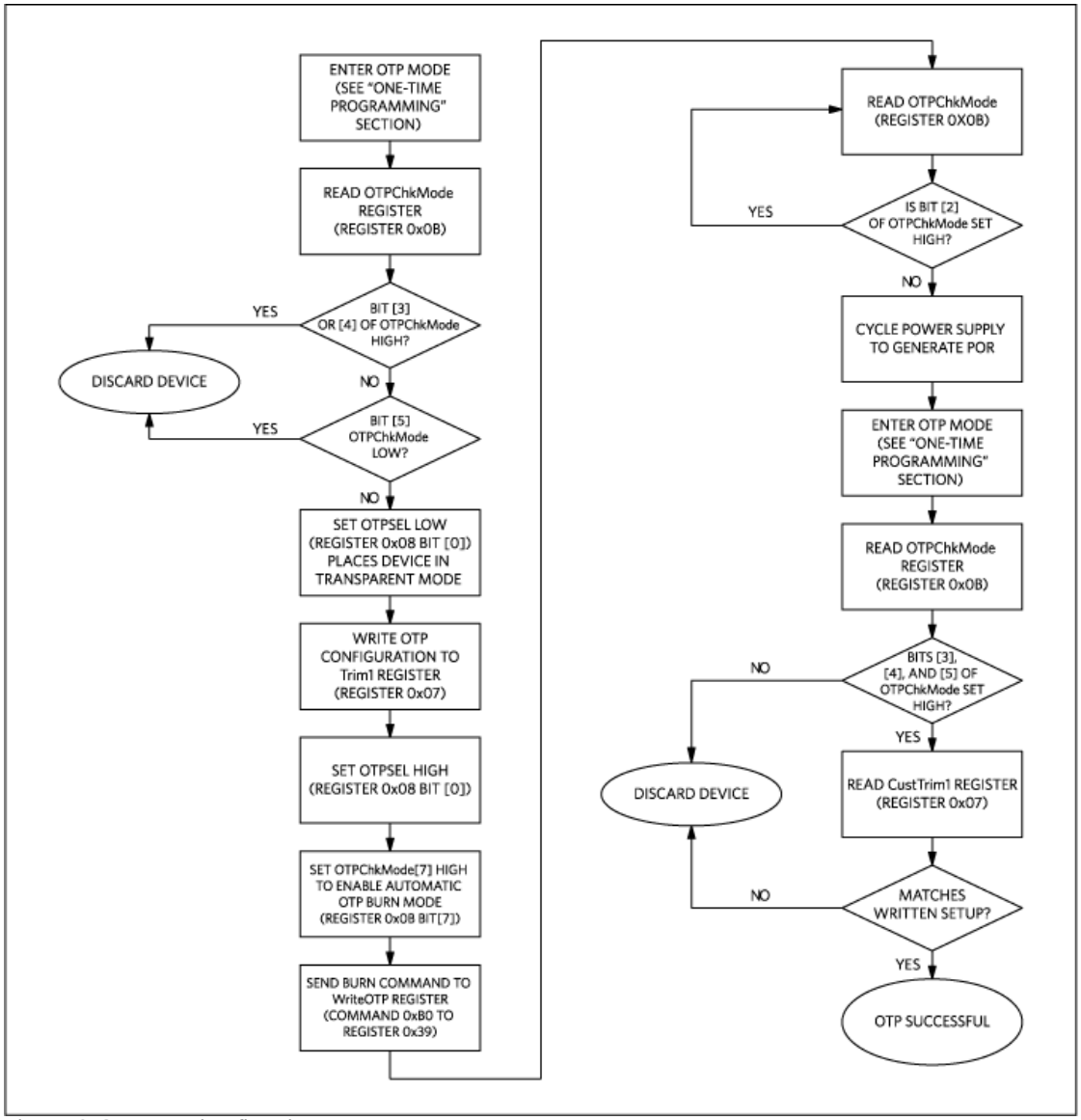

Figure 10. OTP procedure flow chart.

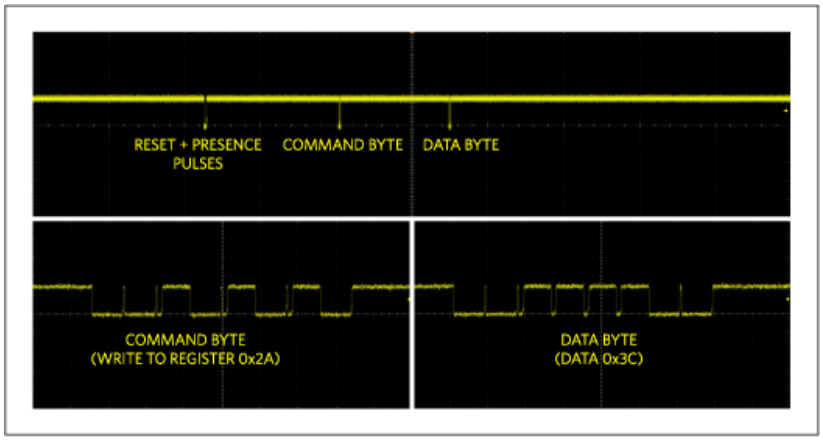

Figure 11. OTP mode enable command.

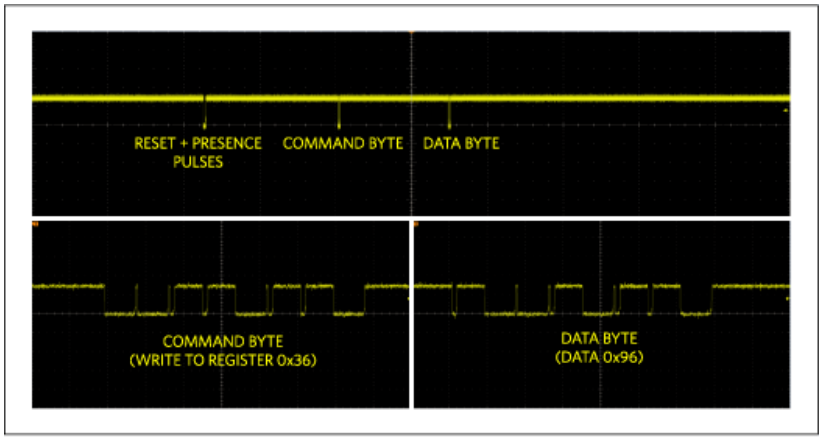

Figure 12. OTP mode validation command.

Test OTP Configuration before Final OTP of MAX14832

Prior to OTP, the operation of the MAX14832 in the desired configuration can be evaluated by entering OTP mode as described above and writing the desired bit configuration to the Trm1 (0x07) register. Once the configuration is written, write a 0 to bit [0] of the OTPCnt (0x08) register, then write any value other than 0x96 to the OTPModeValid (0x36) register to exit OTP mode. The device reads the configuration bits (LDO5, PORD[1:0], NO, PP, NPN, PULSESTR) and keeps it until any value other than 0x96 is written to the OTPModeVal (0x36) register.

OTP Failure Detection

The MAX14832 features an internal OTP failure detection system that provides visual feedback of OTP faults. When the part has not been programmed or when one or more OTP values lose the programmed value for any reason, the MAX14832 enters safe mode and signals a fault condition. The fault condition is signaled by the LED_ pins being driven 180° out of phase at f = 1Hz with 50% duty cycle (**Figure 13**). If a fault is detected, the device has been programmed incorrectly and should be discarded.

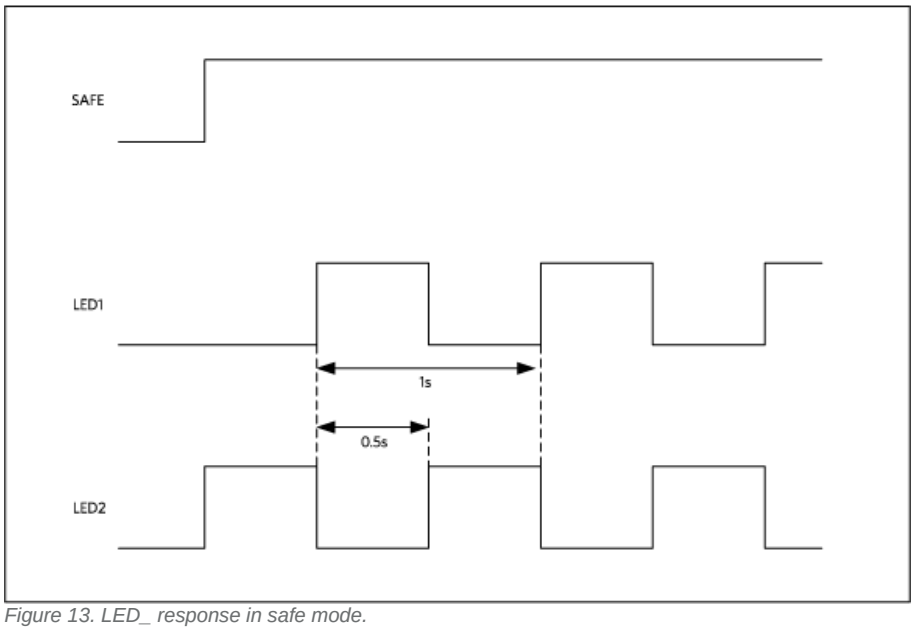

Figure 13. LED_ response in safe mode.

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Related Parts	
MAX14832	One-Time Programmable Industrial Sensor Output Driver

More Information
For Technical Support: http://www.maximintegrated.com/en/support
For Samples: http://www.maximintegrated.com/en/samples
Other Questions and Comments: http://www.maximintegrated.com/en/contact

Application Note 5778: http://www.maximintegrated.com/en/an5778
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