INVENTEK SYSTEMS

ISM43907-L170

System in Package

SiP

802.11 a/b/g/n

Data Sheet

Table of Contents

1 PART NUMBER DETAIL DESCRIPTION

1.1 Ordering Information

Device	Description	Ordering Number
ISM43907-L170	2.4/5G Wi-Fi SiP Module	ISM43907-L170
ISM43907-L170-EVB	2.4/5G Wi-Fi SiP EVB, SDIO I/F Evaluation Board	ISM43907-L170-EVB

2 OVERVIEW

The Inventek ISM43907 single-chip Dual Band, 2.4G/5G (802.11a/b/g/n). radio device provides the highest level of integration for a wireless system, with integrated dual band Wi-Fi based on Cypress' IEEE802.11 a/b/g/n single-stream with support for antenna diversity and provisions for supporting future specifications. Thus, the ISM43907 can be used to enable wireless connectivity to the simplest existing sensor products with minimal engineering effort. The ISM43907 also includes integrated power amplifiers, LNAs and T/R switches for the 2.4 GHz and 5 GHz WLAN bands, greatly reducing the external part count, PCB footprint, and cost of the solution. The ISM43907 also integrates an embedded ARM CortexTM-R4 MCU, clock, and front end with the Dual Band radio. In addition, the ISM43907 includes 640K ROM and 2MB of SRAM.

The ISM43907 is provided in the smallest LGA form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form and function. Comprehensive power management circuitry and software ensure the system can meet the needs of high mobile devices that require minimal power consumption and reliable operations.

The ISM43907 also enables coexistence support for external radios such as cellular and LTE, GPS, and Ultra-Wideband. For the WLAN section, the host interface is a SDIO v2.0 interface.

The ISM43907 is a complete WiFi & MCU SiP which is designed for embedded wireless solution and a cost-effective, low power capabilities high performance MCU in M2M applications.

The ISM43907 includes standards-based wireless technologies to enable IP infrastructures for smart grid, smart home, security, building automation, toys, robots, remote health and wellness monitoring and other M2M and IoT applications.

The ISM43907 enables customers to reduce development time, lower manufacturing costs, save board space, ease certification, and minimize RF expertise required. Additionally, the ISM43907 is provided as a complete platform solution including software drivers, sample applications, API guide, user documentation and a world-class support community from Cypress WICED Platform.

3 FEATURES

The ISM43907 supports the following WLAN functions:

- Dual-band 2.4 GHz and 5 GHz IEEE 802.11 a/b/g/n Frequency Band
- IEEE802.11 a / b / g / n (single-stream), dual-band radio with internal Power Amplifiers, LNAs and T/R switches
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Single and dual-antenna support
- WLAN host interface :
    - SDIO v2.0, including default and high-speed timing.
- ARM 32-bit CortexTM-R4 embedded processor
- SPI, UART serial interface options
- JTAG debug interface
- 2MB of application SRAM, 640KB of ROM containing WICED SDK
- Sensor applications support with ADC, I2C, I2S, GPIO, USB, PWM
- Single-chip MAC/BB/RF On-chip functionality
- Modulation Modes: WiFi: CCK and OFDM with BPSK, QPSK, 16 QAM, 64QAM
- Hardware Encryption: WEP, WPA/WPA2
- Supported Data Rates:
    - IEEE 802.11b 1 – 11 Mbps
    - IEEE 802.11a 6 – 54 Mbps
    - IEEE 802.11g 6 – 54 Mbps
    - IEEE 802.11n (2.4 GHz & 5GHz) 7.2 – 150Mbps
- Advanced 1x1 802.11n features:
    - Full/Half Guard Interval
    - Frame Aggregation
    - Space Time Block Coding (STBC)
    - Low Density Parity Check (LDPC) Encoding
- Two antenna configurations supporting antenna diversity.
- WICED Fully compatible
- Inventek **IWIN** (Inventek Wireless Interoperability Network), AT Command SW
- MSL level 3
- Supports BT/BLE COEX
- Operating Temperature: -40C to +85C
- RoHS compliant
- Pb-Free
- FCC and CE complaint

3.1 Limitations

Inventek Systems products are not authorized for use in safety-critical applications (such as life support) where a failure of the Inventek Systems product would reasonably be expected to cause severe personal injury or death.

3.2 Regulatory Compliance

CE FCC

Regulator	Status
FCC	Pending*
IC	Pending*
RoHS	Compliant

*: Pre-scan only. Certification Testing required.

Inventek has obtained FCC and CE SiP transmitter certifications for the ISM43907 SiP. These certifications can be used to the advantage of any manufacturer developing a product using these devices. In order to take full advantage of the certifications, developers must follow the antenna design/layout guidelines exactly as shown in the datasheet. For FCC compliance, products will still need to go through verification testing or have a declaration of conformance according to 47 CFR Chapter 1, part 15, subpart B.

The testing required for both verification and declaration of conformance is specified in sections 15.107 and 15.109. The official documents can be obtained from the U.S Government Printing Office online. U.S. Government Printing Office CFR 47. There are some changes allowed to the reference design which do not require any testing beyond the verification or declaration of conformance.

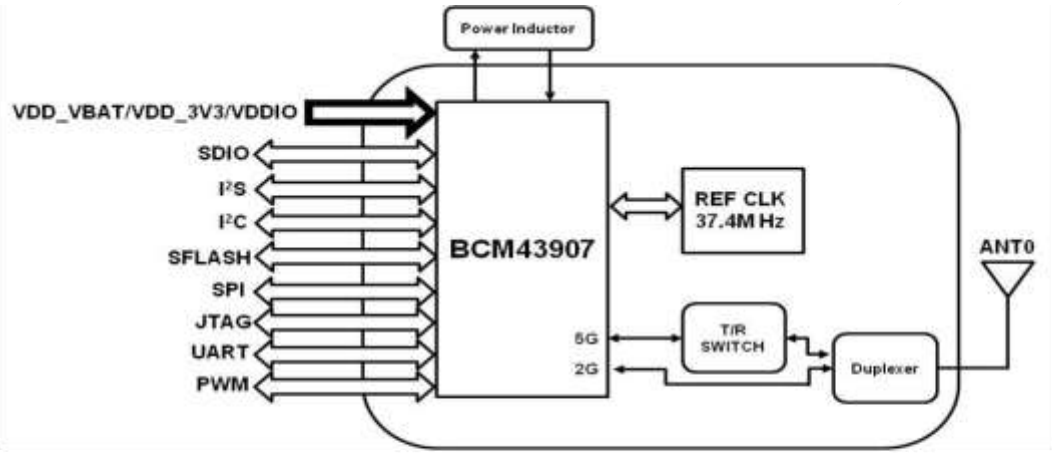
If it is desired to add a connector or U.Fl connector in the RF path, or change the antenna to one of the same type (chip) with equal or less gain, customers can do so without refiling. Other changes such as a different antenna, or adding an antenna diversity switch will require filing for a class 2 permissive change. This costs about half as much as the full certification. Any class 2 permissive changes must be performed under Inventek's grant, and therefore must be done in cooperation with Inventek. In addition to this document, Inventek recommends verifying the schematic board design with Inventek Engineering once the schematic is complete for further review and validation.

4 COMPLEMENTARY DOCUMENTATION

4.1 ISM43907 Support HW, SW and Collateral:

- Evaluation Board
  - Evaluation Board Specification
  - EVB User's Guide
- Drivers under NDA
- Design and Antenna layout Guidelines

5 ISM43907-L170 BLOCK DIAGRAM



I2C	Intelligent Interface Controller
SPI	Serial Peripheral Interface
UART	Universal asynchronousreceiver transmitters
PWM	Pulse Width Modulation
I2S	Inter-integrated sound

Figure 1 Inventek's ISM43907 General Block Diagram

6 HOST INTERFACES

6.1 UART Interface

The ISM43907 UART is a standard 4-wire interface (RX, TX, RTS and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command. The UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFO is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.0 UART HCI specification: H4, a custom Extended H4 and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification ("Three-wire UART Transport Layer"). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals. The ISM43907 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleet state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The ISM43907 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2% (see Table 12).

Desired Rate	*Actual Rate*	*Error (%)*
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Table 1: Example of Common Baud Rates

7 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 28 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Rating	*Symbol*	*Max Value*	*Unit*
Supply Power	Volt	+4	V
Storage Temp.	Celsius	-40C to +85	C
Voltage Ripple	Ripple	+/- 2%	V
DC supply voltage for VBAT	VDD_VBAT	5.5	V
3.3V Input	VDD_3V3_IN	3.9	V
Power I/O supply	VDDIO	3.9	V
I/O supply for Audio	VDDIO_AUDIO	3.9	V
I/O supply for SDIO	VDDIO_SD	3.9	V
3.3V supply for USB	USB_VDD_3V3	3.9	V

Table 3: Absolute Maximum Ratings

NOTE: Please place a 10-15uF Bulk CAP as close to the module as possible to VDD_3V3_IN

7.2 Environmental Ratings

Characteristic	*Value*	*Units*	*Conditions/Comments*
Ambient Temperature (Ta)	-40 to +85	°C	* Functional operation
Storage Temperature	-40 to +125	°C	
Relative Humidity	Less than 60	%	Storage
	Less than 95	%	Operation

Table 4: Environmental Ratings

7.3 Recommended Operating Conditions and DC Characteristics

⚠ **Caution!** Functional operation is not guaranteed outside of the limits shown in Table 5 and operation outside these limits for extended periods can adversely affect long-term reliability of this devices.

Parameter	Symbol	Min	Typical	Max	Unit
VDD_VBAT	DC supply voltage for VBAT	2.0	3.3	3.6	V
VDD_3V3_IN	3.3V Input	2.4	3.3	3.6	V
VDDIO	Power I/O supply	2.4	3.3	3.6	V
VDDIO_AUDIO	I/O supply for Audio	2.4	3.3	3.6	V
VDDIO_SD	I/O supply for SDIO	3.0	3.3	3.6	V
USB_VDD_3V3	3.3V supply for USB	3.0	3.3	3.6	V

Table 5: Recommended Operating Conditions and DC Characteristics

7.4 WLAN Current Consumption

Condition: 25deg.C, includes Both WiFi and embedded R4 MCU

Parameter	Condition	Min	Typical	Max	Unit
Tx mode(11a Max current)	54 Mbps		320		mA
Tx mode(11b Max current)	11 Mbps		380		mA
Tx mode(11g Max current)	54 Mbps		280		mA
Tx mode(11n Max current)	HT20 MCS7 @ 2.4GHz		270		mA
Tx mode(11n Max current)	HT20 MCS7 @ 5GHz		310		mA
Tx mode(11n Max current)	HT40 MCS7 @ 5GHz		121		mA
Rx mode	11a (54Mbps)		107		mA
Rx mode	11b (11Mbps)		107		mA
Rx mode	11g (54Mbps)		107		mA
Rx mode	11n (HT20				

	MCS7 @ 2.4GHz)		120		mA
Rx mode	11n (HT20 MCS7 @ 5GHz)		130		mA
Rx mode	11n (HT40 MCS7 @ 5GHz)		320		mA

8 RF SPECIFICATIONS

8.1 Wi-Fi RF SPECIFICATION

Parameter	***Description***
WLAN Standards	IEEE 802 Part 11a/b/g/n (802.11a/b/g/n single stream n)
Antenna Port	Support Single Antenna for WiFi
Frequency Band	2.400 – 2.484 GHz, 5.180 – 5.825GHz

Table 6: Wi-Fi RF Specifications

Wi-Fi RF Performance: The default voltage is 3.6V.

Parameter	***Description***
Frequency Band	2.4 GHz ISM Band and 5GHz U-NII Band
Number of selectable Sub Channels	2GHz support 14 channels and 5GHz channels
Modulation	OFDM, DSSS (Direct Sequence Spread Spectrum), DBPSK, DQPSK, CCK, 16QAM, 64QAM,
Supported Rates	1,2, 5.5,11,6,9,12,24,36,48,54 Mbps & HT20 and HT40 MCS 0~7
Maximum Receive Input Level	-10dBm (with PER < 8%@11 Mbps) -20dBm (with PER < 10%@54 Mbps at 2.4GHz) -30dBm (with PER < 10%@54 Mbps at 5GHz) -20dBm (with PER < 10%@HT20 MCS7 at 2.4GHz) -30dBm (with PER < 10%@HT20 &HT40 MCS7 at 5GHz)
Output Power	14dBm @ 802.11a 17dBm @ 802.11b 14dBm @ 802.11g 14dBm @ 802.11n HT20 at 2.4GHz 13dBm @ 802.11n HT20 at 5GHz
Carrier Frequency Accuracy	+/- 20ppm

Table 7: RF Performance

8.2 802.11b Transmit

Item	Conditions	Min	Typical	Max	Unit
Transmit output power level	1M/2M/5.5M/11M		17		dBm
Transmit center frequency tolerance		-20	0	20	ppm
Transmit center frequency tolerance	Fc-22MHz<F<Fc-11MHz & Fc+11MHz<F<Fc+22MHz(1/2/5.5/11Mbps; channel 1~13)			-30*	dBr
Transmit spectrum mask	F<Fc-22MHz & F>Fc+22MHz(1/2/5.5/11Mbps; channel 1~13)			-50*	dBr
Transmit power-on	10% ~ 90 %		0.3	2*	us
Transmit power-down	90% ~ 10 %		1.5	2*	us
Transmit modulation accuracy	1/2/5.5/11 Mbps		-17	-10	dB

* Indicates IEEE802.11 specification

Table 8: 802.11b Transmit

8.3 802.11g Transmit

Item	Conditions	Min	Typical	Max	Unit
Transmit output power level	6M/9M/12M/18M/24M/36M/48M/54M		14		dBm
Transmit center frequency tolerance		-20	0	20	ppm
Transmit modulation accuracy	6Mbps 9Mbps 12Mbps 18Mbps 24Mbps 36Mbps 48Mbps 54Mbps @ 11MHz			-5* -8* -10* -13* -16* -19* -22* -25* -20*	dB dB dB dB dB dB dB dB dBr
Transmit spectrum mask	@ 20MHz @ 30MHz			-28* -40*	dBr dBr
Transmit spectrum mask	10% ~ 90 %		0.3	2*	us

* Indicates IEEE802.11 specification

Table 9: 802.11g Transmit

8.4 802.11n Transmit

Item	Conditions	Min	Typical	Max	Unit
Transmit output power level	HT20 MCS 0~7		14		dBm
Transmit center frequency tolerance		-20	0	20	ppm
Transmit modulation accuracy	HT20 MCS 0~7			-27*	dB
Transmit spectrum mask	@11MHz			-20*	dBr
Transmit spectrum mask	@ 20MHz @ 30MHz			-28* -40*	dBr dBr

* Indicates IEEE802.11 specification

Table 10: 802.11n Transmit

8.5 802.11a Transmit

Item	Conditions	Min	Typical	Max	Unit
Transmit output power level	6M/9M/12M/18M/24M/36M/48M/54M		14		dBm
Transmit center frequency tolerance		-20	0	20	ppm
Transmit modulation accuracy	6Mbps 9Mbps 12Mbps 18Mbps 24Mbps 36Mbps 48Mbps 54Mbps @ 11MHz			-5* -8* -10* -13* -16* -19* -22* -25* -20*	dB dB dB dB dB dB dB dB dBr
Transmit spectrum mask	@ 20MHz @ 30MHz			-28* -40*	dBr dBr

* Indicates IEEE802.11 specification

Table 11: 802.11a Transmit

8.6 802.11n Transmit @5GHz

Item	Conditions	Min	Typical	Max	Unit
Transmit output power level	HT20 MCS 0~7		13		dBm
Transmit center frequency tolerance		-20	0	20	ppm
Transmit modulation accuracy	HT20, MCS0~7			-27*	dB
Transmit spectrum mask	@ 11MHz @ 20MHz @ 30MHz			-20* -28* -40*	dBr dBr dBr

* Indicates IEEE802.11 specification

Table 12: 802.11n Transmit @ 5GHz

8.7 Receiver Specification 802.11b

Item	Conditions	Min	Typical	Max	Unit
Receiver minimum input level sensitivity (PER<8%)	1Mbps 2Mbps 5.5Mbps 11Mbps	-80* -80* -76* -76*	-96 -93 -91 -87		dBm dBm dBm dBm
Receiver maximum input level sensitivity (PER<8%)	1/2/5.5/11 Mbps	-10*			dBm

* Indicates IEEE802.11 specification

Table 13: 802.11b Receiver

8.8 Receiver Specification 802.11g

Item	Conditions	Min	Typical	Max	Unit
Receiver minimum input level sensitivity (PER<10%)	6Mbps 9Mbps 12Mbps 18Mbps 24Mbps 36Mbps 48Mbps 54Mbps	-82* -81* -79* -77* -74* -70* -66* -65*	-92 -90 -89 -87 -84 -80 -76 -75		dBm dBm dBm dBm dBm dBm dBm dBm
Receiver maximum input level sensitivity (PER<10%)	6/9/12/18/24/36/48/54	-20*			dBm

* Indicates IEEE802.11 specification

Table 14: 802.11g Receiver

8.9 Receiver Specification 802.11n @ 2.4GHz

Item	Conditions	Min	Typical	Max	Unit
Receiver minimum input level sensitivity (PER<10%)	HT20, MCS0 HT20, MCS1 HT20, MCS2 HT20, MCS3 HT20, MCS4 HT20, MCS5 HT20, MCS6 HT20, MCS7	-82* -79* -77* -74* -70* -66* -65* -64*	-91 -89 -86 -83 -80 -75 -73 -72		dBm dBm dBm dBm dBm dBm dBm dBm
Receiver maximum input level sensitivity (PER<10%)	MSC0~MSC7	-20*			dBm

* Indicates IEEE802.11 specification

Table 15: 802.11n Receiver @ 2.4GHz

8.10 Receiver Specification 802.11a

Item	Conditions	Min	Typical	Max	Unit
Receiver minimum input level sensitivity (PER<10%)	6Mbps 9Mbps 12Mbps 18Mbps 24Mbps 36Mbps 48Mbps 54Mbps	-82* -81* -79* -77* -74* -70* -66* -65*	-90 -89 -88 -85 -82 -79 -74 -73		dBm dBm dBm dBm dBm dBm dBm dBm
Receiver maximum input level sensitivity (PER<10%)	6/9/12/18/24/36/48/54	-30*			dBm

* Indicates IEEE802.11 specification

Table 16: 802.11a Receiver

8.11 Receiver Specification 802.11n @ 5GHz

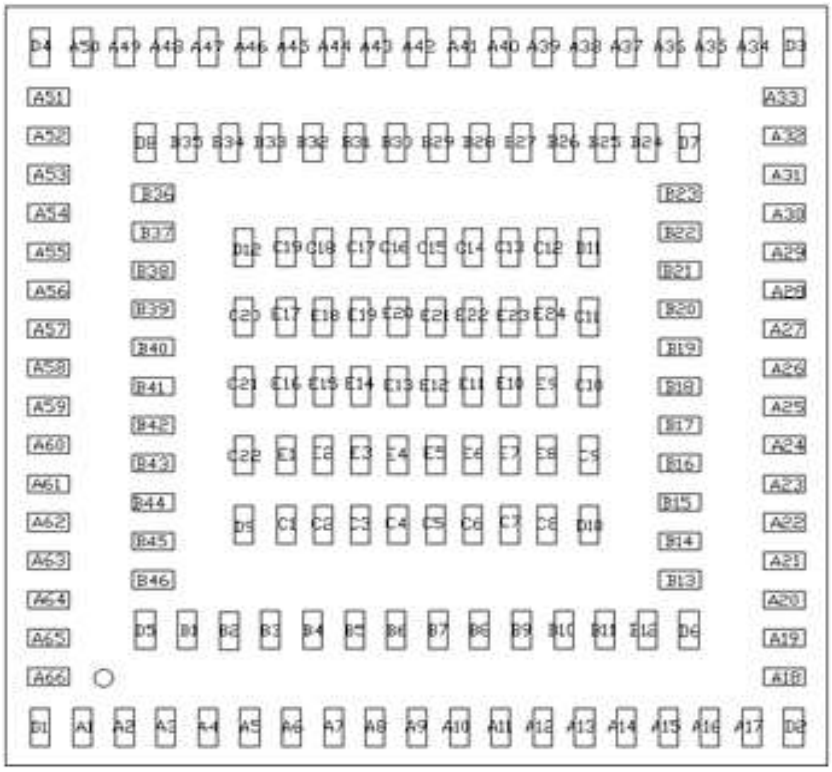
Item	Conditions	Min	Typical	Max	Unit
Receiver minimum input level sensitivity (PER<10%)	HT20, MCS0 HT20, MCS1 HT20, MCS2 HT20, MCS3 HT20, MCS4 HT20, MCS5 HT20, MCS6 HT20, MCS7 HT40, MCS0 HT40, MCS1 HT40, MCS2 HT40, MCS3 HT40, MCS4 HT40, MCS5 HT40, MCS6 HT40, MCS7	-82* -79* -77* -74* -70* -66* -65* -64* -79* -76* -74* -71* -67* -63* -62* -61*	-90 -87 -85 -82 -78 -73.5 -72 -70 -87 -84 -81 -78 -75 -70 -69 -68		dBm dBm dBm dBm dBm dBm dBm dBm dBm dBm dBm dBm dBm dBm dBm dBm
Receiver maximum input level sensitivity (PER<10%)	HT20 &HT40 MSC0~MSC7 @ 5GHz	-30*			dBm

* Indicates IEEE802.11 specification

Table 17: 802.11n Receiver @ 5GHz

9 PIN OUT AND DESCRIPTIONS

9.1 Pin Number sequence definition



TOP View

9.2 The detail pin definition information

Pin Number	Pin Name	Type	Description
A20	ANT0_DIV_RF_SW_CTRL_4	O	ANT0 RF switch control
A19	ANT1_DIV_RF_SW_CTRL_5_DAP_CLK_SEL	I/O	ANT1 RF switch control
A9	NC	-	Floating
C21	NC	-	Floating
B46	NC	-	Floating
B1	NC	-	Floating
A10	NC	-	Floating
B5	NC	-	Floating
B7	NC	-	Floating

C1	NC	-	Floating
C3	NC	-	Floating
D2	GND	GND	
D4	GND	GND	
D3	GND	GND	
D10	GND	GND	
D9	NC	-	Floating
D12	GND	GND	
D11	GND	GND	
A16	GND	GND	
A3	GND	GND	
A62	GND	GND	
A50	GND	GND	
A45	GND	GND	
A43	GND	GND	
A31	GND	GND	
A26	GND	GND	
A24	GND	GND	
A18	GND	GND	
B6	GND	GND	
B3	GND	GND	
B2	GND	GND	
B40	GND	GND	
B38	GND	GND	
B36	GND	GND	
B33	GND	GND	
B32	GND	GND	
B28	GND	GND	
B25	GND	GND	
B24	GND	GND	
B23	GND	GND	
B13	GND	GND	
C4	GND	GND	
C2	GND	GND	
C22	GND	GND	
C20	GND	GND	
C19	GND	GND	
C18	GND	GND	
C14	GND	GND	
C12	GND	GND	
C11	GND	GND	
C9	GND	GND	
E8	GND	GND	
E7	GND	GND	
E6	GND	GND	
E5	GND	GND	

E4	GND	GND	
E3	GND	GND	
E2	GND	GND	
E1	GND	GND	
E16	GND	GND	
E15	GND	GND	
E14	GND	GND	
E13	GND	GND	
E12	GND	GND	
E11	GND	GND	
E10	GND	GND	
E9	GND	GND	
E24	GND	GND	
E23	GND	GND	
E22	GND	GND	
E21	GND	GND	
E20	GND	GND	
E19	GND	GND	
E18	GND	GND	
E17	GND	GND	
A8	GND	GND	
A6	GND	GND	
A47	GND	GND	
A39	GND	GND	
A37	GND	GND	
B20	GND	GND	
C7	GPIO_0	I/O	Programmable GPIO pin
A34	GPIO_1_GSPI_MODE	I/O	Enable gSPI interface
D8	GPIO_10	I/O	Programmable GPIO pin
A21	GPIO_11_ACPU_BOOT_MODE	I/O	Boot from tightly coupled
C17	GPIO_12	I/O	Programmable GPIO pin
B34	GPIO_13_SDIO_MODE	I/O	Programmable GPIO
B35	GPIO_14	I/O	Programmable GPIO pin
B30	GPIO_15	I/O	Programmable GPIO pin
B19	GPIO_16	I/O	Programmable GPIO pin
C16	GPIO_2_JTAG_TCK	I/O	Programmable GPIO/ JTAG
D6	GPIO_3_JTAG_TMS	I/O	JTAG/ Programmable GPIO pin
C6	GPIO_4_JTAG_TDI	I/O	Programmable GPIO pin/JTAG
B9	GPIO_5_JTAG_TDO	I/O	JTAG/ Programmable GPIO pin
C5	GPIO_6_JTAG_TRST	I/O	Programmable GPIO pin/JTAG
B10	GPIO_7_WCPU_BOOT_MODE	I/O	Boot from SoC SROM or SOC
B12	GPIO_8_TAP_SEL	I/O	Programmable GPIO/ JTAG
A15	GPIO_9_USB_SEL	I/O	Select USB Mode
B14	HIB_LPO_SEL	I	Select precise or coarse 32 kHz
			Used by the hibernation block
B17	HIB_WAKE	I	Wake up chip from hibernation
A27	HIB_XTAL_IN	I	XTAL input for hibernation block

A28	HIB_XTAL_OUT	O	XTAL output for hibernation
A58	I2C_0_SCL	O	BSC master clock
A51	I2C_0_SDA	I/O	BSC serial data
A57	I2C_1_SCL	O	BSC master clock
A52	I2C_1_SDA	I/O	BSC serial data
A61	I2S1_MCK	I/O	I2S M clock
B41	I2S0_MCK	I/O	I2S M clock
A59	I2S0_SCK_BCLK	I/O	I2S Bit clock
A54	I2S0_SD_IN	I	I2S data input
A56	I2S0_SD_OUT	O	I2S data output
A55	I2S0_WS_LRCLK	I/O	I2S LR clock
B43	I2S1_SCK_BCLK	I/O	I2S Bit clock
B42	I2S1_SD_IN	I	I2S data input
A60	I2S1_SD_OUT	O	I2S data output
A53	I2S1_WS_LRCLK	I/O	I2S LR clock
B21	JTAG_SEL	I	JTAG enable
C13	PWM_0	O	Pulse width modulation bit 0
B15	PWM_1	O	Pulse width modulation bit 1
A30	PWM_2	O	Pulse width modulation bit 2
A29	PWM_3	O	Pulse width modulation bit 3
A35	PWM_4	O	Pulse width modulation bit 4
D7	PWM_5	O	Pulse width modulation bit 5
A22	RESET_N	I	Reset
A17	RF_ANT0	I/O	Antenna port 0
A7	NC	-	Floating
B18	RF_GPAIO_OUT	I/O	Analog GPIO
B22	RF_SW_CTRL_6_UART1_RX_IN	I	RF switch control/UART_RX
B16	RF_SW_CTRL_7_RSRC_INIT_MODE	I/O	RF switch control/UART_TX
A23	RF_SW_CTRL_8_BT_SECI_IN	I/O	RF switch control/SECI_IN
C10	RF_SW_CTRL_9_HIB_LPO_SEL	I/O	RF switch control/SECI_OUT
B29	SDIO_CLK	I/O	SDIO clock
A41	SDIO_CMD	I/O	SDIO command line
B27	SDIO_DATA0	I/O	SDIO data line 0
B26	SDIO_DATA1	I/O	SDIO data line 1
A42	SDIO_DATA2	I/O	SDIO data line 2
B31	SDIO_DATA3	I/O	SDIO data line 3
A2	SFLASH_CLK	O	Flash clock
D5	SFLASH_CSN	O	Flash slave select
A65	SFLASH_MISO_1	I/O	Flash data bit 2
A1	SFLASH_MISO_2	I/O	Flash data bit 3
A66	SFLASH_MISO_3	I/O	Flash data bit 4
D1	SFLASH_MOSI_0	I/O	Flash data bit 1
A12	SPI_0_CLK	O	SPI clock
A13	SPI_0_CS	O	SPI slave select
A11	SPI_0_MISO	I	SPI data master in
A14	SPI_0_MOSI	O	SPI data master out
B8	SPI_1_CLK	O	SPI clock

B11	SPI_1_CS	O	SPI slave select
B4	SPI_1_MISO	I	SPI data master in
B37	SPI_1_MOSI	O	SPI data master out
A49	SR_VLX1_35	PWR	PMU CBUCK Switching
A64	UART0_CTS_IN	I	UART clear-to-send
A63	UART0_RTS_OUT	O	UART request-to-send
B45	UART0_RXD_IN	I	UART serial input
B44	UART0_TXD_OUT	O	UART serial output
A38	USB_VDD_3V3	PWR	3.3V supply for USB
A32	USB2_DN	I/O	USB Data
A33	USB2_DP	I/O	USB Data
A36	USB2_HOST_DEV_SEL	I	USB HOST/DEV select
A4	NC	-	Floating
A25	VDD_3V3_IN	PWR	3.3V input
A44	VDD_3V3_LDO	PWR	3.3V output of internal LDO
A48	VDD_VBAT	PWR	VBAT input
A46	VDD1_35	PWR	Input to internal PMU LDO
B39	VDDIO	PWR	Power I/O supply
A40	VDDIO_AUDIO	PWR	I/O supply for audio
A5	NC	-	Floating
C15	VDDIO_SD	PWR	I/O supply for SDIO

9.3 Pin Multiplexing information

Function											
Pin	1	2	3	4	5	6	7	8	9	10	11
GPIO_0	GPIO_0	FAST_UART_RX	I2C1_SDAT A	PWM0	SPI1_MISO	PWM2	GPIO_12	GPIO_8		PWM4	USB20H_CTL1
GPIO_1	GPIO_1	FAST_UART_TX	I2C1_CLK	PWM1	SPI1_CLK	PWM3	GPIO_13	GPIO_9		PWM5	-
GPIO_2	GPIO_2	-	-	GCI_GPIO_0	-	-	-	-	TCK	-	-
GPIO_3	GPIO_3	-	-	GCI_GPIO_1	-	-	-	-	TMS	-	-
GPIO_4	GPIO_4	-	-	GCI_GPIO_2	-	-	-	-	TDI	-	-
GPIO_5	GPIO_5	-	-	GCI_GPIO_3	-	-	-	-	TDO	-	-
GPIO_6	GPIO_6	-	-	GCI_GPIO_4	-	-	-	-	TRST_L	-	-
GPIO_7	GPIO_7	FAST_UART_RTS_OUT	PWM1	PWM3	SPI1_CS	I2C1_ CLK	GPIO_15	GPIO_11	PMU_TESTO	-	PWM5
GPIO_8	GPIO_8	SPI1_MISO	PWM2	PWM4	FAST_UART_RX	-	GPIO_16	GPIO_12	TAP_SEL_P	I2C1_SDAT A	PWM0
GPIO_9	GPIO_9	SPI1_CLK	PWM3	PWM5	FAST_UART_TX	-	GPIO_0	GPIO_13	-	I2C1_CLK	PWM1
GPIO_10	GPIO_10	SPI1_MOSI	PWM4	I2C1_SDAT A	FAST_UART_CTS_IN	PWM0	GPIO_1	GPIO_14	PWM2	SDIO_SEP_ INT	SDIO_SEP_ INT_0D
GPIO_11	GPIO_11	SPI1_CS	PWM5	I2C1_CLK	FAST_UART_RTS_OUT	PWM1	GPIO_7	GPIO_15	PWM3	-	-
GPIO_12	GPIO_12	I2C1_SDAT A	FAST_UART_RX	SPI1_MISO	PWM2	PWM4	GPIO_8	GPIO_16	PWM0	SDIO_SEP_ INT_0D	SDIO_SEP_ INT
GPIO_13	GPIO_13	I2C1_CLK	FAST_UART_TX	SPI1_CLK	PWM3	PWM5	GPIO_9	GPIO_0	PWM1	-	-
GPIO_14	GPIO_14	PWM0	FAST_UART_CTS_IN	SPI1_MOSI	I2C1_SDAT A	-	GPIO_10	-	PWM4	-	PWM2
GPIO_15	GPIO_15	PWM1	FAST_UART_RTS_OUT	SPI1_CS	I2C1_CLK	-	GPIO_11	GPIO_7	PWM5	-	PWM3
GPIO_16	GPIO_16	FAST_UART_CTS_IN	PWM0	PWM2	SPI1_MOSI	I2C1_SDAT A	GPIO_14	GPIO_10	RF_DISABL E_L	USB20H_CTL2	PWM4

	Function										
Pin	1	2	3	4	5	6	7	8	9	10	11
SDIO_CLK	SDIO_CLK	-	-	-	-	-	-	-	SDIO_AOS_CLK	-	-
SDIO_CMD	SDIO_CMD	-	-	-	-	-	-	-	SDIO_AOS_CMD	-	-
SDIO_DATA_0	SDIO_D0	-	-	-	-	-	-	-	SDIO_AOS_D0	-	-
SDIO_DATA_1	SDIO_D1	-	-	-	-	-	-	-	SDIO_AOS_D1	-	-
SDIO_DATA_2	SDIO_D2	-	-	-	-	-	-	-	SDIO_AOS_D2	-	-
SDIO_DATA_3	SDIO_D3	-	-	-	-	-	-	-	SDIO_AOS_D3	-	-
RF_SW CTRL_5	RF_SW CTRL_5	GCI_GPIO_5	-	-	-	-	-	-	-	-	-
RF_SW CTRL_6	RF_SW CTRL_6	UART_DBG_RX	SECI_IN	-	-	-	-	-	-	-	-
RF_SW CTRL_7	RF_SW CTRL_7	UART_DBG_TX	SECI_OUT	-	-	-	-	-	-	-	-
RF_SW CTRL_8	RF_SW CTRL_8	SECI_IN	UART_DBG_RX	-	-	-	-	-	-	-	-
RF_SW CTRL_9	RF_SW CTRL_9	SECI_OUT	UART_DBG_TX	-	-	-	-	-	-	-	-
PWM0	PWM0	GPIO_2	GPIO_18	-	-	-	-	-	-	-	-
PWM1	PWM1	GPIO_3	GPIO_19	-	-	-	-	-	-	-	-
PWM2	PWM2	GPIO_4	GPIO_20	-	-	-	-	-	-	-	-
PWM3	PWM3	GPIO_5	GPIO_21	-	-	-	-	-	-	-	-
PWM4	PWM4	GPIO_6	GPIO_22	-	-	-	-	-	-	-	-
PWM5	PWM5	GPIO_8	GPIO_23	-	-	-	-	-	-	-	-
SPI0_MISO	SPI0_MISO	GPIO_17	GPIO_24								
SPI0_CLK	SPI0_CLK	GPIO_18	GPIO_25								
SPI0_MOSI	SPI0_MOSI	GPIO_19	GPIO_26								
SPI0_CS	SPI0_CS	GPIO_20	GPIO_27								
I2C0_SDATA	I2C0_SDATA	GPIO_21	GPIO_28								
I2C0_CLK	I2C0_CLK	GPIO_22	GPIO_29								
I2S_MCLK0	I2S_MCLK0	GPIO_23	GPIO_0								

Function											
Pin	1	2	3	4	5	6	7	8	9	10	11
I2S_SCLK0	I2S_SCLK0	GPIO_24	GPIO_2	-	-	-	-	-	-	-	-
I2S_LRCLK0	I2S_LRCLK0	GPIO_25	GPIO_3	-	-	-	-	-	-	-	-
I2S_SDATAI0	I2S_SDATAI0	GPIO_26	GPIO_4	-	-	-	-	-	-	-	-
I2S_SDATA0	I2S_SDATA0	GPIO_27	GPIO_5	-	-	-	-	-	-	-	-
I2S_SDATA1	I2S_SDATA1	GPIO_28	GPIO_6	-	-	-	-	-	-	-	-
I2S_SDATAI1	I2S_SDATAI1	GPIO_29	GPIO_8	-	-	-	-	-	-	-	-
I2S_MCLK1	I2S_MCLK1	GPIO_30	GPIO_17	-	-	-	-	-	-	-	-
I2S_SCLK	I2S_SCLK	GPIO_31	GPIO_30	-	-	-	-	-	-	-	-
I2S_LRCLK1	I2S_LRCLK1	GPIO_0	GPIO_31	-	-	-	-	-	-	-	-

10 Additional Information

10.1 Low Speed External Clock Source Characteristics

The ISM43907-L170 uses a secondary low frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator or crystal is required. The internal LPO frequency range is approximately 33 kHz +/- 30% over process, voltage, and temperature, which is adequate for some applications. However, one tradeoff caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake-up earlier to avoid missing beacons.

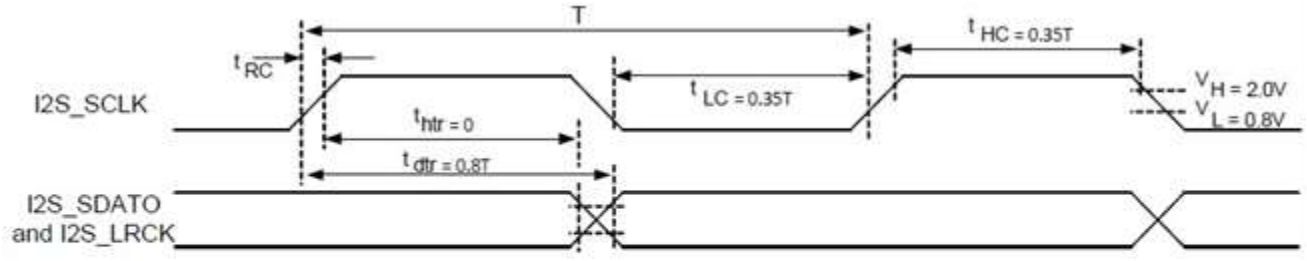
Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in below table.

a. When power is applied or switched off

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-200	Ppm
Duty cycle	30-70	%
Input signal amplitude	200-3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance[a]	>100k <5	 pF
Clock jitter (during initial start-up)	<10000	ppm

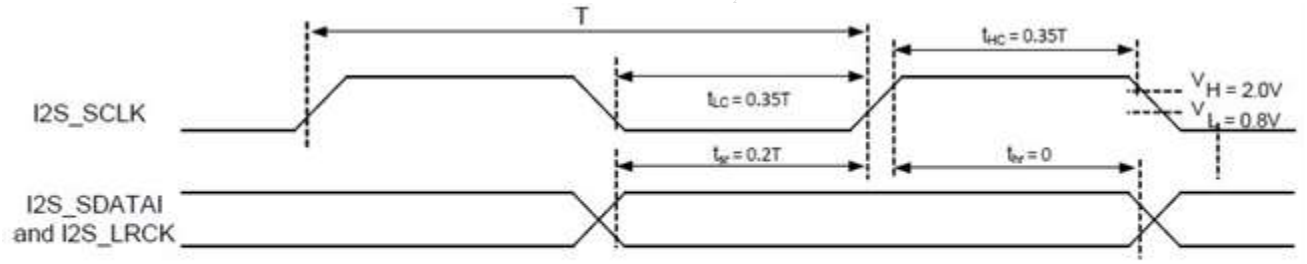
10.2 Communications Interfaces

10.2.1 I2S Master and Slave Mode TX Timing



T = Clock period.
T_{tr} = Minimum allowed clock period for transmitter.
$T > T_{tr}$.
t_{RC} is only relevant for transmitters in Slave mode.

10.2.1.1 I2S Master Mode Transmitter Timing



T = Clock period.
T_r = Minimum allowed clock period for the transmitter.
$T > T_r$.

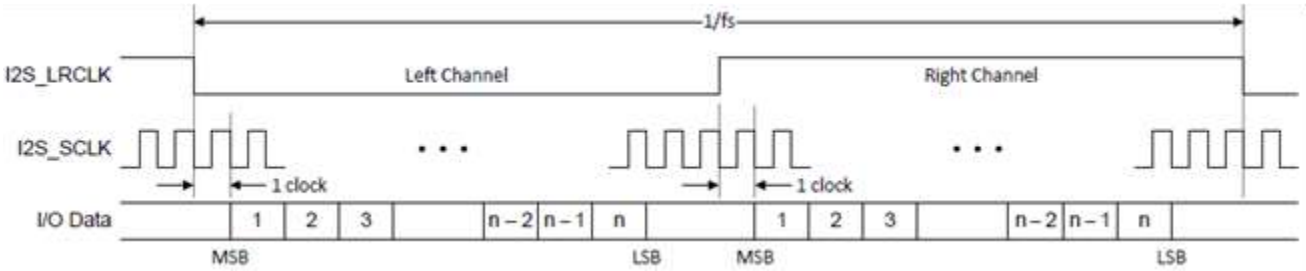
Parameter	Transmitter				Receiver	
	Lower Limit		Upper Limit		Lower Limit	
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum
Clock Period T	T_{tr}					
Slave mode: Clock		0.35 T_r				0.35 T_r
HIGH. t_{HC}		0.35 T_r				0.35 T_r
Clock Low, t_{LC}			0.15 T_r			
Clock rise time, t_{RC}				0.8T		
Transmitter delay, t_{dtr}						
Transmitter Hold Time, t_{htr}	0					
Receiver setup time, t_{sr}						0.2 T_r
Receiver hold time, t_{hr}						0

Timing for I^2S Transmitters and Receivers

Parameter	Minimum	Typical	Maximum	units
Frequency range	1		40	MHz
Frequency accuracy (with respect to the XTAL frequency)		1		ppb
Tuning resolution		50		ppb
Tuning range		1000		ppm
Tuning step size			10	ppm
Tuning rate		1		ppm/ms
Baseband jitter (100 Hz to 40 kHz)			100	ps rms
Wideband jitter (100 Hz to 1 MHz)			200	ps rms

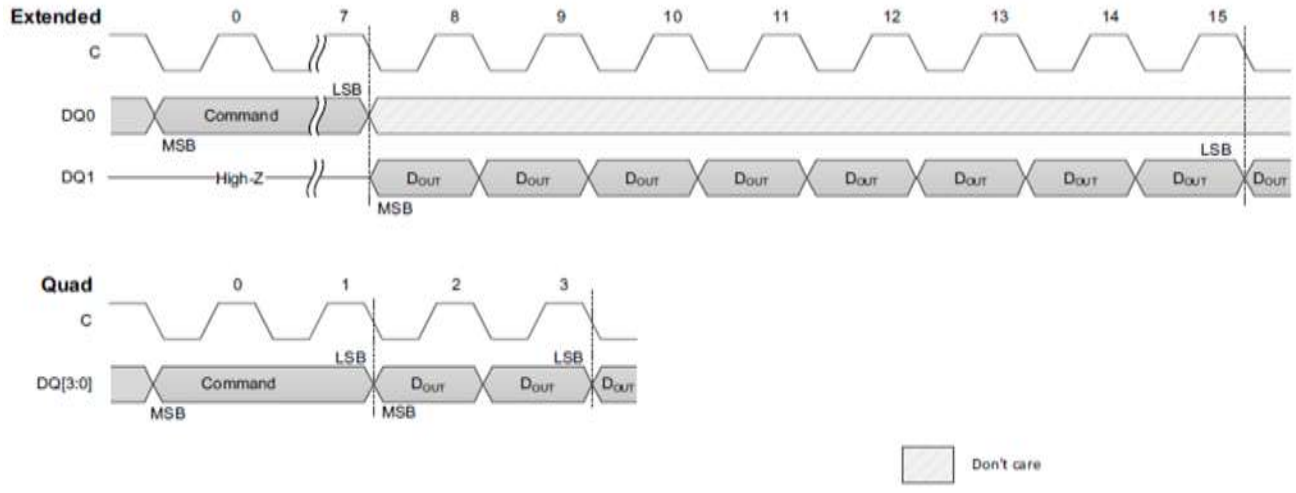
I2S_MCLK Specification

10.2.2 I2S Frame-Level Timing



10.2.3 SPI Flash Timing

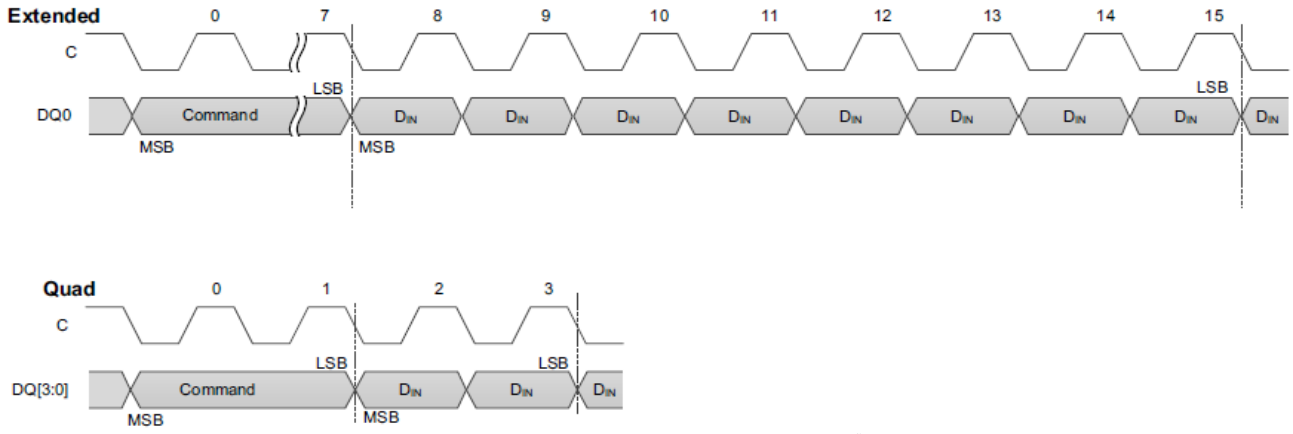
10.2.3.1 Read-Register Timing



Notes:
1. All Read Register commands except Read Lock Register are supported.
2. A Read Nonvolatile Configuration Register operation will output data starting from the least significant byte.

10.2.3.2 Write-Register Timing

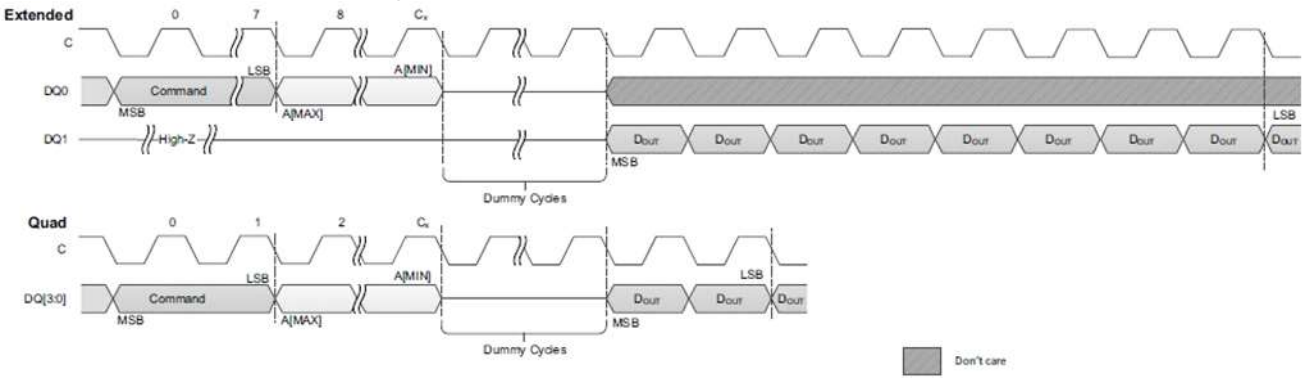
The SPI flash extended and quad write-register timing is show in below



Notes:
1. All write-register commands except Write Lock Register are supported.
2. The waveform must be extended for each protocol: to 23 for extended and five for quad.
3. A Write Nonvolatile Configuration Register operation requires data sent starting from the least significant byte.

10.2.3.3 Memory Fast-Reading Timing

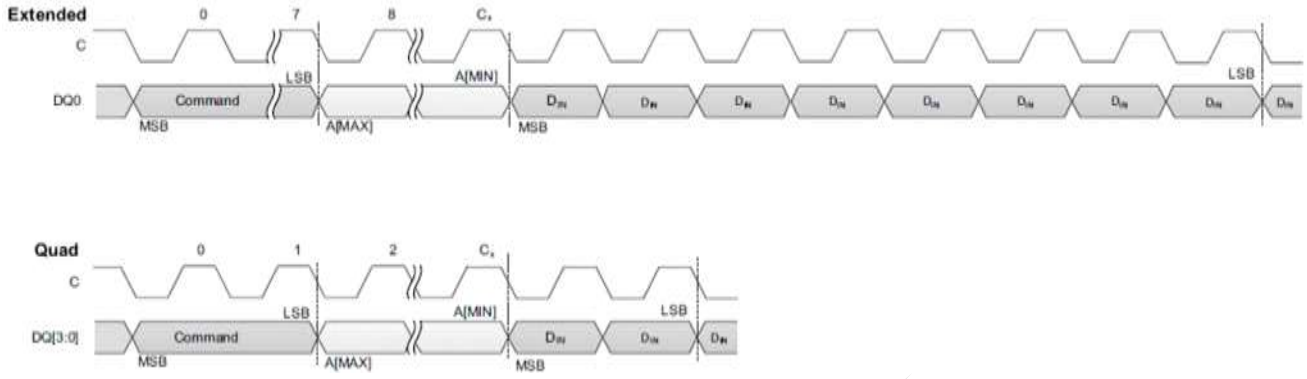
The SPI flash extended and quad memory fast-read timing is show in below



Notes:
1. 24-bit addressing is used, so A[MAX] = A[23] and A[MIN] = A[0].
2. For an extended SPI protocol, Cx = 7 + (A[MAX] + 1)
3. For a quad SPI protocol, Cx = 1 + (A[MAX] + 1)/4.

10.2.3.4 Memory Fast-Write Timing

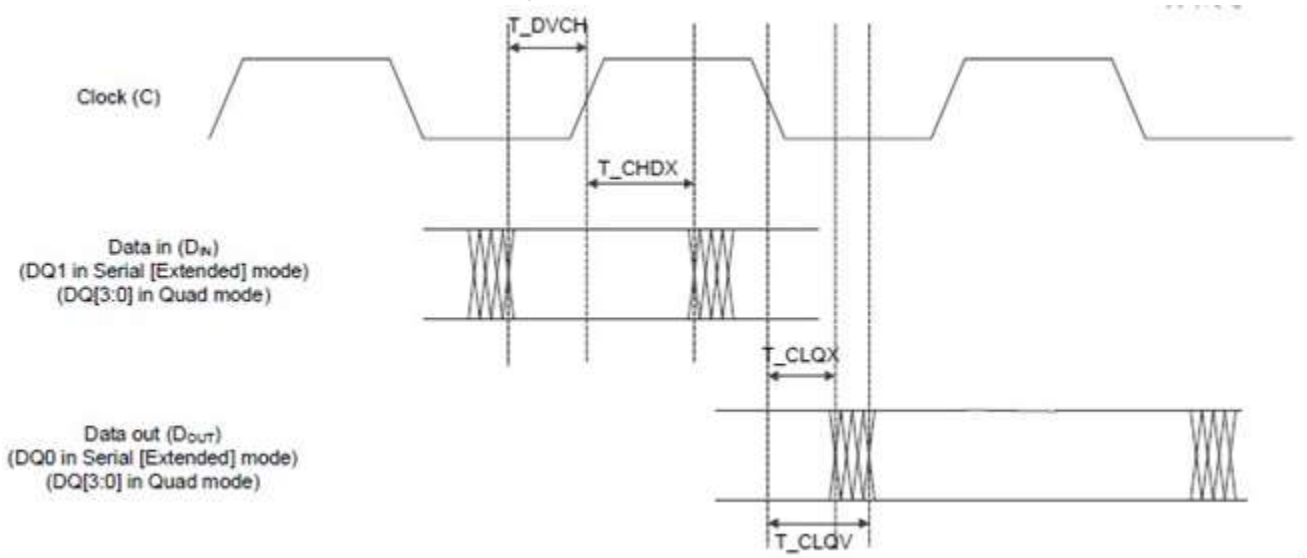
The SPI flash extended and quad memory-write (Page Program) timing is show in below



Notes:
1. For an extended SPI protocol, Cx = 7 + (A[MAX] + 1)
2. For a quad SPI protocol, Cx = 1 + (A[MAX] + 1)/4.

10.2.3.5 SPI Flash Parameters

The SPI flash timing parameters is show in below



Parameter	Description	Minimum	Maximum	Units
T_DVCH	Data setup time	2		ns
T_CHDX	Data hold time	3		ns
T_CLQX	Output hold time	1		ns
T_CLQV	Output valid time (With a 10pF load)		5	ns

10.2.4 USB PHY Electrical Characteristics and Timing

10.2.4.1 USB 2.0 and USB 1.1 Electrical Characteristics and Timing

The USB 2.0 and USB 1.1 Electrical Characteristics and Timing parameters are shown below

Parameter	Symbol	Minimum	Typical	Maximum	Units	Conditions
Baud rate	B_{ps}		480		Mbps	
Unit interval	UI		2083		ps	
Receiver – HS Mode						
Differential input voltage sensitivity	V_{HSDI}	300			mV	Static | V_{IDP}-V_{IDN}|
Input common mode voltage range	V_{HSCM}	-50		500	mV	
Receiver jitter tolerance	T_{HSRX}	-0.15		0.15	UI	
Input impedance	R_{IN}	40.5	45	49.5		Single ended
Transmitter – HS Mode						
Output high voltage	V_{HSDI}	360	400	440	mV	Static condition
Output low voltage	V_{HSCM}	-10	0	10	mV	Static condition
Output rise time	T_{HSR}	500			ps	10% to 90%
Output fall time	T_{HSF}	500			ps	90% to 10%
Transmitter jitter	T_{HSRX}	-0.05		0.05	UI	Transmit output jitter
Output impedance	R_o	40.5	45	49.5		Single ended
Chip-J output voltage (differential)	CHIRPJ	700		1100	mV	HS termination disabled 1.5K +/- 5% pull-up resistor connected.
Chip-K Output voltage (differential)	V_{CHIRPK}	-900		-500		HS termination disabled 1.5K +/- 5% pull-up resistor connected.

USB 2.0 Electrical and Timing Parameters

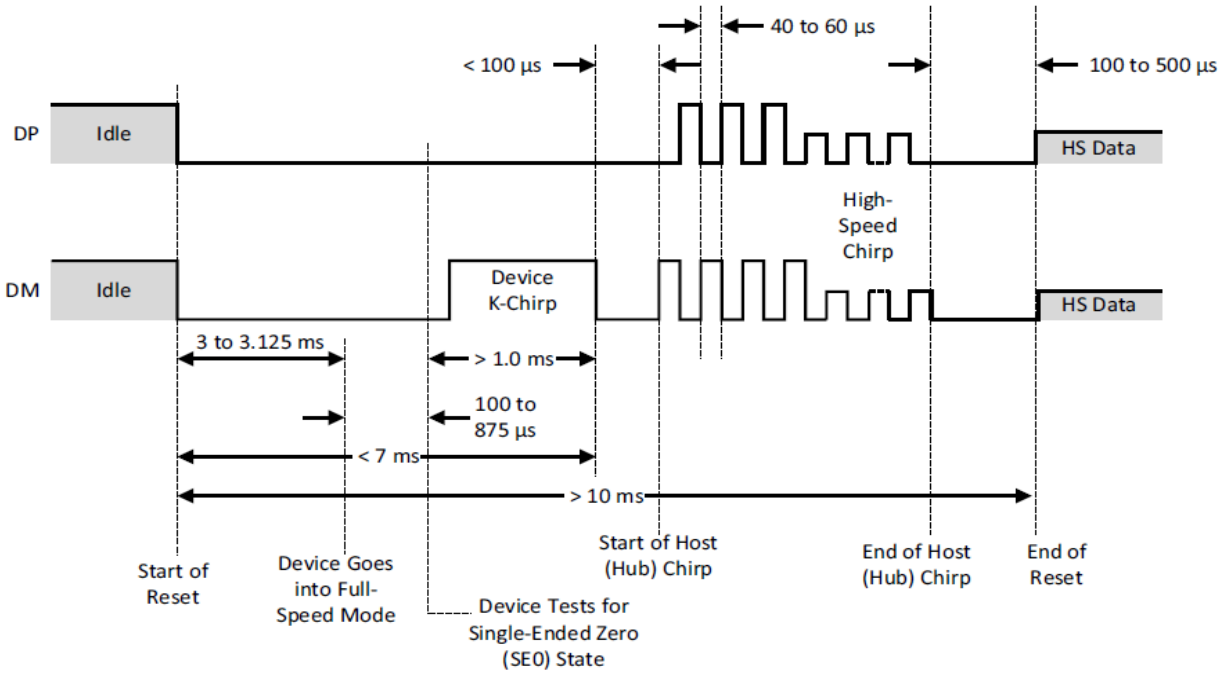
Parameter	Symbol	Minimum	Typical	Maximum	Units	Conditions
Baud rate						
FS	B_{ps}		12		Mbps	
LS	B_{ps}		1.5		Mbps	
Unit Interval						
FS	UI		83.33		ns	
LS	UI		666.67		ns	
Receiver						
Differential input sensitivity	V_{FSDI}	200			mV	Static | V_{IDP}-V_{IDN}|
Input common mode range	V_{FSCM}	0.8		2.5	V	
Input impedance	Z_{IN}	300			k	
Input high voltage	V_{FSIH}	2.0			V	Static
Input low voltage	V_{FSIL}			0.8	V	Static
Transmitter						
Output high voltage	V_{FSOH}	2.8			V	Static
Output low voltage	V_{FSOL}			0.3	V	Static
Output rise/fall time for fast speed	T_R ,T_F	4		20	ns	10% to 90%
Output rise/fall time for low speed	T_R ,T_F	75		300	ns	10% to 90%
Fast-speed jitter	$_{FSTX}$	-2		2	ns	
Low-speed jitter	$_{LSTX}$	-25		25	ns	
Output impedance	R_o	28		44		Single ended

USB 1.1 FS/LS Electrical and Timing Parameters (a)

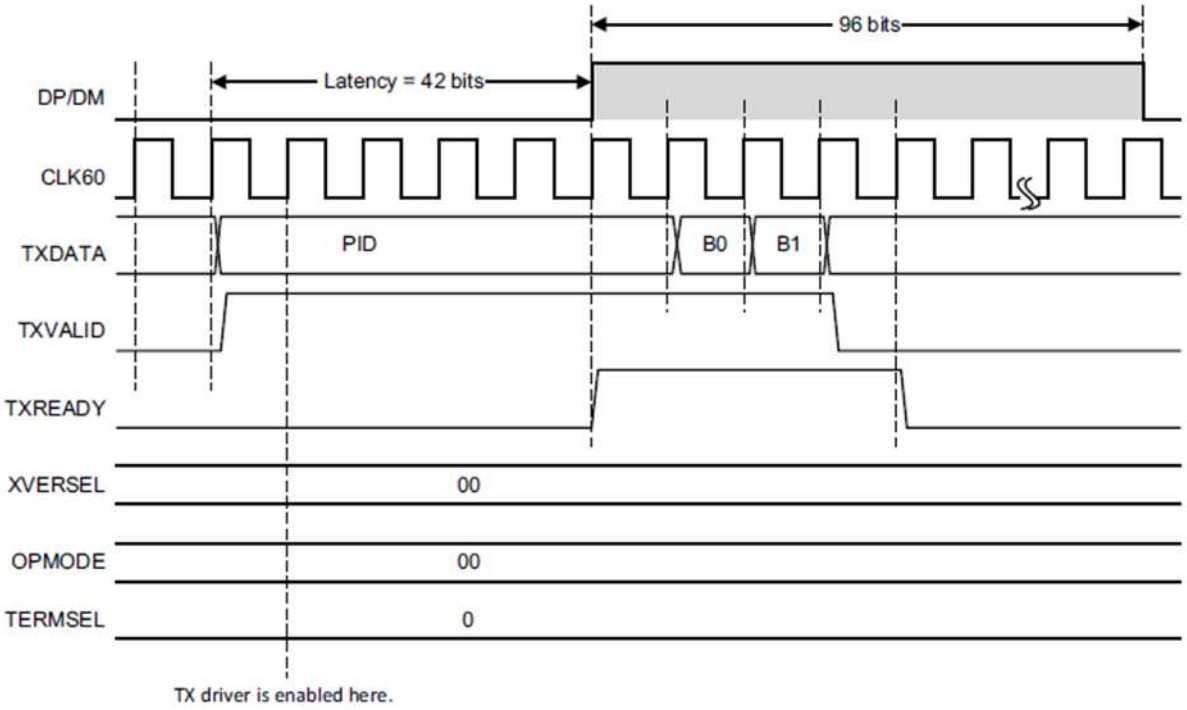
(a.) : For more details, refer to the USB 1.1 Specification.

10.2.4.2 USB 2.0 Timing Diagrams

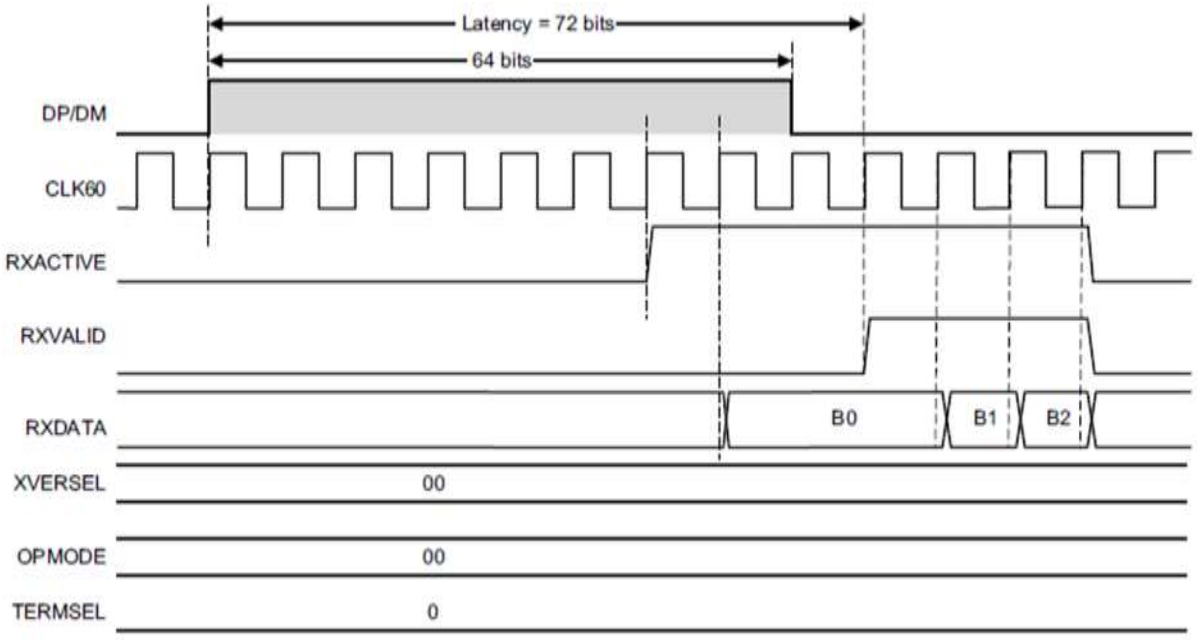
The important timing parameters associated with a post-reset transition to high-speed (HS) operation is show in below:



USB 2.0 Bus Reset to High-Speed Mode Operation



USB 2.0 High-Speed Mode Transmit Timing



USB 2.0 High-Speed Mode Receive Timing.

11 Mechanical Specification

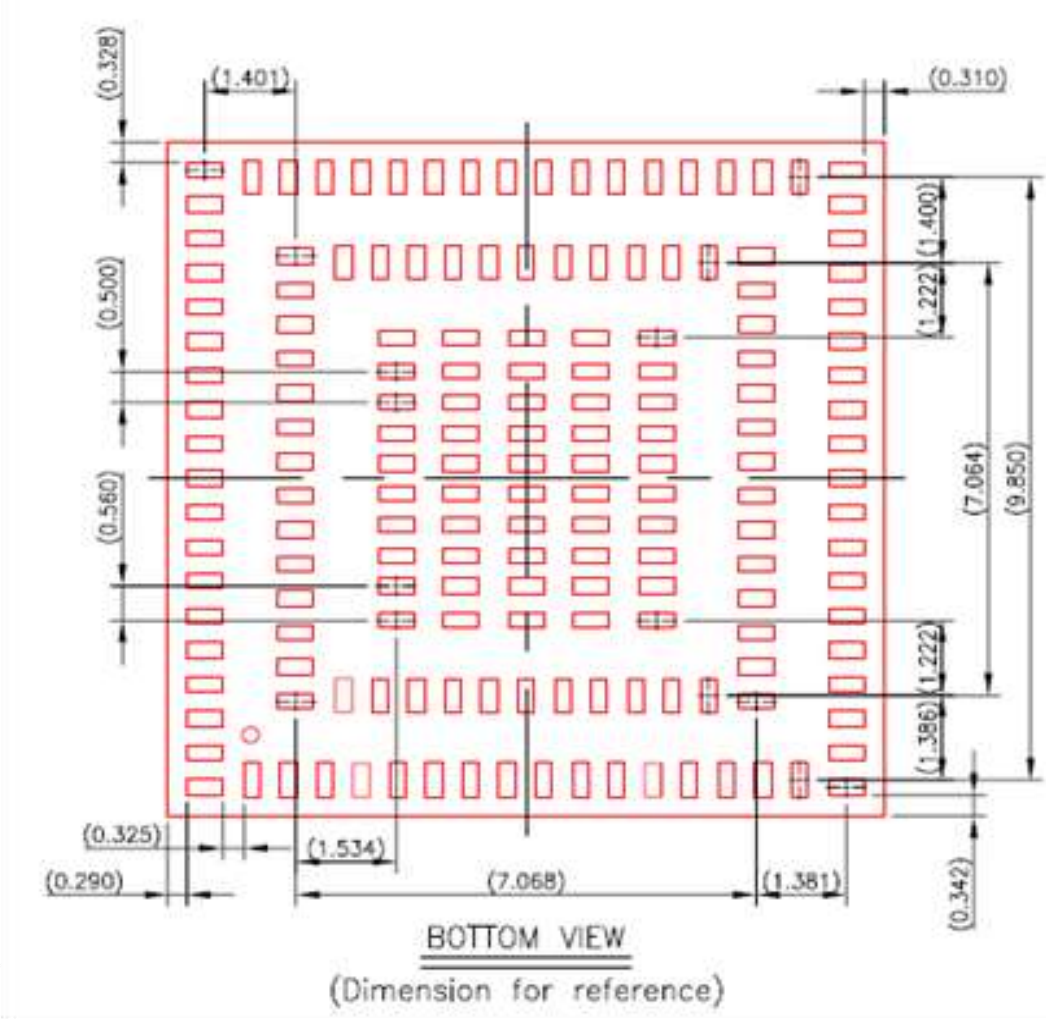
11.1 Size of the SiP

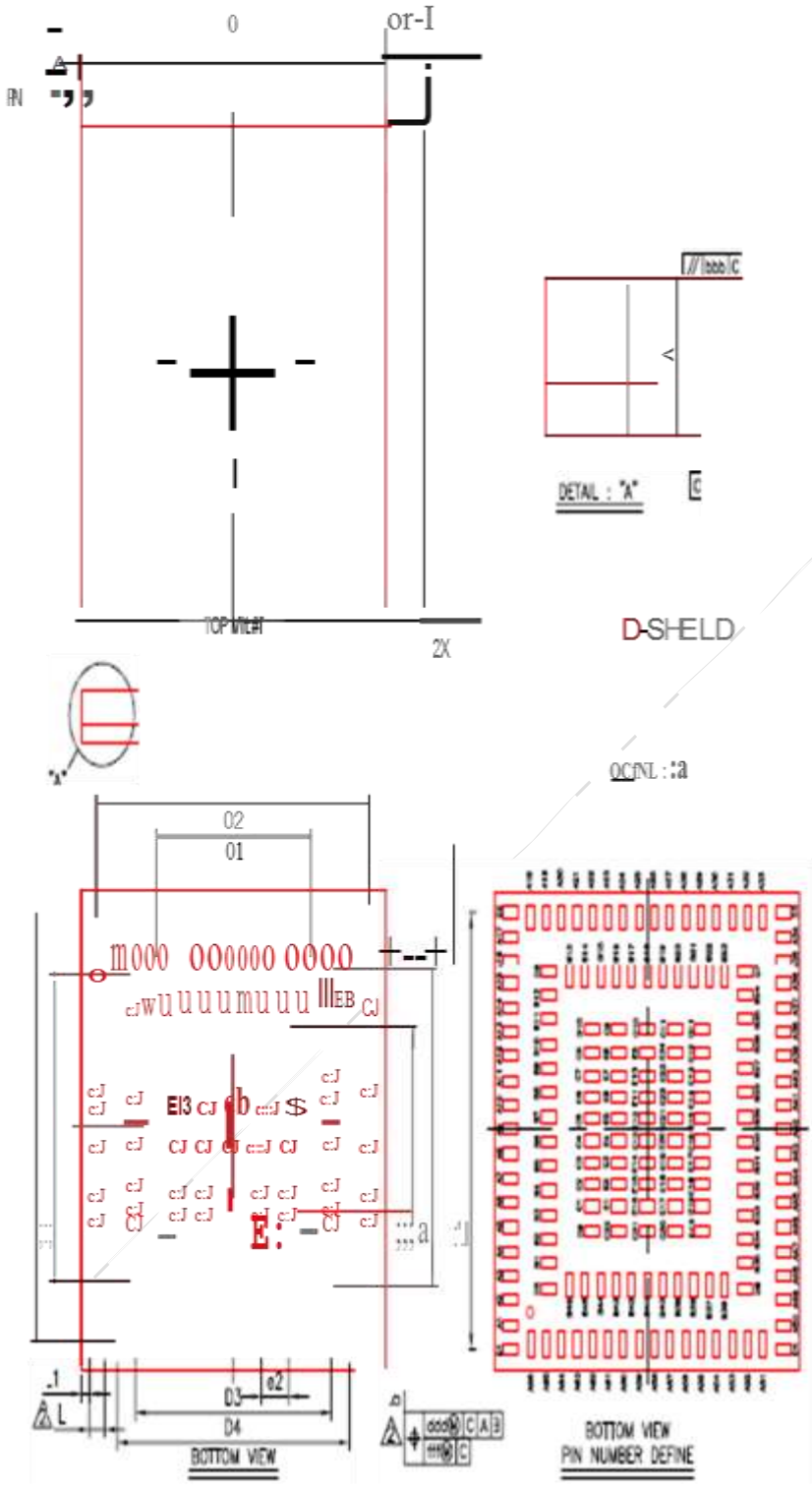
The following paragraphs provide the requirements for the size and weight of the ISM43907-L170.

The size and thickness of the ISM43907-L170 SiP is 11mm (W) x 11mm (L) x 1.2mm (H): (Tolerance: +/- 0.1mm)

11.2 Mechanical Dimension

Dimension: 11 x 11 x 1.2 mm3





symb-01	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.14	1.20	1.26	0.045	0.047	0.050
c	0.36	0.40	0.44	0.014	0.016	0.017
D	10.30	11.00	11.10	0.429	0.433	0.437
D1	---	4.00	---	---	0.157	---
D2	-	5.60			0.220	
D3	-	7.07			0.278	
D4	-	8.40			0.331	
E1		4.62			0.182	
E2	---	7.28	---	---	0.287	---
E3	---	10.08	---	---	0.397	---
E4	---	7.06	---	---	0.278	---
e1	---	0.56	---	---	0.022	---
e2	---	1.00	---	---	0.039	---
b	0.20	0.25	0.30	0.008	0.010	0.012
L	0.50	0.55	0.60	0.020	0.022	0.024
L1	---	0.29	---	---	0.011	---
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.10			0.004	
fff		0.05			0.002	

NOTE:

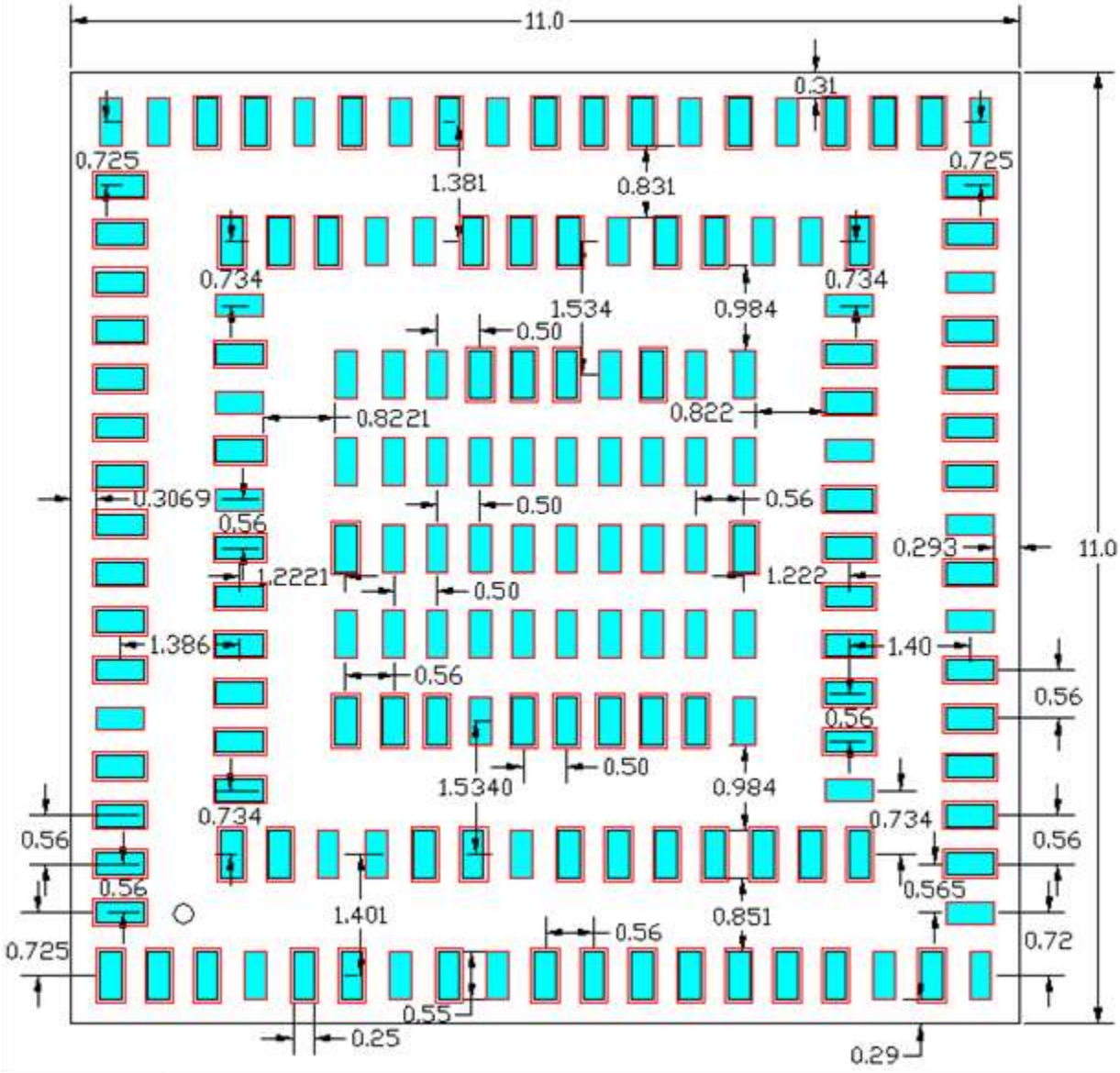
1. CONTROLLING DIMENSION : MILLIMETER
   DIMENSION b,L IS MEASURED

   AT THE MAXIMUM OPENING DIAMETER,

   PARALLEL TO PRIMARY DATUM C.

11.3 Recommended Footprint (Board Design)

11.3.1 Module Dimension Measurement Unit: mm

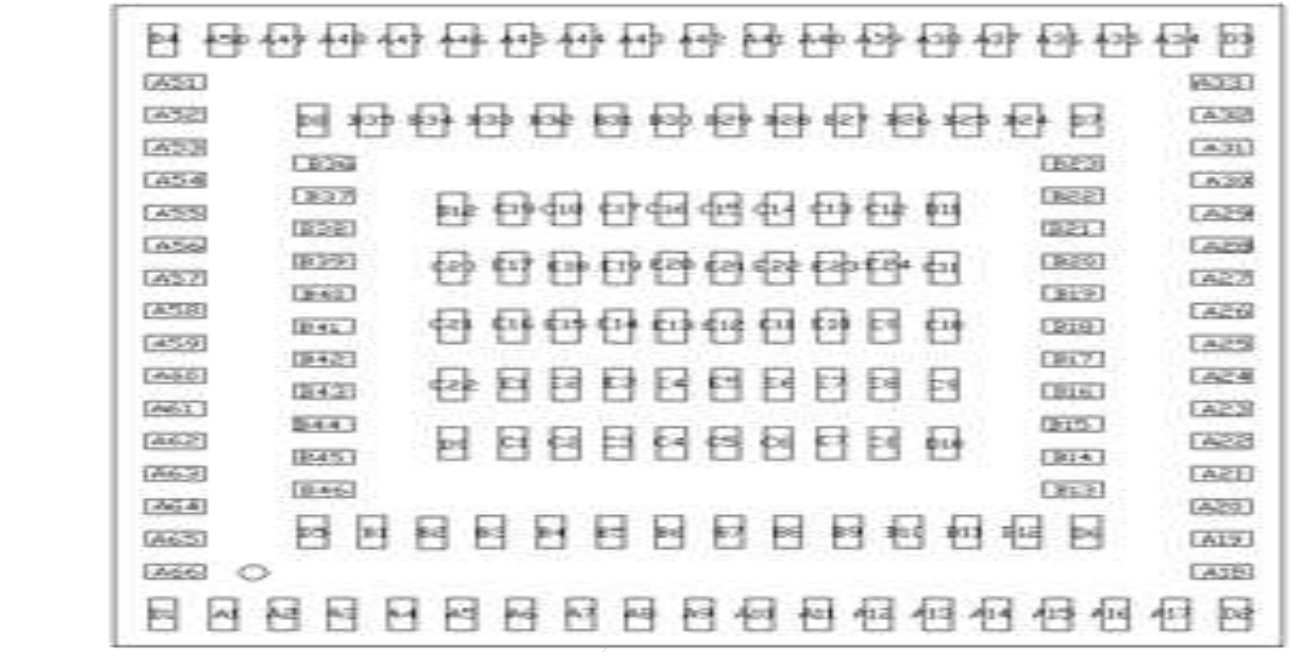


Note:
i.Solder Mask = 0.35mm x 0.65mm
ii.Pin = 0.25mm x 0.55mm
iii.Solder Paste = 0.25mm x 0.55mm

For PINs on the board that have a copper pour (flood) associated with it, usually the case with Ground PINs, please assure that the Land Pattern (PCB Footprint) for these PINs becomes Solder Mask Defined (SMD).
In other words, the SOLDERMASK for these Ground (GND) pins should be 0.550 mm x 0.250 mm (basically SODLERMASK becomes same size as the PIN).

11.3.2 The X-Y Central Location Coordinates

Unit: mm (Drawn dimensions with chip 0,0 at bottom right corner)



PIN_NUMBER	PAD_Size (mm^2)	Solder Mask_Size	PIN_X(mm)	PIN_Y(mm)
D1	0.25 x 0.55	0.35 x 0.65	0.467	0.565
A1	0.25 x 0.55	0.35 x 0.65	1.027	0.565
A2	0.25 x 0.55	0.35 x 0.65	1.587	0.565
A3	0.25 x 0.55	0.25 x 0.55	2.147	0.565
A4	0.25 x 0.55	0.35 x 0.65	2.707	0.565
A5	0.25 x 0.55	0.35 x 0.65	3.267	0.565
A6	0.25 x 0.55	0.25 x 0.55	3.827	0.565
A7	0.25 x 0.55	0.35 x 0.65	4.387	0.565
A8	0.25 x 0.55	0.25 x 0.55	4.947	0.565
A9	0.25 x 0.55	0.35 x 0.65	5.507	0.565
A10	0.25 x 0.55	0.35 x 0.65	6.067	0.565
A11	0.25 x 0.55	0.35 x 0.65	6.627	0.565
A12	0.25 x 0.55	0.35 x 0.65	7.187	0.565

A13	0.25 x 0.55	0.35 x 0.65	7.747	0.565
A14	0.25 x 0.55	0.35 x 0.65	8.307	0.565
A15	0.25 x 0.55	0.35 x 0.65	8.867	0.565
A16	0.25 x 0.55	0.25 x 0.55	9.427	0.565
A17	0.25 x 0.55	0.35 x 0.65	9.987	0.565
D2	0.25 x 0.55	0.25 x 0.55	10.547	0.565
A18	0.25 x 0.55	0.25 x 0.55	10.432	1.285
A19	0.25 x 0.55	0.35 x 0.65	10.432	1.85
A20	0.25 x 0.55	0.35 x 0.65	10.432	2.41
A21	0.25 x 0.55	0.35 x 0.65	10.432	2.97
A22	0.25 x 0.55	0.35 x 0.65	10.432	3.53
A23	0.25 x 0.55	0.35 x 0.65	10.432	4.09
A24	0.25 x 0.55	0.25 x 0.55	10.432	4.65
A25	0.25 x 0.55	0.35 x 0.65	10.432	5.21
A26	0.25 x 0.55	0.25 x 0.55	10.432	5.77
A27	0.25 x 0.55	0.35 x 0.65	10.432	6.33
A28	0.25 x 0.55	0.35 x 0.65	10.432	6.89
A29	0.25 x 0.55	0.35 x 0.65	10.432	7.45
A30	0.25 x 0.55	0.35 x 0.65	10.432	8.01
A31	0.25 x 0.55	0.25 x 0.55	10.432	8.57
A32	0.25 x 0.55	0.35 x 0.65	10.432	9.13
A33	0.25 x 0.55	0.35 x 0.65	10.432	9.69
D3	0.25 x 0.55	0.25 x 0.55	10.547	10.415
A34	0.25 x 0.55	0.35 x 0.65	9.987	10.415
A35	0.25 x 0.55	0.35 x 0.65	9.427	10.415
A36	0.25 x 0.55	0.35 x 0.65	8.867	10.415
A37	0.25 x 0.55	0.25 x 0.55	8.307	10.415
A38	0.25 x 0.55	0.35 x 0.65	7.747	10.415
A39	0.25 x 0.55	0.25 x 0.55	7.187	10.415
A40	0.25 x 0.55	0.35 x 0.65	6.627	10.415
A41	0.25 x 0.55	0.35 x 0.65	6.067	10.415
A42	0.25 x 0.55	0.35 x 0.65	5.507	10.415
A43	0.25 x 0.55	0.25 x 0.55	4.947	10.415
A44	0.25 x 0.55	0.35 x 0.65	4.387	10.415
A45	0.25 x 0.55	0.25 x 0.55	3.827	10.415
A46	0.25 x 0.55	0.35 x 0.65	3.267	10.415
A47	0.25 x 0.55	0.25 x 0.55	2.707	10.415
A48	0.25 x 0.55	0.35 x 0.65	2.147	10.415
A49	0.25 x 0.55	0.35 x 0.65	1.587	10.415

A50	0.25 x 0.55	0.25 x 0.55	1.027	10.415
D4	0.25 x 0.55	0.25 x 0.55	0.467	10.415

A51	0.25 x 0.55	0.35 x 0.65	0.5819	9.69
A52	0.25 x 0.55	0.35 x 0.65	0.5819	9.13
A53	0.25 x 0.55	0.35 x 0.65	0.5819	8.57
A54	0.25 x 0.55	0.35 x 0.65	0.5819	8.01
A55	0.25 x 0.55	0.35 x 0.65	0.5819	7.45
A56	0.25 x 0.55	0.35 x 0.65	0.5819	6.89
A57	0.25 x 0.55	0.35 x 0.65	0.5819	6.33
A58	0.25 x 0.55	0.35 x 0.65	0.5819	5.77
A59	0.25 x 0.55	0.35 x 0.65	0.5819	5.21
A60	0.25 x 0.55	0.35 x 0.65	0.5819	4.65
A61	0.25 x 0.55	0.35 x 0.65	0.5819	4.09
A62	0.25 x 0.55	0.25 x 0.55	0.5819	3.53
A63	0.25 x 0.55	0.35 x 0.65	0.5819	2.97
A64	0.25 x 0.55	0.35 x 0.65	0.5819	2.41
A65	0.25 x 0.55	0.35 x 0.65	0.5819	1.85
A66	0.25 x 0.55	0.35 x 0.65	0.5819	1.29
D5	0.25 x 0.55	0.35 x 0.65	1.867	1.966
B1	0.25 x 0.55	0.35 x 0.65	2.427	1.966
B2	0.25 x 0.55	0.25 x 0.55	2.9870	1.9625
B3	0.25 x 0.55	0.25 x 0.55	3.547	1.966
B4	0.25 x 0.55	0.35 x 0.65	4.107	1.966
B5	0.25 x 0.55	0.35 x 0.65	4.667	1.966
B6	0.25 x 0.55	0.25 x 0.55	5.227	1.966
B7	0.25 x 0.55	0.35 x 0.65	5.787	1.966
B8	0.25 x 0.55	0.35 x 0.65	6.347	1.966
B9	0.25 x 0.55	0.35 x 0.65	6.907	1.966
B10	0.25 x 0.55	0.35 x 0.65	7.467	1.966
B11	0.25 x 0.55	0.35 x 0.65	8.027	1.966
B12	0.25 x 0.55	0.35 x 0.65	8.587	1.966
D6	0.25 x 0.55	0.35 x 0.65	9.147	1.966
B13	0.25 x 0.55	0.25 x 0.55	9.032	2.7
B14	0.25 x 0.55	0.35 x 0.65	9.032	3.26
B15	0.25 x 0.55	0.35 x 0.65	9.032	3.82
B16	0.25 x 0.55	0.35 x 0.65	9.032	4.38
B17	0.25 x 0.55	0.35 x 0.65	9.032	4.94

PIN_NUMBER	PAD_Size (mm)		PIN_X(mm)	PIN_Y(mm)
B18	0.25 x 0.55	0.35 x 0.65	9.032	5.5
B19	0.25 x 0.55	0.35 x 0.65	9.032	6.06
B20	0.25 x 0.55	0.25 x 0.55	9.032	6.62
B21	0.25 x 0.55	0.35 x 0.65	9.032	7.18
B22	0.25 x 0.55	0.35 x 0.65	9.032	7.74
B23	0.25 x 0.55	0.25 x 0.55	9.032	8.3
D7	0.25 x 0.55	0.35 x 0.65	9.147	9.034
B24	0.25 x 0.55	0.25 x 0.55	8.587	9.034
B25	0.25 x 0.55	0.25 x 0.55	8.027	9.034
B26	0.25 x 0.55	0.35 x 0.65	7.467	9.034
B27	0.25 x 0.55	0.35 x 0.65	6.907	9.034
B28	0.25 x 0.55	0.25 x 0.55	6.347	9.034
B29	0.25 x 0.55	0.35 x 0.65	5.787	9.034
B30	0.25 x 0.55	0.35 x 0.65	5.227	9.034
B31	0.25 x 0.55	0.35 x 0.65	4.667	9.034
B32	0.25 x 0.55	0.25 x 0.55	4.107	9.034
B33	0.25 x 0.55	0.25 x 0.55	3.547	9.034
B34	0.25 x 0.55	0.35 x 0.65	2.987	9.034
B35	0.25 x 0.55	0.35 x 0.65	2.427	9.034
D8	0.25 x 0.55	0.35 x 0.65	1,867	9.034
B36	0.25 x 0.55	0.25 x 0.55	1.9679	8.3
B37	0.25 x 0.55	0.35 x 0.65	1.9679	7.74
B38	0.25 x 0.55	0.25 x 0.55	1.9679	7.18
B39	0.25 x 0.55	0.35 x 0.65	1.9679	6.62
B40	0.25 x 0.55	0.25 x 0.55	1.9679	6.06
B41	0.25 x 0.55	0.35 x 0.65	1.9679	5.5
B42	0.25 x 0.55	0.35 x 0.65	1.9679	4.94
B43	0.25 x 0.55	0.35 x 0.65	1.9679	4.38
B44	0.25 x 0.55	0.35 x 0.65	1.9679	3.82
B45	0.25 x 0.55	0.35 x 0.65	1.9679	3.26
B46	0.25 x 0.55	0.35 x 0.65	1.9679	2.7
D9	0.25 x 0.55	0.35 x 0.65	3.19	3.5
C1	0.25 x 0.55	0.35 x 0.65	3.75	3.5
C2	0.25 x 0.55	0.25 x 0.55	4.25	3.5

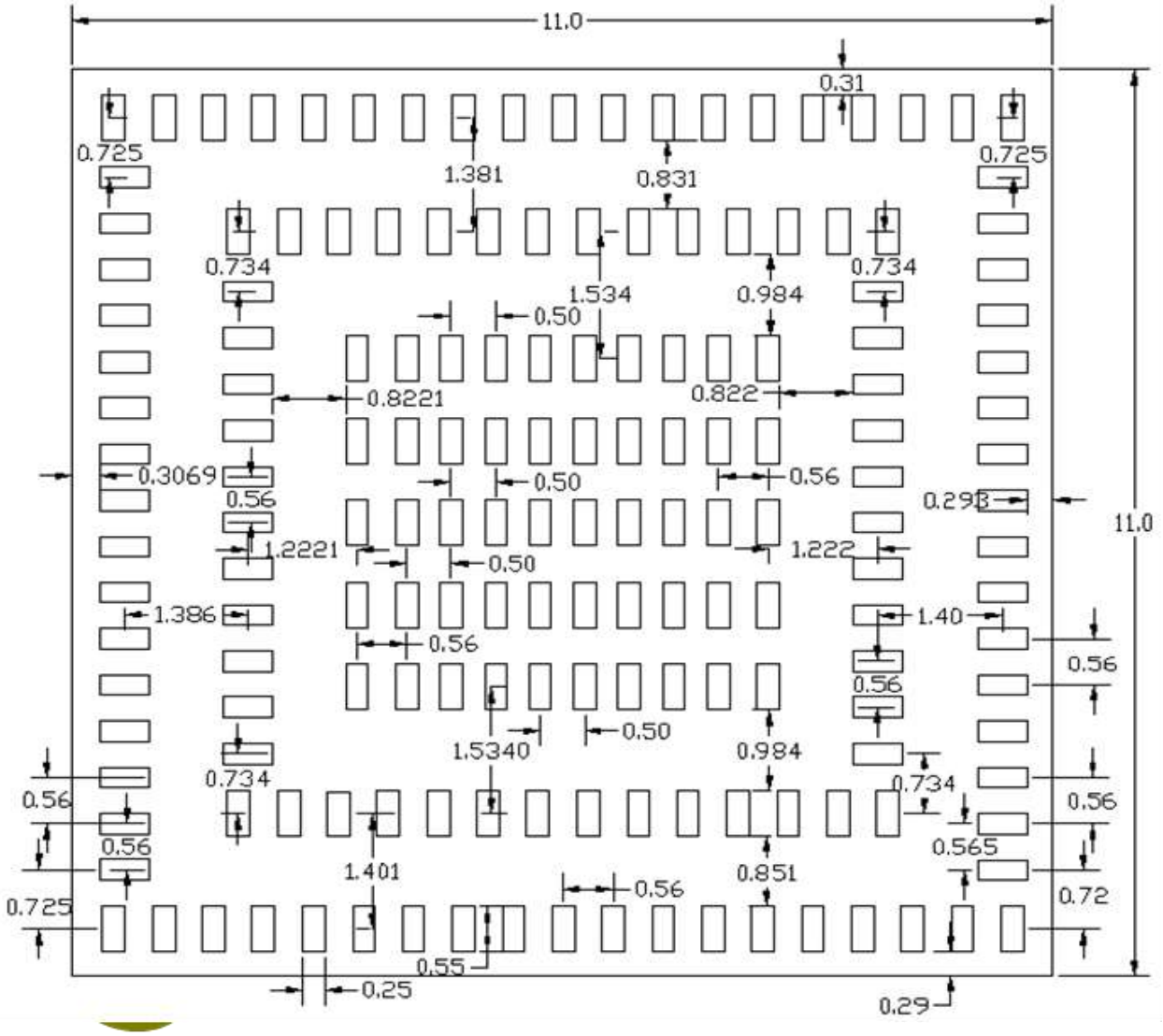
C3	0.25 x 0.55	0.35 x 0.65	4.75	3.5
C4	0.25 x 0.55	0.25 x 0.55	5.25	3.5

PIN_NUMBER	PAD_Size (mm)		PIN_X(mm)	PIN_Y(mm)
C5	0.25 x 0.55	0.35 x 0.65	5.75	3.5
C6	0.25 x 0.55	0.35 x 0.65	6.25	3.5
C7	0.25 x 0.55	0.35 x 0.65	6.75	3.5
C8	0.25 x 0.55	0.35 x 0.65	7.25	3.5
D10	0.25 x 0.55	0.25 x 0.55	7.81	3.5
C9	0.25 x 0.55	0.25 x 0.55	7.81	4.5
C10	0.25 x 0.55	0.35 x 0.65	7.81	5.5
C11	0.25 x 0.55	0.25 x 0.55	7.81	6.5
D11	0.25 x 0.55	0.25 x 0.55	7.81	7.5
C12	0.25 x 0.55	0.25 x 0.55	7.25	7.5
C13	0.25 x 0.55	0.35 x 0.65	6.75	7.5
C14	0.25 x 0.55	0.25 x 0.55	6.25	7.5
C15	0.25 x 0.55	0.35 x 0.65	5.75	7.5
C16	0.25 x 0.55	0.35 x 0.65	5.25	7.5
C17	0.25 x 0.55	0.35 x 0.65	4.75	7.5
C18	0.25 x 0.55	0.25 x 0.55	4.25	7.5
C19	0.25 x 0.55	0.25 x 0.55	3.75	7.5
D12	0.25 x 0.55	0.25 x 0.55	3.19	7.5
C20	0.25 x 0.55	0.25 x 0.55	3.19	6.5
C21	0.25 x 0.55	0.35 x 0.65	3.19	5.5
C22	0.25 x 0.55	0.25 x 0.55	3.19	4.5
E1	0.25 x 0.55	0.25 x 0.55	3.75	4.5
E2	0.25 x 0.55	0.25 x 0.55	4.25	4.5
E3	0.25 x 0.55	0.25 x 0.55	4.75	4.5
E4	0.25 x 0.55	0.25 x 0.55	5.25	4.5
E5	0.25 x 0.55	0.25 x 0.55	5.75	4.5
E6	0.25 x 0.55	0.25 x 0.55	6.25	4.5
E7	0.25 x 0.55	0.25 x 0.55	6.75	4.5
E8	0.25 x 0.55	0.25 x 0.55	7.25	4.5
E9	0.25 x 0.55	0.25 x 0.55	7.25	5.5
E10	0.25 x 0.55	0.25 x 0.55	6.75	5.5
E11	0.25 x 0.55	0.25 x 0.55	6.25	5.5
E12	0.25 x 0.55	0.25 x 0.55	5.75	5.5

E13	0.25 x 0.55	0.25 x 0.55	5.25	5.5
E14	0.25 x 0.55	0.25 x 0.55	4.75	5.5
E15	0.25 x 0.55	0.25 x 0.55	4.25	5.5
E16	0.25 x 0.55	0.25 x 0.55	3.75	5.5
E17	0.25 x 0.55	0.25 x 0.55	3.75	6.5
E18	0.25 x 0.55	0.25 x 0.55	4.25	6.5
E19	0.25 x 0.55	0.25 x 0.55	4.75	6.5
E20	0.25 x 0.55	0.25 x 0.55	5.25	6.5
E21	0.25 x 0.55	0.25 x 0.55	5.75	6.5
E22	0.25 x 0.55	0.25 x 0.55	6.25	6.5
E23	0.25 x 0.55	0.25 x 0.55	6.75	6.5
E24	0.25 x 0.55	0.25 x 0.55	7.25	6.5

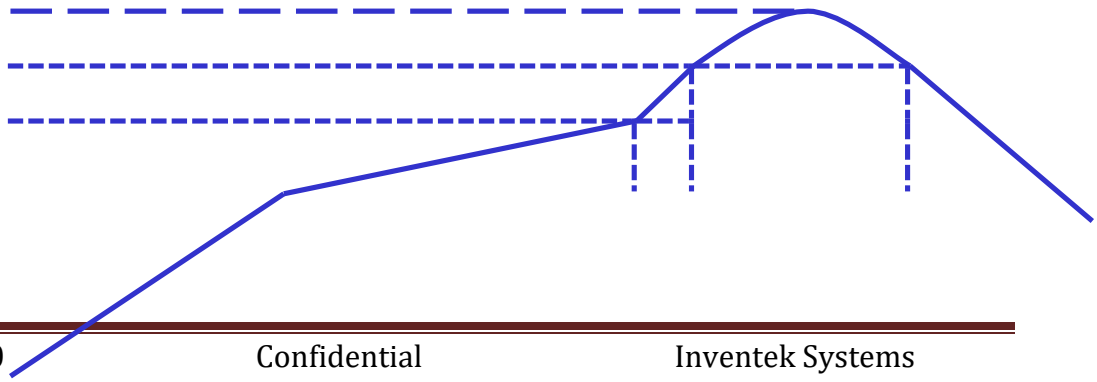
11.3.3 Recommended Stencil (Unit: mm)

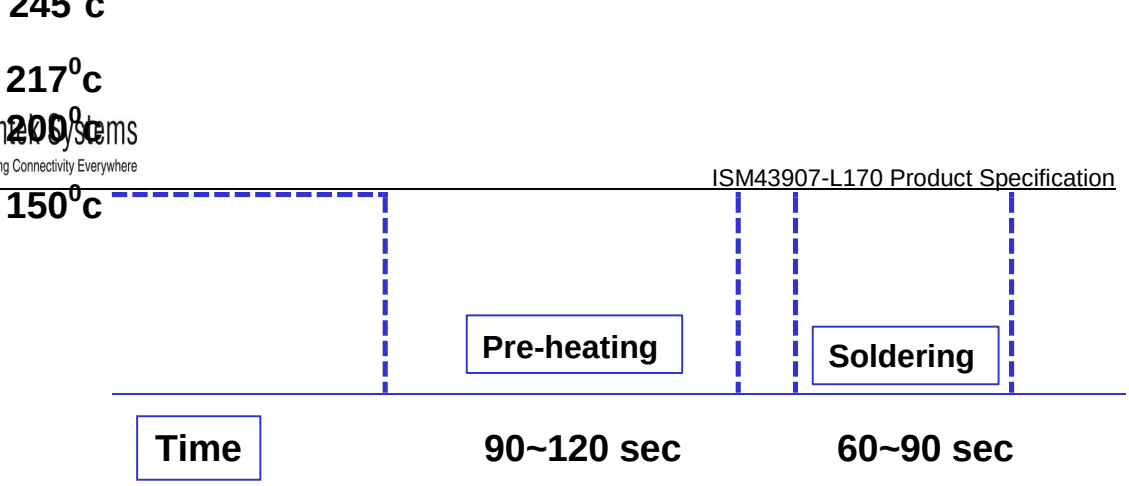
Top View:



11.3.4 Recommended Reflow Profile

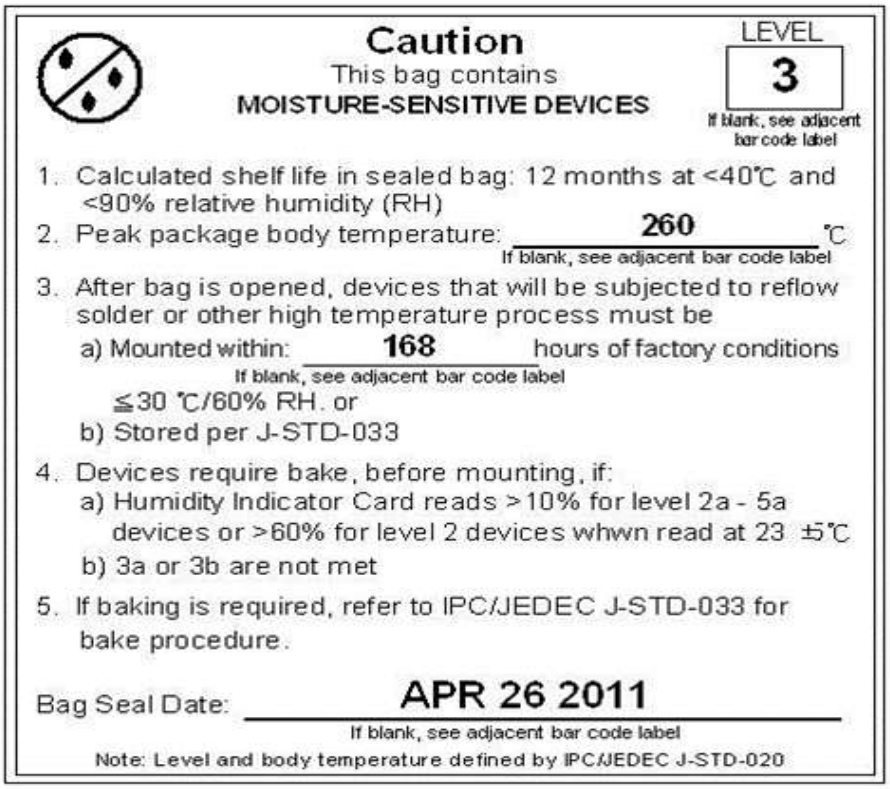
Temperature





12 Packaging Information

12.1 MSL & Moisture Sensitive Level



12.2 Device baking requirements prior to assembly

Boards must be baked prior to rework or assembly to avoid damaging moisture sensitive components during localized reflow. The default bake cycles is 24 hours at 125C.
Maintaining proper control of moisture uptake in components is critical.
Before opening the shipping bag and attempting solder reflow, you should maintain a minimal out-of-bag time and ensure the highest possible package reliability for the final product.

13 REVISION CONTROL

Document: ISM43907-L170	802.11a/b/g/n Wi-Fi SiP module
External Release	DOC-DS-2017-1.0

Date	Author	Revision	Comment
2/17/2016	AS	1.0	Preliminary
3/08/2016	AS	1.0.1	Electrical Parameters Update
6/23/2016	AS	1.1	I2S & SPI updates
10/03/2016	AS	1.8	Final Preliminary
2/17/17	AS	2.0	Release

14 CONTACT INFORMATION

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