KSZ9893RNX

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for KSZ9893RNX. These checklist items should be followed when utilizing the KSZ9893RNX in a new board design.

A summary of the hardware design checklist items is provided in Section 12.0, "Hardware Checklist Summary," on page 30. Detailed information on each checklist item can be found in the following corresponding sections:

A listing of available KSZ9893RNX hardware design collaterals can be found in Section 11.0, "Reference Materials," on page 29.

2.0 PACKAGE AND PIN CONSIDERATIONS

2.1 Package Orientation and Pin Numbering

Check to ensure the package orientation and pin numbering with respect to top view of package are in the counterclockwise direction. Refer to the *KSZ9893RNX Data Sheet* for additional information.

2.2 Pin Type

Check the pin-outs of the KSZ9893RNX device to ensure all pin types and directions match the *KSZ9893RNX Data Sheet* and the interfacing devices are configured with corresponding input, output, or bidirectional pin types for schematic design rule error checking.

It is important to always check the pin types in the data sheet of the connecting pins between two devices to ensure the adjoining pins are not both inputs and not both outputs. Do not rely on just the pin name of the bus interface between two connecting devices. The same pin name may be defined as an input or an output depending on the interface perspective. This is especially for the RGMII, RMII, and MII pins, as defined from the PHY perspective or MAC perspective.

2.3 Configuration Strap Pins

The KSZ9893RNX utilizes configuration strap pins to configure the device for different modes. These strap pins are configured by using internal and external pull-up/pull-down resistors to create a High or Low state on the pins which are sampled at the end of a device power-up or software reset cycle. They are also latched when powering-up from a hardware or software power-down or Hardware Reset state (rising edge of **RESET_N**).

In some systems, for example, the connecting MAC input pins may drive high during power-up or reset and consequently cause the multiplexed strap-in pins on the RGMII/RMII/MII signals to be latched high instead of low. In this case, it is recommended to add 1K pull-downs to these strap-in pins to ensure they latch low.

Check to ensure proper external pull-ups or pull-downs, as needed, are installed for all the strap pins as defined in the *KSZ9893RNX Data Sheet.*

3.0 REFERENCE CLOCK CIRCUITS AND CONNECTIONS

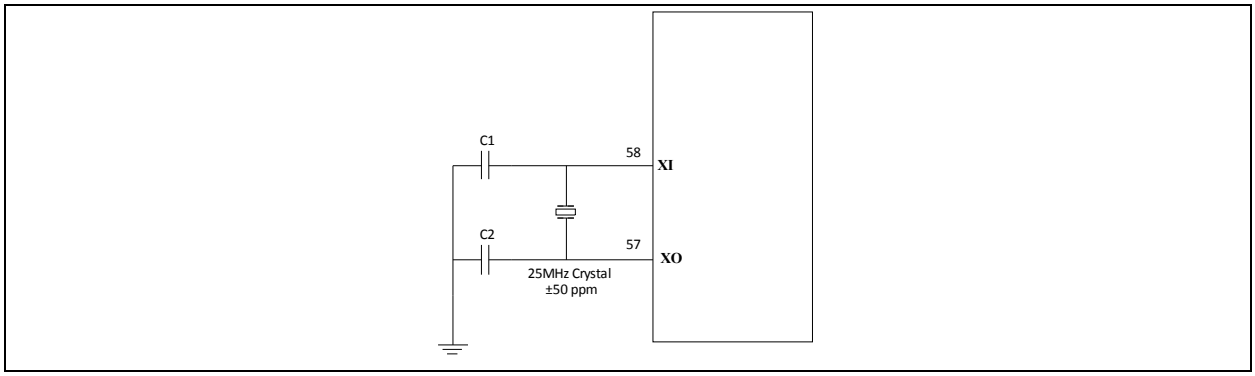
A crystal or external clock source can be used to generate the 25 MHz reference clock for the device.

3.1 Crystal Circuit

The following notes for the crystal circuit refer to Figure 3-1:

- A 25.000 MHz (±50 ppm) crystal is recommended. Refer to the latest version of the *KSZ9893RNX Data Sheet*.
- **XI** (pin 58) is the crystal circuit input. This pin connects to one side of the crystal as well as a capacitor to ground.
- **XO** (pin 57) is the clock circuit output. This pin connects to the other side of the crystal and also connects to a capacitor to ground.
- The external capacitor value for the crystal can vary and depends on the CL specifications of the selected crystal and the stray capacitance of the PCB traces.
- The selected crystal and PCB design and layout contribute to the performance of the crystal circuit. Once the board is brought up and is operational, a check for frequency accuracy and stability across the system operating conditions is recommended.

FIGURE 3-1: CRYSTAL CIRCUIT

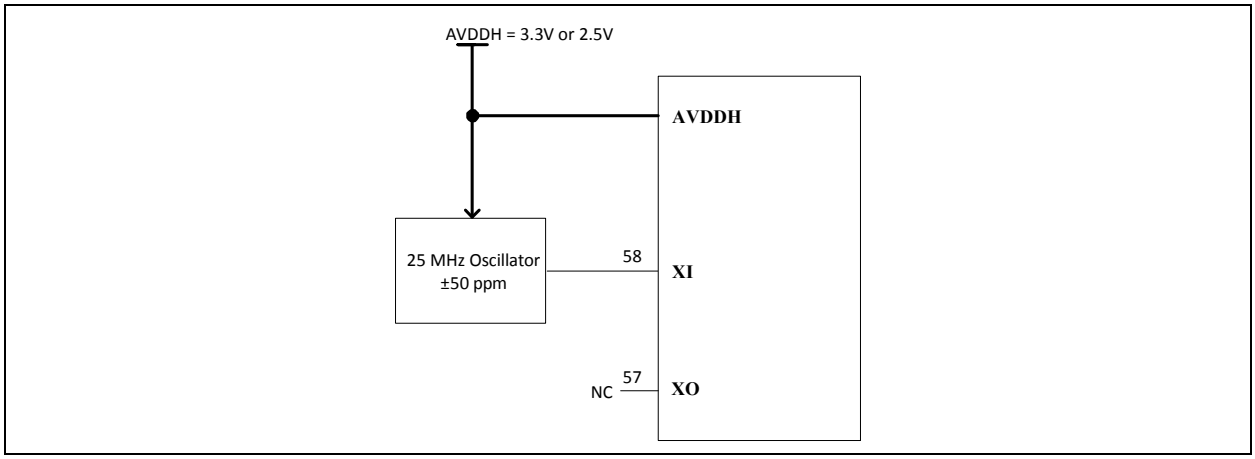


3.2 External Clock Source/Oscillator Circuit

The following notes for the external clock/oscillator circuit refer to Figure 3-2:

- An external 25.000 MHz (±50 ppm) clock source, such as an oscillator, with a Total Period Jitter (peak-to-peak) of less than 100 ps is recommended. Refer to the latest version of the *KSZ9893RNX Data Sheet*.
- **XI** (pin 58) is the input for the external clock source. A 22-ohm-to-50-ohm series source termination at the clock output pin is recommended.
- **XO** (pin 57) is a no connect.
- The external clock source should reference the AVDDH voltage level supplied to the KSZ9893RNX device.

FIGURE 3-2: EXTERNAL CLOCK SOURCE/OSCILLATOR CIRCUIT

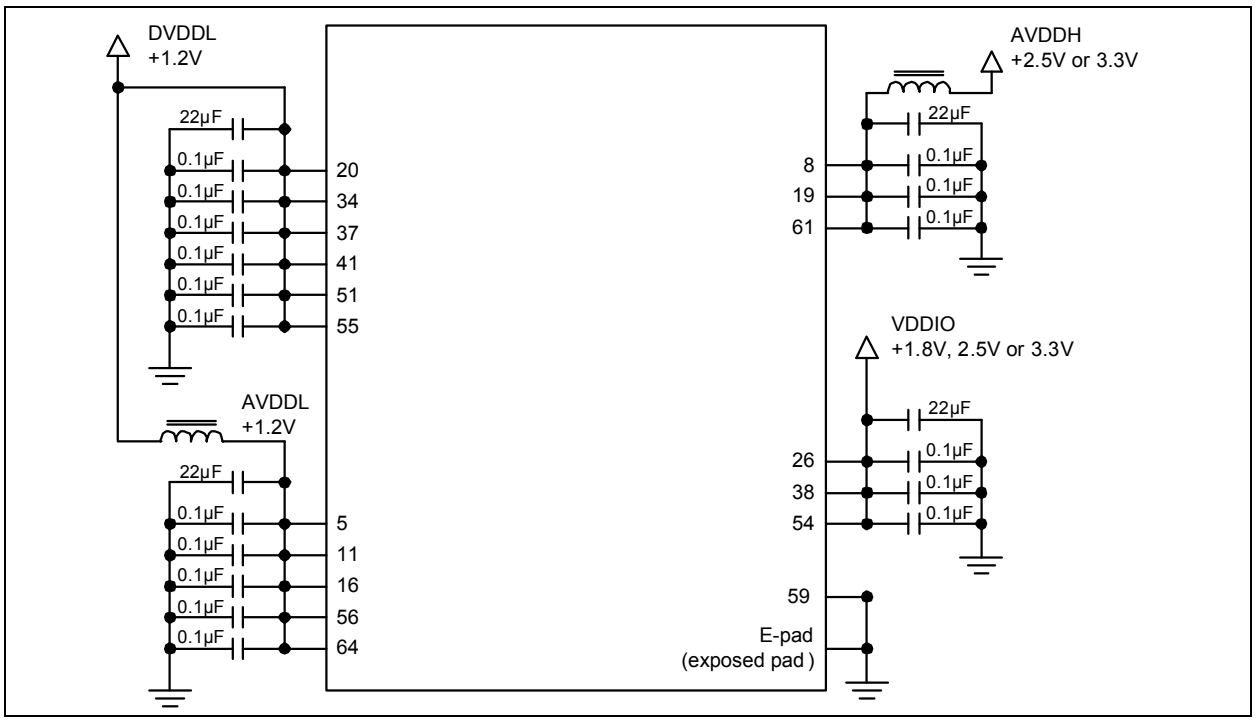


4.0 POWER/GROUND CONNECTIONS

4.1 Power and Ground Block Diagram

The power and ground connections are shown in Figure 4-1.

FIGURE 4-1: POWER AND GROUND CONNECTIONS



4.1.1 POWER PINS

The following notes for the power pins and their connections refer to Figure 4-1:

- **VDDIO** powers the digital I/O pins and can operate at either +3.3V, +2.5V, or +1.8V.
- **AVDDH** powers the analog transceiver, can operate at either +3.3V or +2.5V for reduced power consumption, and should have a series ferrite bead placed between the board power supply to provide further filtering.
- **DVDDL** powers the digital core and operates at +1.2V.
- **AVDDL** powers the analog core and operates at +1.2V. If a single 1.2V board supply is used, a series ferrite bead should be placed between **DVDDL** power and **AVDDL** power to provide further filtering.
- Each power pin requires a 0.1 µF decoupling capacitor. These capacitors should be placed as close as possible to the power pins without using vias.
- The ferrite bead is typically 100Ω to 220Ω (at 100 MHz).
- A bulk capacitor should be placed on each power rail near the device. These capacitors should have a typical capacitance value of 22 µF and an Equivalent Series Resistance (ESR) of no more than 1Ω. Microchip recommends a very low ESR ceramic capacitor for design stability.
- All four power rails (**VDDIO**, **AVDDH**, **DVDDL**, and **AVDDL**) should have less than 50 mVp-p ripple each.

4.1.2 GROUND PIN AND EXPOSED PAD

The following notes for the ground pin, the exposed pad ground, and their connections refer to Figure 4-1:

- Ground pin 59 should connect directly to the solid ground plane on the board.
- Exposed pad (E-pad) ground on the bottom side of the chip should connect directly to the solid ground plane on the board. See device data sheet for the E-pad dimensions, recommended land pattern and thermal via size, and number requirements.
- All ground connections, ground pin 59, and the E-pad should tie directly together to the same ground plane. Separate ground planes are not recommended.

5.0 ISET RESISTOR

The **ISET** pin of the KSZ9893RNX should connect to signal ground through a 6.04 kΩ 1.0% resistor. The resistor value sets the bias currents to generate the 10BASE-T/100BASE-TX/1000BASE-T transmit signal swing.

Some design guidelines for the ISET resistor:

- Place the resistor close to ISET pin of the device.
- Do not place any capacitor in parallel with the ISET resistor.
- Route all signals, especially clocks and high frequency signals, away from this pin to avoid coupling.
- Do not share the ISET resistor ground via with any other component's grounding via.

6.0 ETHERNET PHY PORTS

6.1 Ethernet Signal Pins

The KSZ9893RNX has Voltage-mode transmit drivers and on-chip terminations for its PHY differential pairs. No external termination is required for the four differential pairs for the two PHY ports.

The following are the PHY port 1 differential signals:

- **TXRX1P_A** (pin 62): This pin is the PHY port 1 differential pair A twisted pair positive connection. It is used for 10BASE-T/100BASE-TX/1000BASE-T speeds and connects the internal PHY to the external 10/100/100 magnetics.
- **TXRX1M_A** (pin 63): This pin is the PHY port 1 differential pair A twisted pair negative connection. It is used for 10BASE-T/100BASE-TX/1000BASE-T speeds and connects the internal PHY to the external 10/100/1000 magnetics.
- **TXRX1P_B** (pin 1): This pin is the PHY port 1 differential pair B twisted pair positive connection. It is used for 10BASE-T/100BASE-TX/1000BASE-T speeds and connects the internal PHY to the external 10/100/1000 magnetics.
- **TXRX1M_B** (pin 2): This pin is the PHY port 1 differential pair B twisted pair negative connection. It is used for 10BASE-T/100BASE-TX/1000BASE-T speeds and connects the internal PHY to the external 10/100/1000 magnetics.
- **TXRX1P_C** (pin 3): This pin is the PHY port 1 differential pair C twisted pair positive connection. It is used for 1000 BASE-T speed only and connects the internal PHY to the external 1000 magnetics. For 10BASE-T/100BASE-TX speeds only, this pin can be left as a no connect.
- **TXRX1M_C** (pin 4): This pin is the PHY port 1 differential pair C twisted pair negative connection. It is used for 1000BASE-T speed only and connects the internal PHY to the external 1000 magnetics. For 10BASE-T/100BASE-TX speeds only, this pin can be left as a no connect.
- **TXRX1P_D** (pin 6): This pin is the PHY port 1 differential pair D twisted pair positive connection. It is used for 1000BASE-T speed only and connects the internal PHY to the external 1000 magnetics. For 10BASE-T/100BASE-TX speeds only, this pin can be left as a no connect.
- **TXRX1M_D** (pin 7): This pin is the PHY port 1 differential pair D twisted pair negative connection. It is used for 1000BASE-T speed only and connects the internal PHY to the external 1000 magnetics. For 10BASE-T/100BASE-TX speeds only, this pin can be left as a no connect.

The following are the PHY port 2 differential signals:

- **TXRX2P_A** (pin 9): This pin is the PHY port 2 differential pair A twisted pair positive connection. It is used for 10BASE-T/100BASE-TX/1000BASE-T speeds and connects the internal PHY to the external 10/100/100 magnetics.
- **TXRX2M_A** (pin 10): This pin is the PHY port 2 differential pair A twisted pair negative connection. It is used for 10BASE-T/100BASE-TX/1000BASE-T10BASE-T/100BASE-TX/1000BASE-T speeds and connects the internal PHY to the external 10/100/1000 magnetics.
- **TXRX2P_B** (pin 12): This pin is the PHY port 2 differential pair B twisted pair positive connection. It is used for 10BASE-T/100BASE-TX/1000BASE-T speeds and connects the internal PHY to the external 10/100/1000 magnetics.
- **TXRX2M_B** (pin 13): This pin is the PHY port 2 differential pair B twisted pair negative connection. It is used for 10BASE-T/100BASE-TX/1000BASE-T speeds and connects the internal PHY to the external 10/100/1000 magnetics.
- **TXRX2P_C** (pin 14): This pin is the PHY port 2 differential pair C twisted pair positive connection. It is used for

1000BASE-T speed only and connects the internal PHY to the external 1000 magnetics. For 10BASE-T/100BASE-TX speeds only, this pin can be left as a no connect.

- **TXRX2M_C** (pin 15): This pin is the PHY port 2 differential pair C twisted pair negative connection. It is used for 1000BASE-T speed only and connects the internal PHY to the external 1000 magnetics. For 10BASE-T/100BASE-TX speeds only, this pin can be left as a no connect.
- **TXRX2P_D** (pin 17): This pin is the PHY port 2 differential pair D twisted pair positive connection. It is used for 1000BASE-T speed only and connects the internal PHY to the external 1000 magnetics. For 10BASE-T/100BASE-TX speeds only, this pin can be left as a no connect.
- **TXRX2M_D** (pin 18): This pin is the PHY port 2 differential pair D twisted pair negative connection. It is used for 1000BASE-T speed only and connects the internal PHY to the external 1000 magnetics. For 10BASE-T/100BASE-TX speeds only, this pin can be left as a no connect.

6.2 Magnetics Selection

A 1:1 isolation transformer is required at the line interface. For designs exceeding FCC requirements, utilize one with integrated Common-mode chokes. An optional auto-transformer stage following the chokes provides additional Common-mode noise and signal attenuation.

A magnetic with symmetrical and identical circuits for all four differential pairs is recommended for Auto MDI/MDI-X support.

Table 6-1 provides a list of recommended magnetic characteristics. Check to ensure selected magnetics meet or exceed these requirements.

TABLE 6-1: MAGNETICS SELECTION CRITERIA

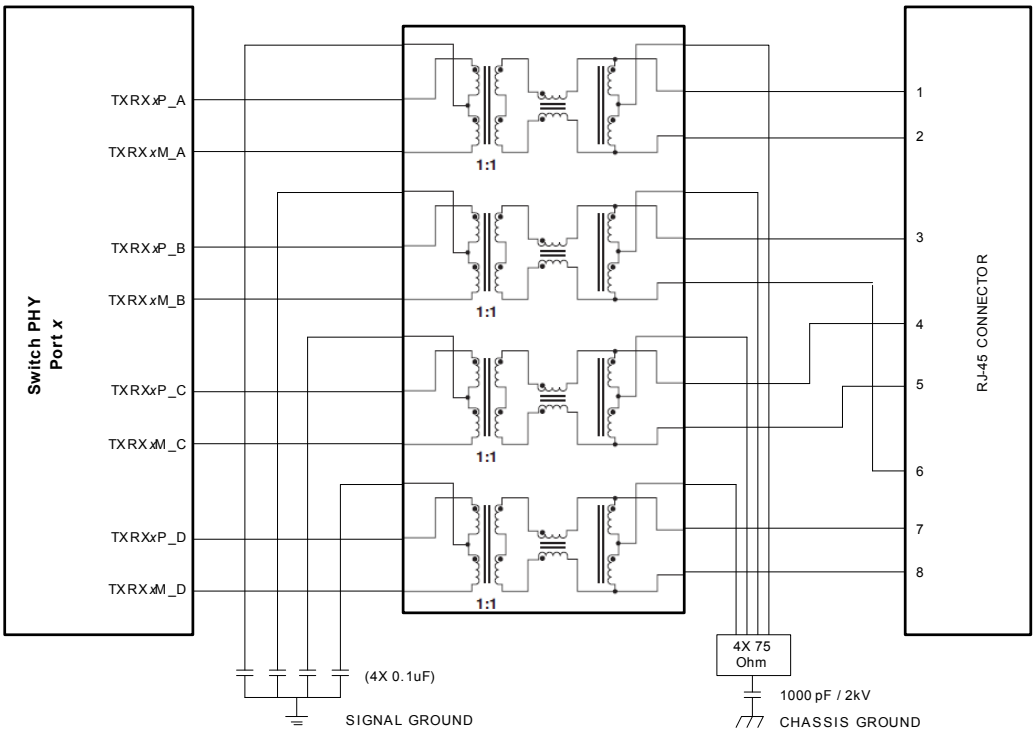
Parameter	Value	Test Condition
Turns Ratio	1 CT:1 CT	—
Minimum Open-circuit Inductance	350 µH	100 mV, 100 kHz, 8 mA
Typical Insertion Loss	1.0 dB	100 kHz to 100 MHz
Minimum HIPOT	1500 Vrms	—

6.3 Magnetic and RJ45 Plug Connections

6.3.1 10/100/1000 MBPS (GIGABIT) ETHERNET

For Gigabit Ethernet support, the Ethernet signal connections between the KSZ9893RNX device and magnetics, and between magnetics and the RJ45 connector are shown in Figure 6-1.

FIGURE 6-1: GIGABIT ETHERNET CONNECTIONS



With the Voltage-mode implementation, the KSZ9893RNX transmit drivers supply the Common-mode voltages to the four differential pairs.

On the KSZ9893R chip side, each of the four transformer center tap pins should not be connected to any power supply source on the board. Instead, the center tap pins should be separated from one another and connected through separate 0.1 µF Common-mode capacitors to ground. Separation is required because the Common-mode voltage could be different between the differential pairs, depending on the operating mode.

On the RJ45 connector side, each of the four transformer center tap pins is terminated through separate 75Ω resistors which are joined together through a single 1000 pF, 2 kV capacitor to chassis ground. And the metal case shield of the RJ45 connector is tied directly to the chassis ground.

The Ethernet signal mappings across the magnetics between the KSZ9893RNX device and RJ45 connector are shown in Table 6-2 for Gigabit Ethernet support.

TABLE 6-2: KSZ9893RNX/RJ45 CONNECTOR MAPPING – GIGABIT ETHERNET

KSZ9893RNX Pin-Out	RJ45 Connector Pin-Out
TXRXxP_A	Pin 1
TXRXxM_A	Pin 2
TXRXxP_B	Pin 3
TXRXxM_B	Pin 6
TXRXxP_C	Pin 4
TXRXxM_C	Pin 5
TXRXxP_D	Pin 7
TXRXxM_D	Pin 8

6.3.2 10/100 MBPS (FAST) ETHERNET ONLY

For applications that require link-up limited to 10/100 Mbps speeds only, the autonegotiation advertisement for 1000 Mbps speed and full-/half-duplex capabilities should be removed to avoid any potential link-up issue due to interoperability. After power-up or reset, program the following 16-bit Port N register bit settings, where N is 1 for port 1 and 2 for port 2.

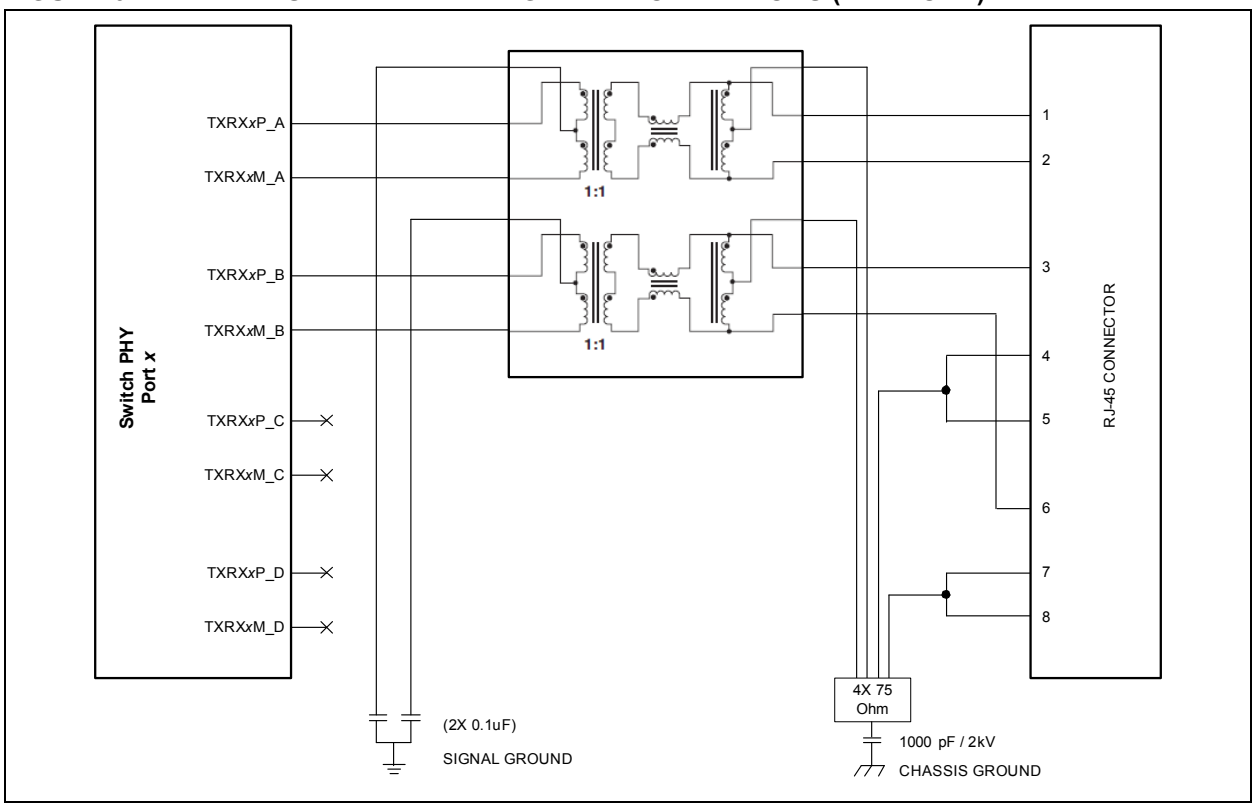
1. Set Port Register 0xN100, Bit [6] = ‘0’ to remove 1000 Mbps speed.
2. Set Port Register 0xN112, Bits [9:8] = ‘00’ to remove autonegotiation advertisements for 1000 Mbps full/half-duplex.
3. Write a ‘1’ to Register 0xN100, Bit [9], a self-clearing bit, to force a restart of autonegotiation.

6.3.2.1 10/100 Mbps Ethernet (MDI Mode)

For Fast Ethernet support for the MDI mode configuration, the Ethernet signal connections between the KSZ9893RNX device and magnetics and between magnetics and RJ45 connector are shown in Figure 6-2.

Note: Despite having the Auto MDI/MDI-X function to swap differential pairs, PHY ports that are implemented as Ethernet end devices are connected by default to the MDI mapping with differential pairs A and B mapped to RJ45 connector pin pairs 1 and 2 as well as pin pairs 3 and 6, respectively.

FIGURE 6-2: FAST ETHERNET MAGNETIC CONNECTIONS (MDI MODE)



With the Voltage-mode implementation, the KSZ9893RNX transmit drivers supply the Common-mode voltages to the four differential pairs (two active: pairs A and B; and two inactive: pairs C and D for 10/100 Mbps Speed modes).

On the KSZ9893R chip side:

- The two transformer center tap pins, for the active differential pairs A and B, should not be connected to any power supply source on the board. Instead, the center tap pins should be separated from one another and connected through separate 0.1 µF Common-mode capacitors to ground. Separation is required because the Common-mode voltage could be different between the differential pairs, depending on the operating mode.
- Autonegotiation and 10BASE-T/100BASE-TX speeds use only differential pairs A and B. The inactive (unused) differential pairs C and D are left as no connects.

On the RJ45 connector side:

- The two transformer center tap pins, for the active differential pairs A and B, are terminated through separate 75Ω resistors which are joined together with the other two separate 75Ω resistors (in the following bullet point) through a single 1000 pF, 2 kV capacitor to chassis ground.
- The unused RJ45 pins are shorted together as pin pairs 4 and 5 and pairs 7 and 8. They are also terminated through separate 75Ω resistors which are joined together with the other two separate 75Ω resistors (in the previous bullet point) through the same single 1000 pF, 2 kV capacitor (in the previous bullet point) to chassis ground.
- The metal case shield of the RJ45 connector is tied directly to chassis ground.

The Ethernet signal mappings across the magnetics between the KSZ9893RNX device and RJ45 connector are shown in Table 6-3.

TABLE 6-3: KSZ9893RNX/RJ45 CONNECTOR MAPPING – FAST ETHERNET (MDI MODE)

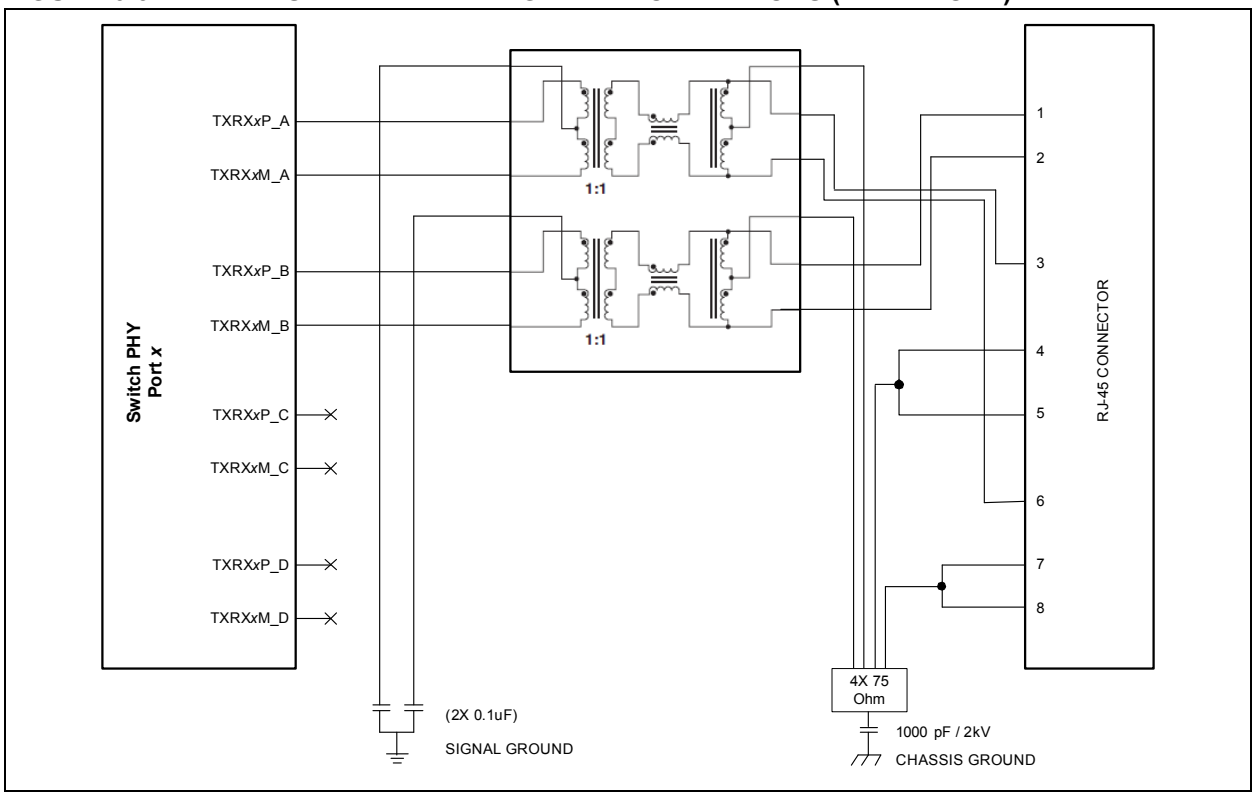
KSZ9893RNX Pin-Out	RJ45 Connector Pin-Out
TXRXxP_A	Pin 1
TXRXxM_A	Pin 2
TXRXxP_B	Pin 3
TXRXxM_B	Pin 6

6.3.2.2 10/100 Mbps Ethernet (MDI-X Mode)

For Fast Ethernet support for the MDI-X mode configuration, the Ethernet signal connections between the KSZ9893RNX device and magnetics, and between magnetics and RJ45 connector are shown in Figure 6-3.

Note: Despite having the Auto MDI/MDI-X function to swap differential pairs, PHY ports that are implemented as Ethernet midspan devices are connected by default to the MDI-X mapping with differential pairs A and B mapped to RJ45 connector pin pairs 1 and 2 as well as pin pairs 3 and 6, respectively.

FIGURE 6-3: FAST ETHERNET MAGNETIC CONNECTIONS (MDI-X MODE)



With the Voltage-mode implementation, the KSZ9893RNX transmit drivers supply the Common-mode voltages to the four differential pairs (two active: pairs A and B; and two inactive: pairs C and D for 10/100 Mbps Speed modes).

On the KSZ9893R chip side:

- The two transformer center tap pins, for the active differential pairs A and B, should not be connected to any power supply source on the board. Instead, the center tap pins should be separated from one another and connected through separate 0.1 µF Common-mode capacitors to ground. Separation is required because the Common-mode voltage could be different between the differential pairs, depending on the operating mode.
- Autonegotiation and 10BASE-T/100BASE-TX speeds use only differential pairs A and B. The inactive (unused) differential pairs C and D are left as no connects.

On the RJ45 connector side:

- The two transformer center tap pins, for the active differential pairs A and B, are terminated through separate 75Ω resistors which are joined together with the other two separate 75Ω resistors (in the following bullet point) through a single 1000 pF, 2 kV capacitor to chassis ground.
- The unused RJ45 pins are shorted together as pin pairs 4 and 5 and pin pairs 7 and 8. They are also terminated through separate 75Ω resistors which are joined together with the other two separate 75Ω resistors (in the previous bullet point) through the same single 1000 pF, 2 kV capacitor (in the previous bullet point) to chassis ground.
- The metal case shield of the RJ45 connector is tied directly to chassis ground.

The Ethernet signal mappings across the magnetics between the KSZ9893RNX device and RJ45 connector are shown in Table 6-4.

TABLE 6-4: KSZ9893RNX/RJ45 CONNECTOR MAPPING – FAST ETHERNET (MDI-X MODE)

KSZ9893RNX Pin-Out	RJ45 Connector Pin-Out
TXRXxP_A	Pin 3
TXRXxM_A	Pin 6
TXRXxP_B	Pin 1
TXRXxM_B	Pin 2

7.0 MANAGEMENT BUS SELECTION

For the selected management bus interface in the following sub-sections, check to ensure the listed design guidelines are followed. Also, refer to application note, *AN2661 Getting Started with 3-Port Gigabit Ethernet Switch Configuration Options*, for further details.

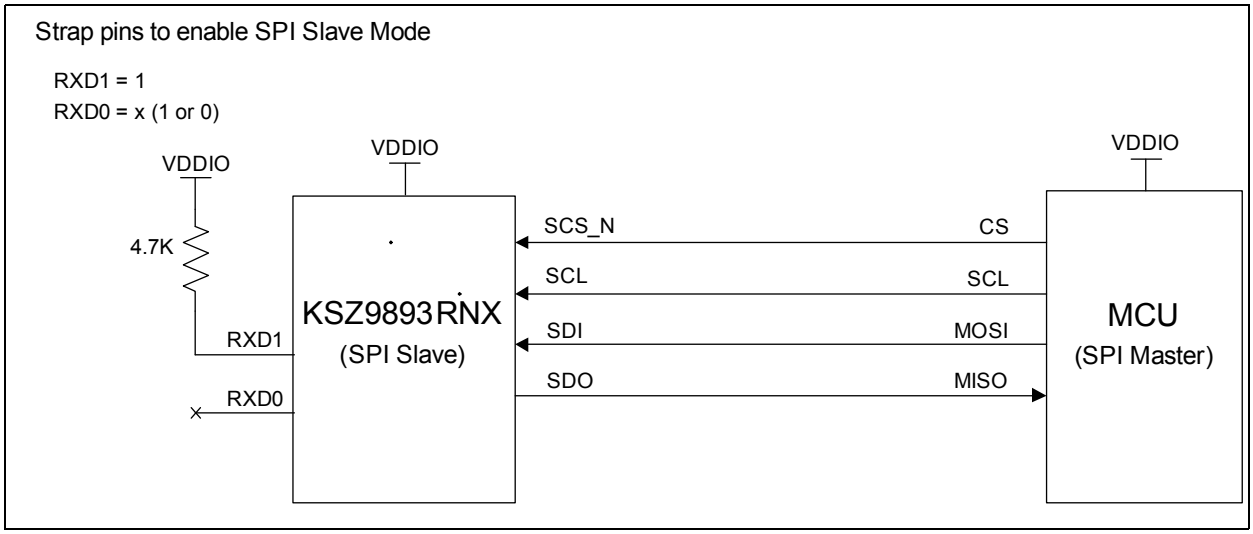
7.1 SPI Slave Management

SPI Slave Management mode provides complete read and write access to all KSZ9893RNX device (PHY and Switch) registers. The external SPI master device supplies the chip select (SCS_N), serial clock (SCL), and serial input data (SDI). Serial output data (SDO) is driven by the KSZ9893RNX.

To select and enable SPI Slave mode, the RXD1 and RXD0 strap pins are set to 1 and x (either 1 or 0), respectively, Refer to Section 2.3, "Configuration Strap Pins" for more details.

Voltage translators are needed if the VDDIO voltages of the KSZ9893RNX device and external SPI master device are different. The SPI block diagram and pin connections between the KSZ9893RNX device and micro-controller (MCU) are shown in Figure 7-1.

FIGURE 7-1: SPI BLOCK DIAGRAM



7.2 I²C Slave Management

I²C Slave Management mode provides complete read and write access to all KSZ9893RNX device (PHY and Switch) registers. The external I²C master device supplies the serial clock (SCL). The serial data (SDA) is a bi-directional open-drain that is driven by the I²C master for register read and write access and is driven by the KSZ9893RNX device to return the register read value.

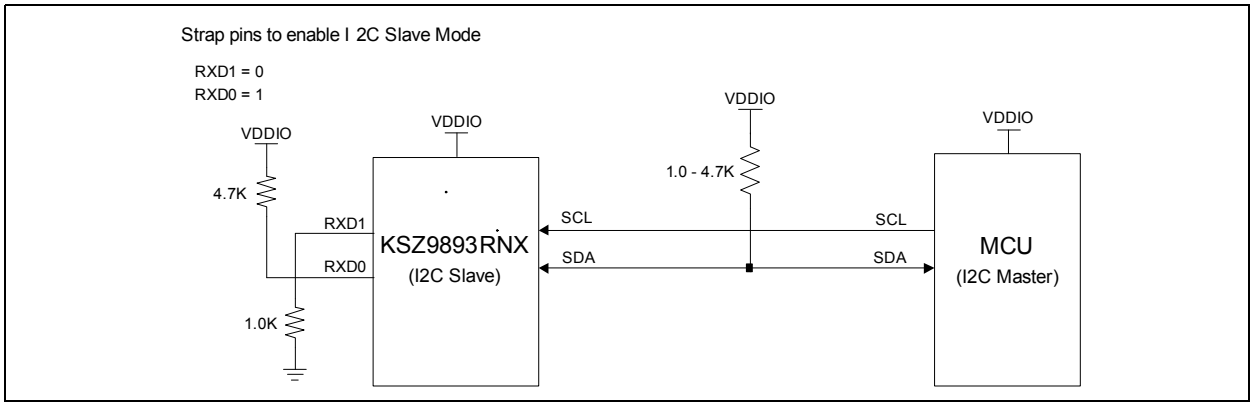
To select and enable I²C Slave mode, the RXD1 and RXD0 strap pins are set to 0 and 1, respectively. Refer to Section 2.3, "Configuration Strap Pins" for more details.

An external 1.0-kΩ-to-4.7-kΩ pull-up resistor is required on the SDA signal.

Voltage translators are needed if the VDDIO voltages of the KSZ9893RNX device and external I²C master device are different.

The I²C block diagram and pin connections between the KSZ9893RNX device and micro-controller (MCU) are shown in Figure 7-2.

FIGURE 7-2: I²C BLOCK DIAGRAM



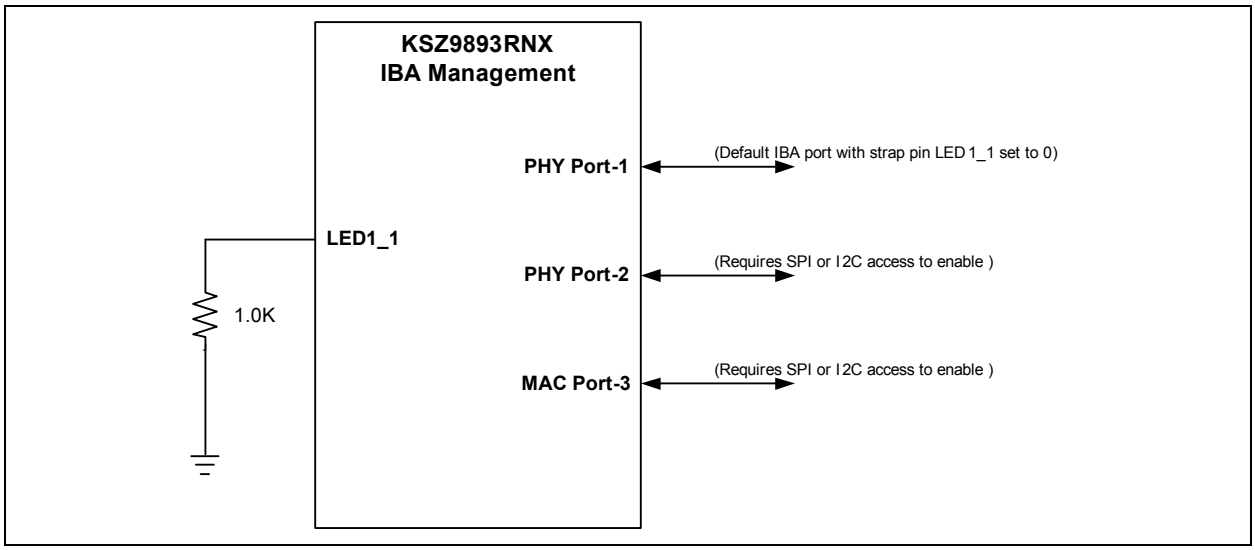
7.3 In-Band Access (IBA) Management

In-Band Access (IBA) Management is a proprietary feature that uses customized 64-byte Ethernet frames to provide complete read and write access to all KSZ9893RNX device (PHY and Switch) registers. Any one of the three data ports (PHY port 1, PHY port 2, or MAC port 3) can be used for in-band register access.

To select and enable IBA Management mode, the LED1_1 strap pins are pulled down. Refer to Section 2.3, "Configuration Strap Pins" for more details. With the IBA pin strapping, PHY port 1 is assigned as the default IBA port. SPI or I²C management is required to enable MAC port 3 (host processor port) or PHY port 2 (alternative PHY port) as the IBA port.

Refer to the In-Band Management (IBA) Control register at address locations 0x0104 – 0x0107 in the *KSZ9893RNX Data Sheet* for the bit settings to select MAC port 3 or PHY port 2 as the IBA port. Figure 7-3 shows the IBA block diagram.

FIGURE 7-3: IBA BLOCK DIAGRAM



7.4 MII Management (MIIM)

MII Management mode provides access only to the KSZ9893RNX PHY registers. The external MDC/MDIO controller device supplies the serial clock (MDC). The serial data (MDIO) is a bi-directional open drain that is driven by the controller for register read and write access. It is also driven by the KSZ9893RNX device to return the register read value.

To select and enable MIIM mode, the RXD1 and RXD0 strap pins are both set to 0s. Refer to Section 2.3, "Configuration Strap Pins" for more details.

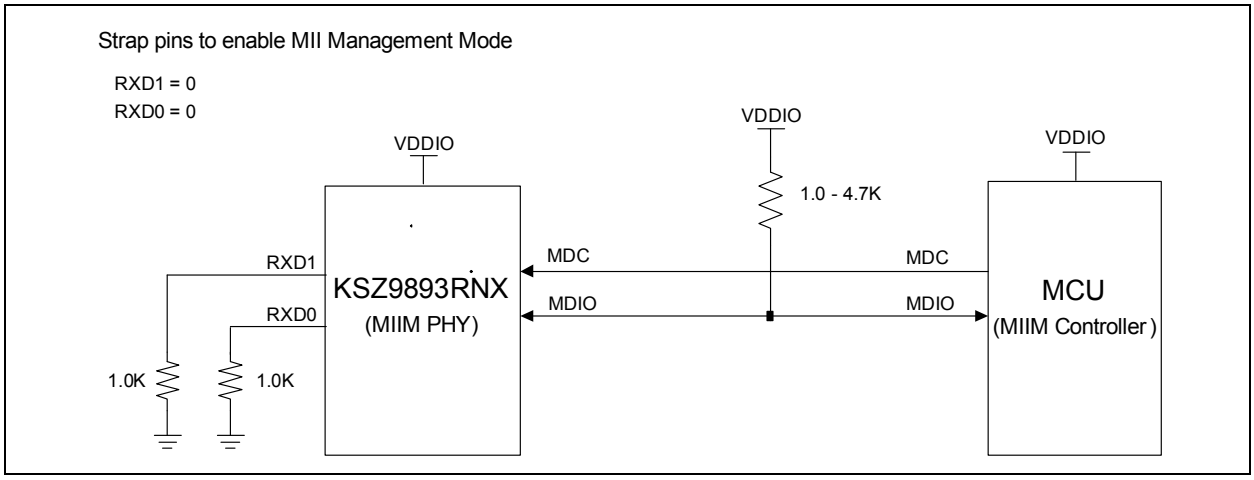
An external 1.0-kΩ-to-4.7 kΩ pull-up resistor is required on the MDIO signal.

Voltage translators are needed if the VDDIO voltages of the KSZ9893RNX device and external MDC/MDIO controller device are different.

Note: It is recommended to keep the pull-up resistor on MDIO pin of the MCU even if this interface is not used.

The MII Management block diagram and pin connections between the KSZ9893RNX device and micro-controller (MCU) are shown in Figure 7-4.

FIGURE 7-4: MII MANAGEMENT BLOCK DIAGRAM



8.0 MAC PORT 3 – DIGITAL DATA BUS INTERFACES

The MAC port 3 data interface can be set to one of the following five xMII configurations:

- RGMII Interface: Supports 1000, 100, and 10 Mbps data rates
- RMII (Clock Mode) Interface: Supports 100 and 10 Mbps data rates and outputs 50 MHz RMII REF_CLK
- RMII (Normal Mode) Interface: Supports 100 and 10 Mbps data rates and inputs 50 MHz RMII REF_CLK
- MII (MAC Mode) Interface: Supports 100 and 10 Mbps data rates and connects to external MII PHY or MII port of chipset in PHY mode (e.g., Ethernet Switch or MAC processor)
- MII (PHY Mode) Interface: Supports 100 and 10 Mbps data rates and connects to external MII MAC

For the selected data bus interface in the following sub-sections, check to ensure the listed design guidelines are followed.

8.1 RGMII Interface

8.1.1 RGMII FUNCTIONAL CONFIGURATION

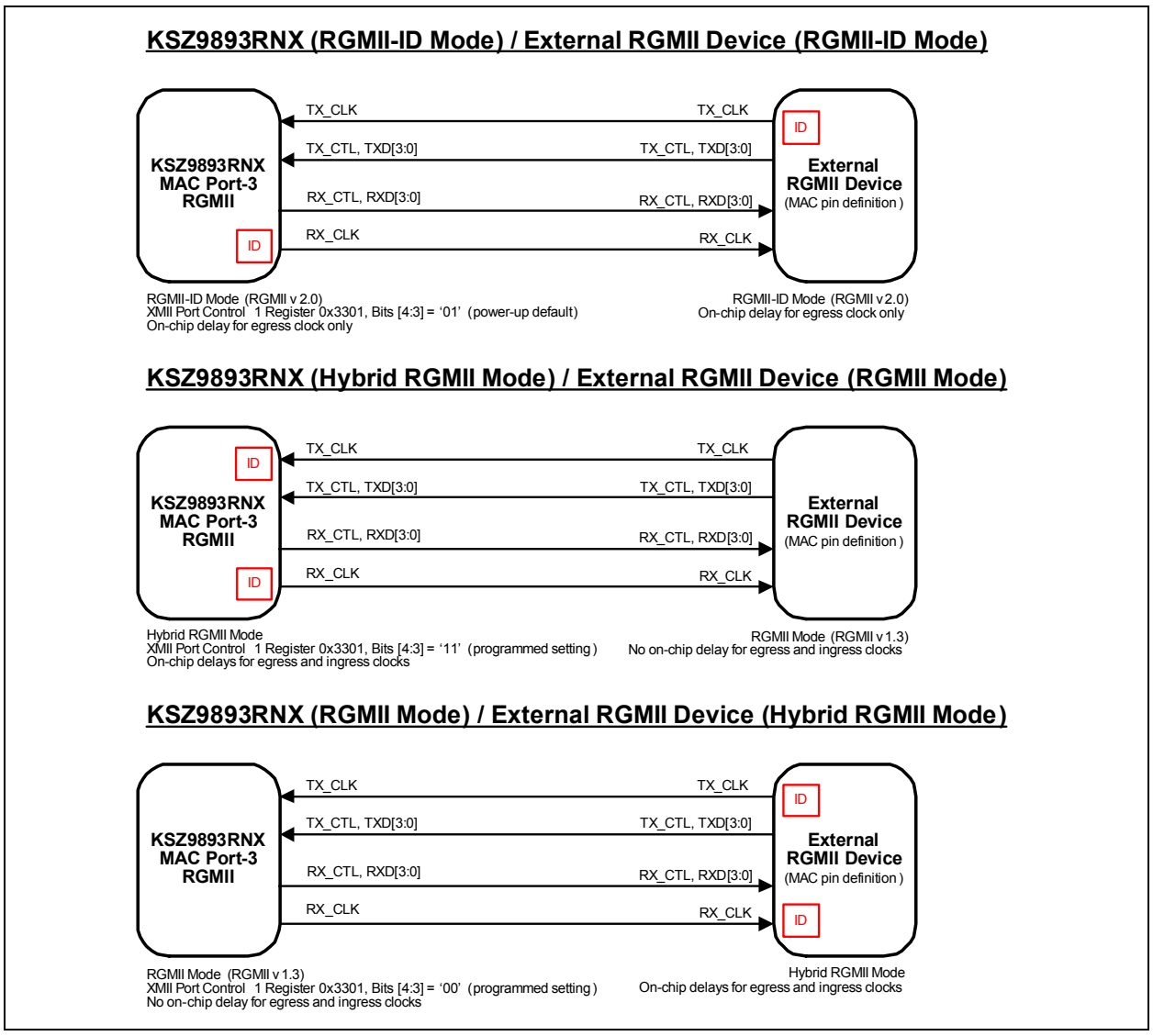
When the KSZ9893RNX is set to the RGMII configuration, MAC port 3 is configured to support RGMII-ID mode (with internal delay for egress output clock) for RGMII v2.0 support, as the power-up default setting.

Optionally, the KSZ9893RNX can be programmed after power-up to support either one of the following two modes:

- Hybrid RGMII mode (with internal delays for egress output clock and for ingress input clock) when interfacing with an RGMII device that is configured with no internal delay for egress output clock and ingress input clock
- RGMII mode (without internal delay for egress output clock and ingress input clock) for RGMII v1.3 support when interfacing with an RGMII device that is configured with internal delays for egress output clock and ingress input clock

Figure 8-1 shows the on-chip delays for the three aforementioned common RGMII functional configurations. The on-chip clock delays (denoted by “ID”) are depicted in the figure with RGMII connections between KSZ9893RNX and external RGMII device (MAC pin definition). KSZ9893RNX register bit settings to enable/disable the on-chip egress and ingress clock delays are provided in the figure.

FIGURE 8-1: KSZ9893RNX AND EXTERNAL RGMII DEVICE (MAC PIN DEFINITION) – RGMII FUNCTIONAL CONFIGURATION WITH ON-CHIP CLOCK DELAY OPTIONS



8.1.2 RGMII SKEW CALCULATION

RGMII is a source synchronous clock data bus. The clock is sourced from the device side that is sending out the 4-bit data and control signals. This allows for RGMII skew calculation and PCB trace length matching or delay (if applicable) to be applied separately for the RGMII transmit bus group (TX_CLK, TX_CTL, and TXD[3:0]) and RGMII receive bus group (RX_CLK, RX_CTL, and RXD[3:0]).

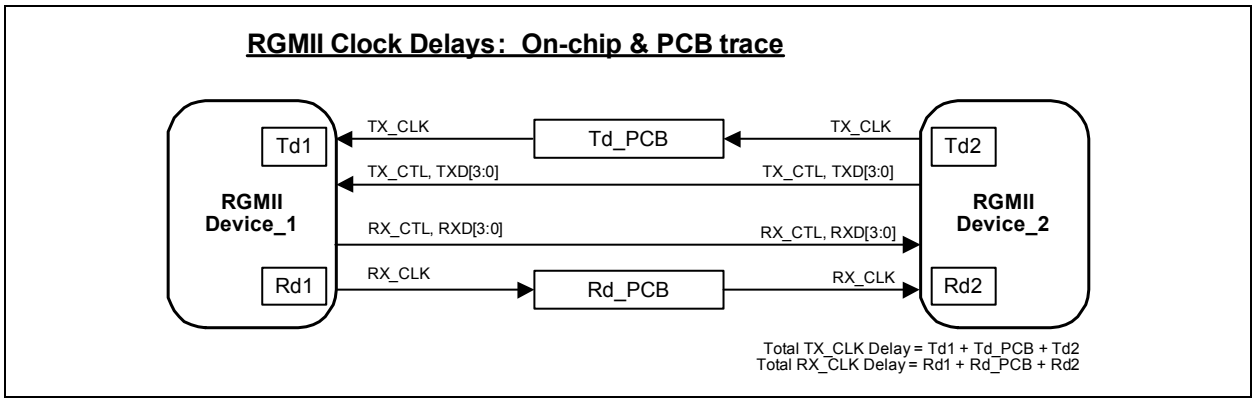
The RGMII clock skews are summarized in Figure 8-2 below, and are computed as follows:

- Total TX_CLK Delay = Td1 + Td_PCB + Td2
- Total RX_CLK Delay = Rd1 + Rd_PCB + Rd2

Separately, in each direction, the RGMII data/control signal to clock skew should be set between 1.2 ns (minimum) and 2.0 ns (maximum).

Note:	The calculations assume that there is no skew (i.e., virtually zero delay) between data and control signals. If there is significant skew (e.g., due to device errata) between data and control lines, corrections (e.g., by adjusting PCB trace lengths and/or by setting skew registers if applicable) to match the data and control lines should be made prior to applying the above clock skew requirement.

FIGURE 8-2: RGMII CLOCK SKEW DIAGRAM



8.1.3 RGMII INTERFACE WITH EXTERNAL RGMII DEVICE

When the KSZ9893RNX MAC port 3 is connected to an external RGMII device, remember the following key design guidelines:

- Determine the RGMII functional mode (RGMII-ID, Hybrid, or RGMII) to use to connect with the external RGMII device, as defined in Section 8.1.1, "RGMII Functional Configuration".
- For the selected RGMII functional mode, calculate the RGMII clock delay and, if needed, make additional skew adjustments to the RGMII clock, data, and/or control lines, as discussed in Section 8.1.2, "RGMII Skew Calculation". The additional skew adjustments can be achieved by inserting PCB trace length delays and, if supported by the RGMII device, by programming RGMII pad skew step settings (e.g., Microchip KSZ9031RNX Gigabit Ethernet PHY has RGMII Pad Skew Step registers).
- Route RGMII signals over a continuous ground plane layer for 50Ω impedance control.
- The signal traces should be matched within 7.62 mm (300 mils) for best performance. All Transmit signals should be matched, and all Receive signals should be matched. It is not as critical for the Transmit and Receive signal groups to be matched to each other.
- It is recommended to place series termination resistors on all RGMII output pins. Refer to Figure 8-3 for output pin placement. Combined with the output pin impedance, these series resistors provide the means to tune and match the PCB trace impedance to minimize ringing, and thus improve signal integrity and reduce EMI. The typical resistor value ranges from 22Ω to 50Ω with the optimum value being dependent on the board layout. A resistor value of 33Ω can be used as the starting point for the schematic design.

8.1.3.1 KSZ9893RNX RGMII AND EXTERNAL RGMII DEVICE (MAC PIN DEFINITION)

The KSZ9893RNX RGMII signal connections with an external RGMII device (MAC pin definition), such as a MAC processor or the MAC port of a Gigabit Ethernet switch, are shown in Figure 8-3 and Table 8-1.

Note: Always check the pin types in the data sheet for the connecting RGMII pins between two devices to ensure the adjoining pins are neither both inputs nor both outputs. Do not rely on just the pin name of the RGMII interface between two connecting devices. The same pin name may be defined as an input or an output depending on the interface perspective.

FIGURE 8-3: KSZ9893RNX RGMII AND EXTERNAL RGMII DEVICE (MAC PIN DEFINITION) – BLOCK DIAGRAM

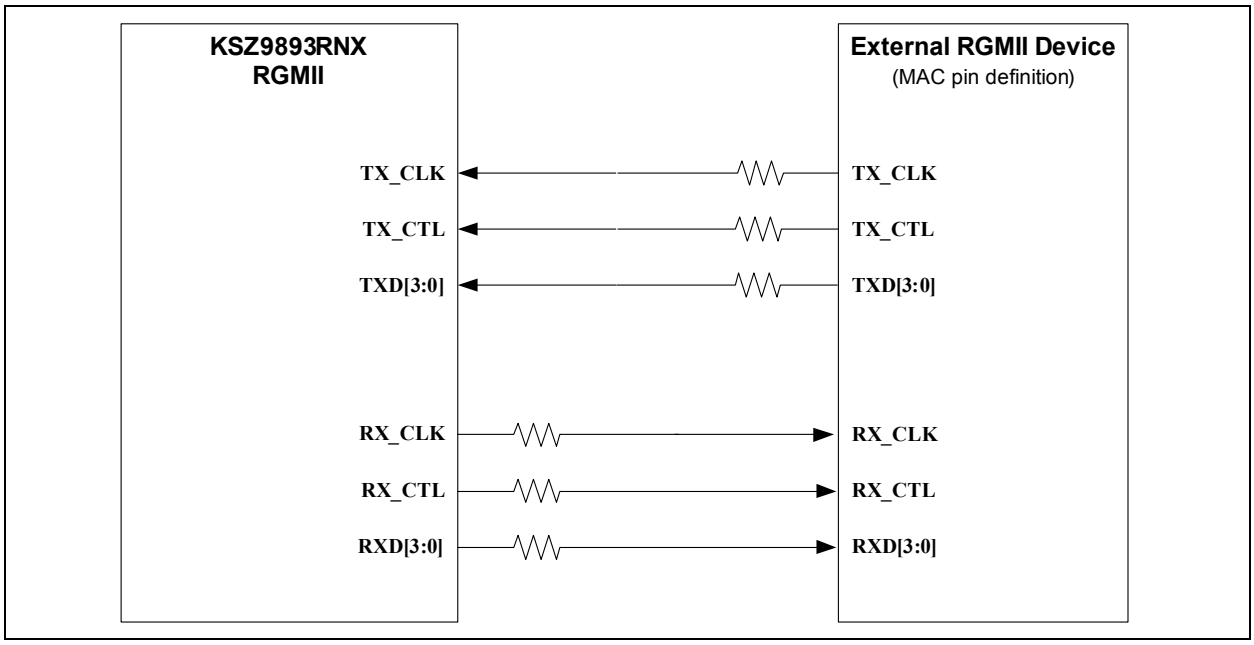


TABLE 8-1: KSZ9893RNX RGMIII AND EXTERNAL RGMII DEVICE (MAC PIN DEFINITION) – PIN CONNECTIONS

KSZ9893RNX RGMII			External RGMII Device (Mac Pin Definition)	
Pin Number	**Pin Name**	**Pin Type**	**Pin Name**	**Pin Type**
33	TX_CLK	Input	TX_CLK	Output
35	TX_CTL	Input	TX_CTL	Output
29	TXD3	Input	TXD3	Output
30	TXD2	Input	TXD2	Output
31	TXD1	Input	TXD1	Output
32	TXD0	Input	TXD0	Output
25	RX_CLK	Output	RX_CLK	Input
27	RX_CTL	Output	RX_CTL	Input
21	RXD3	Output	RXD3	Input
22	RXD2	Output	RXD2	Input
23	RXD1	Output	RXD1	Input
24	RXD0	Output	RXD0	Input

8.1.3.2 KSZ9893RNX RGMII AND EXTERNAL RGMII DEVICE (PHY PIN DEFINITION)

The KSZ9893RNX RGMII signal connections with an external RGMII device (PHY pin definition), such as a Gigabit Ethernet PHY or the MAC port of a Gigabit Ethernet switch, are shown in Figure 8-4 and Table 8-2.

Note: Always check the pin types in the data sheet for the connecting RGMII pins between two devices to ensure the adjoining pins are neither both inputs nor both outputs. Do not rely on just the pin name of the RGMII interface between two connecting devices. The same pin name may be defined as an input or an output depending on the interface perspective.

FIGURE 8-4: KSZ9893RNX RGMII AND EXTERNAL RGMII DEVICE (PHY PIN DEFINITION) – BLOCK DIAGRAM

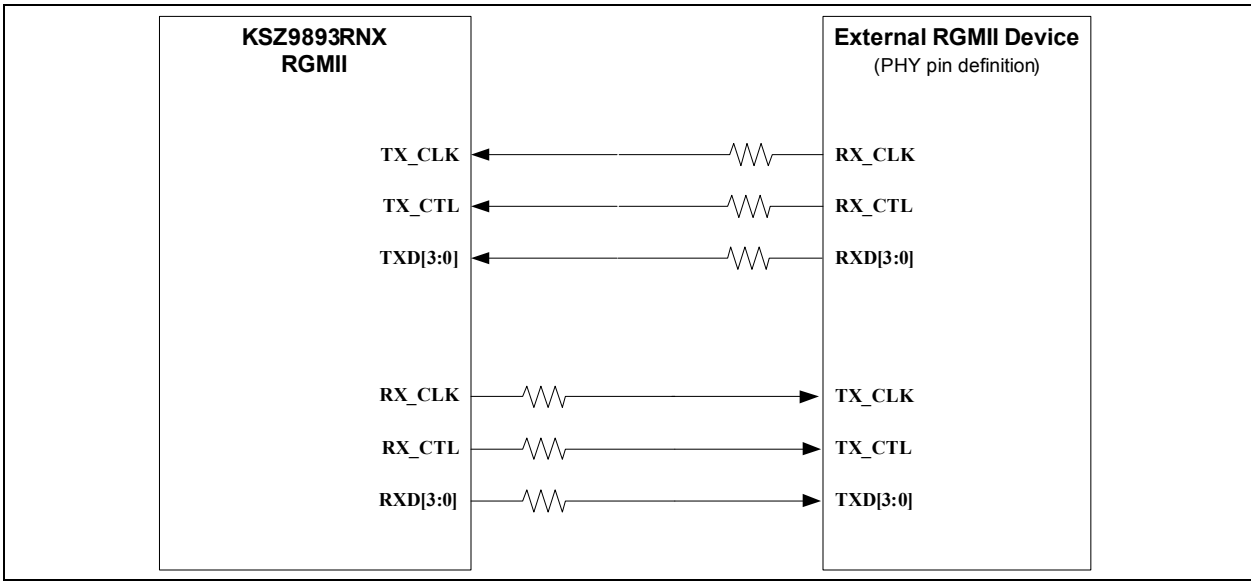


TABLE 8-2: KSZ9893RNX RGMIII AND EXTERNAL RGMII DEVICE (PHY PIN DEFINITION) – PIN CONNECTIONS

KSZ9893RNX RGMII			External RGMII Device PHY Pin Definition	
Pin Number	**Pin Name**	**Pin Type**	**Pin Name**	**Pin Type**
33	TX_CLK	Input	RX_CLK	Output
35	TX_CTL	Input	RX_CTL	Output
29	TXD3	Input	RXD3	Output
30	TXD2	Input	RXD2	Output
31	TXD1	Input	RXD1	Output
32	TXD0	Input	RXD0	Output
25	RX_CLK	Output	TX_CLK	Input
27	RX_CTL	Output	TX_CTL	Input
21	RXD3	Output	TXD3	Input
22	RXD2	Output	TXD2	Input
23	RXD1	Output	TXD1	Input
24	RXD0	Output	TXD0	Input

8.2 RMII (Clock Mode) Interface

When the KSZ9893RNX is configured to RMII (Clock mode), MAC port 3 is configured to output the RMII Reference clock.

The key design guidelines to note are:

- The RMII 50 MHz reference clock (REF_CLK) is an output from the KSZ9893RNX and is an input to the connecting RMII device.
- The receive error (RX_ER) signal is not supported by the KSZ9893RNX. External RMII MAC with the RX_ER input should have this pin pulled low or tied to ground, and external RMII PHY with the RX_ER output should have this pin left as a no connect.
- Users need to ensure the RMII timing is met between two connecting RMII devices. RMII timing uses a common 50 MHz reference clock between two connecting RMII devices. The RMII timing margin becomes critical when the REF_CLK source is located within or is placed close to one RMII device, with the other RMII device placed farther away or across the backplane connector.

Note: The 50 MHz RMII clock has a 20 ns clock period. With minimum specification requirements of 4 ns and 2 ns for the input setup and hold times, the RMII clock period is left with 14 ns (20 ns minus 6 ns for setup/hold times) to cover the transmit output delay and round trip PCB trace delays for the RMII device located furtherest away from the REF_CLK. For example, if the farthest RMII device has the worst case transmit output delay of 12 ns, the PCB trace delay between the two connecting RMII devices is limited to 2 ns (round-trip) or 1 ns (one-way).

- It is recommended to place series termination resistors on all RMII output pins. Refer to Figure 8-5 for output pin placement. Combined with the output pin impedance, these series resistors provide the means to tune and match the PCB trace impedance to minimize ringing, and thus improve signal integrity and reduce EMI. The typical resistor value ranges from 22Ω to 50Ω with the optimum value being dependent on the board layout. A resistor value of 33Ω can be used as the starting point for the schematic design.

The KSZ9893RNX RMII (Clock mode) signal connections with an external RMII device (MAC pin definition) are shown in Figure 8-5 and Table 8-3.

Note: Always check the pin types in the data sheet for the connecting RMII pins between two devices to ensure the adjoining pins are neither both inputs nor both outputs. Do not rely on just the pin name of the RMII interface between two connecting devices. The same pin name may be defined as an input or an output depending on the interface perspective.

FIGURE 8-5: KSZ9893RNX RMII (CLOCK MODE) AND EXTERNAL RMII DEVICE (MAC PIN DEFINITION) – BLOCK DIAGRAM

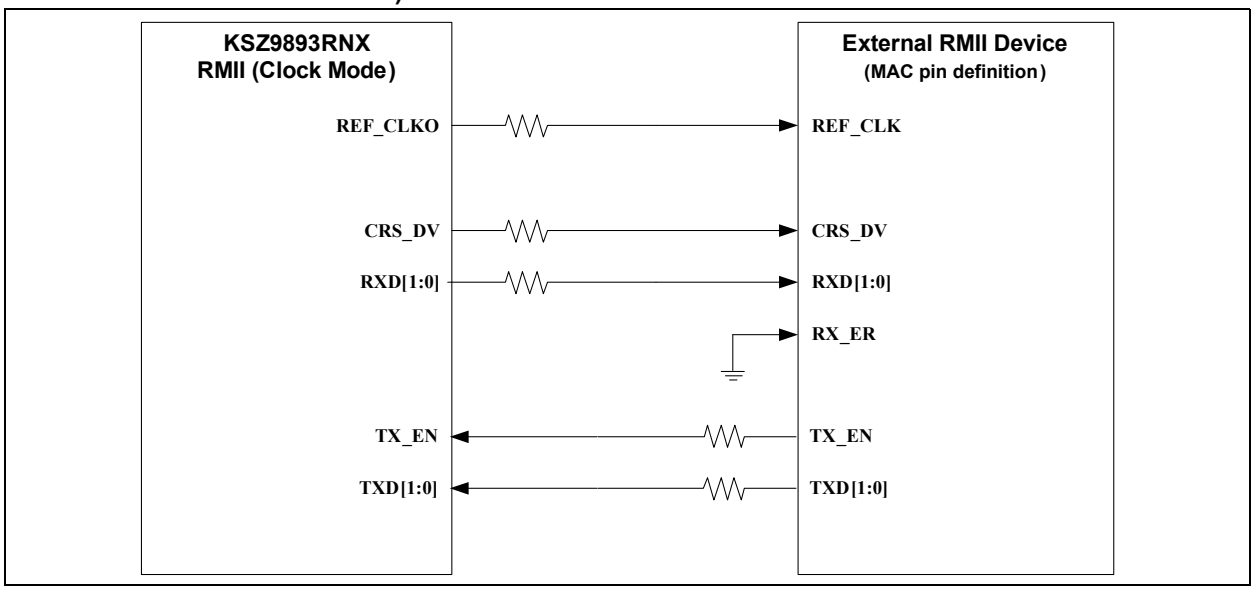


TABLE 8-3: KSZ9893RNX RMII (CLOCK MODE) AND EXTERNAL RMII DEVICE (MAC PIN DEFINITION) – PIN CONNECTIONS

KSZ9563 RMII (Clock Mode)			External RMII Device (MAC Pin Definition)	
Pin Number	**Pin Name**	**Pin Type**	**Pin Name**	**Pin Type**
25	REF_CLKO	Output	REF_CLK	Input
27	CRS_DV	Output	CRS_DV	Input
23	RXD1	Output	RXD1	Input
24	RXD0	Output	RXD0	Input
—	<NO CONNECTION>	—	RX_ER	Input
35	TX_EN	Input	TX_EN	Output
31	TXD1	Input	TXD1	Output
32	TXD0	Input	TXD0	Output

8.3 RMII (Normal Mode) Interface

When the KSZ9893RNX is configured to RMII (Normal mode), MAC port 3 is configured to input the RMII reference clock.

The key design guidelines to note are:

- The RMII 50 MHz reference clock (REF_CLK) is an input to the KSZ9893RNX and is sourced from either external system clock (e.g. 50 MHz oscillator clock) or connecting RMII device. If sourced from external system clock, the REF_CLK is also an input to the connecting RMII device.
- The receive error (RX_ER) signal is not supported by the KSZ9893RNX. External RMII MAC with the RX_ER input should have this pin pulled low or tied to ground, and external RMII PHY with the RX_ER output should have this pin left as a no connect.
- Users need to ensure the RMII timing is met between two connecting RMII devices. RMII timing uses a common 50 MHz reference clock between two connecting RMII devices. The RMII timing margin becomes critical when the REF_CLK source is located within or is placed close to one RMII device, with the other RMII device placed further away or across backplane connector.

Note: The 50 MHz RMII clock has a 20 ns clock period. With minimum specification requirements of 4 ns and 2 ns for the input setup and hold times, the RMII clock period is left with 14 ns (20 ns minus 6 ns for setup/hold times) to cover the transmit output delay and round trip PCB trace delays for the RMII device located furtherest away from the REF_CLK. For example, if the farthest RMII device has the worst case transmit output delay of 12 ns, the PCB trace delay between the two connecting RMII devices is limited to 2 ns (round-trip) or 1 ns (one-way).

- It is recommended to place series termination resistors on all RMII output pins. Refer to Figure 8-6 for output pin placement. Combined with the output pin impedance, these series resistors provide the means to tune and match the PCB trace impedance to minimize ringing, and thus improve signal integrity and reduce EMI. The typical resistor value ranges from 22Ω to 50Ω with the optimum value being dependent on the board layout. A resistor value of 33Ω can be used as the starting point for the schematic design.

The KSZ9893RNX RMII (Normal mode) signal connections with an external RMII device (PHY pin definition) are shown in Figure 8-6 and Table 8-4.

Note: Always check the pin types in the data sheet for the connecting RMII pins between two devices to ensure the adjoining pins are neither both inputs nor both outputs. Do not rely on just the pin name of the RMII interface between two connecting devices. The same pin name may be defined as an input or an output depending on the interface perspective.

FIGURE 8-6: KSZ9893RNX RMII (NORMAL MODE) AND EXTERNAL RMII DEVICE (PHY PIN DEFINITION) – BLOCK DIAGRAM

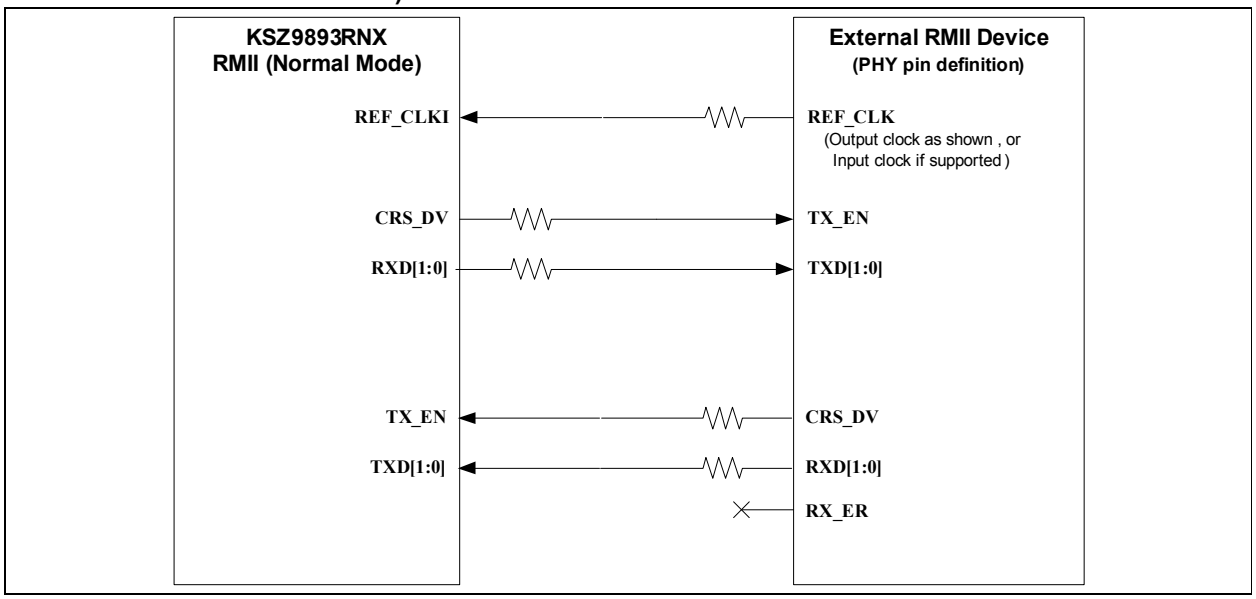


TABLE 8-4: KSZ9893RNX RMII (NORMAL MODE) AND EXTERNAL RMII DEVICE (PHY PIN DEFINITION) – PIN CONNECTIONS

KSZ9563RNX RMII (Normal Mode)			External RMII Device (PHY Pin Definition)	
Pin Number	**Pin Name**	**Pin Type**	**Pin Name**	**Pin Type**
33	REFCLKI	Input	REF_CLK	Output/Input
27	CRS_DV	Output	TX_EN	Input
23	RXD1	Output	TXD1	Input
24	RXD0	Output	TXD0	Input
35	TX_EN	Input	CRS_DV	Output
31	TXD1	Input	RXD1	Output
32	TXD0	Input	RXD0	Output
—	<NO CONNECTION>	—	RX_ER	Output

8.4 MII (MAC Mode) Interface

When the KSZ9893RNX is configured to MII (MAC mode), MAC port 3 is configured like a MII MAC device. The key design guidelines to note are:

- Transmit clock (TX_CLK) and receive clock (RX_CLK) are inputs to the KSZ9893RNX and outputs from the external MII PHY.
- Collision (COL) and carrier sense (CRS) inputs are not supported by the KSZ9893RNX. External MII PHY with COL and CRS outputs should have these two pins left as no connects.
- It is recommended to place series termination resistors on all MII output pins. Refer to Figure 8-7 for output pin placement. Combined with the output pin impedance, these series resistors provide the means to tune and match the PCB trace impedance to minimize ringing and thus improve signal integrity and reduce EMI. The typical resistor value ranges from 22Ω to 50Ω with the optimum value being dependent on the board layout. A resistor value of 33Ω can be used as the starting point for the schematic design.

The KSZ9893RNX MII (MAC mode) signal connections with an external MII PHY are shown in Figure 8-7 and Table 8-5.

Note: Always check the pin types in the data sheet for the connecting MII pins between two devices to ensure the adjoining pins are not both inputs and not both outputs. Do not rely on just the pin name of the MII interface between two connecting devices. The same pin name may be defined as an input or an output depending on the interface perspective.

FIGURE 8-7: KSZ9893RNX MII (MAC MODE) AND EXTERNAL MII PHY – BLOCK DIAGRAM

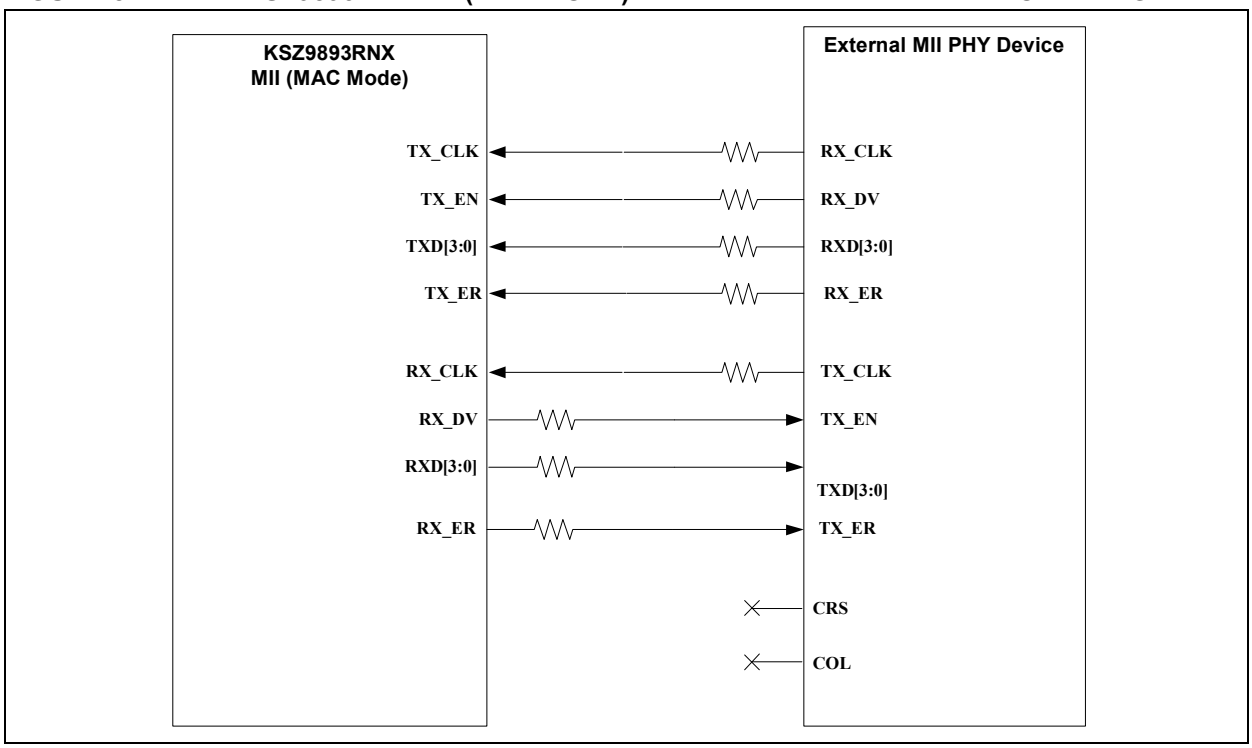


TABLE 8-5: KSZ9893RNX MII (MAC MODE) AND EXTERNAL MII PHY – PIN CONNECTIONS

KSZ9893RNX MII (MAC Mode)			External MII PHY Device	
Pin Number	**Pin Name**	**Pin Type**	**Pin Names**	**Pin Type**
33	TX_CLK	Input	RX_CLK	Output
35	TX_EN	Input	RX_DV	Output
29	TXD3	Input	RXD3	Output
30	TXD2	Input	RXD2	Output
31	TXD1	Input	RXD1	Output
32	TXD0	Input	RXD0	Output
36	TX_ER	Input	RX_ER	Output
25	RX_CLK	Input	TX_CLK	Output
27	RX_DV	Output	TX_EN	Input
21	RXD3	Output	TXD3	Input
22	RXD2	Output	TXD2	Input
23	RXD1	Output	TXD1	Input
24	RXD0	Output	TXD0	Input
28	RX_ER	Output	TX_ER	Input
—	<NO CONNECTION>	—	CRS	Output
—	<NO CONNECTION>	—	COL	Output

8.5 MII (PHY Mode) Interface

When the KSZ9893RNX is configured to MII (PHY Mode), MAC port 3 is configured like a MII PHY device. The key design guidelines to note are:

- Transmit clock (TX_CLK) and receive clock (RX_CLK) are outputs from the KSZ9893RNX and inputs into the external MII MAC.
- Collision (COL) and carrier sense (CRS) outputs are not supported by the KSZ9893RNX. External MII MAC with COL and CRS inputs should have these two pins pulled low or tied to ground.
- It is recommended to place series termination resistors on all MII output pins. Refer to Figure 8-8 for output pin placement. Combined with the output pin impedance, these series resistors provide the means to tune and match the PCB trace impedance to minimize ringing, and thus improve signal integrity and reduce EMI. The typical resistor value ranges from 22Ω to 50Ω with the optimum value being dependent on the board layout. A resistor value of 33Ω can be used as the starting point for the schematic design.

The KSZ9893RNX MII (PHY mode) signal connections with an external MII MAC are shown in Figure 8-8 and Table 8-6.

Note: Always check the pin types in the data sheet for the connecting MII pins between two devices to ensure the adjoining pins are not both inputs and not both outputs. Do not rely on just the pin name of the MII interface between two connecting devices. The same pin name may be defined as an input or an output depending on the interface perspective.

FIGURE 8-8: KSZ9893RNX MII (PHY MODE) AND EXTERNAL MII MAC – BLOCK DIAGRAM

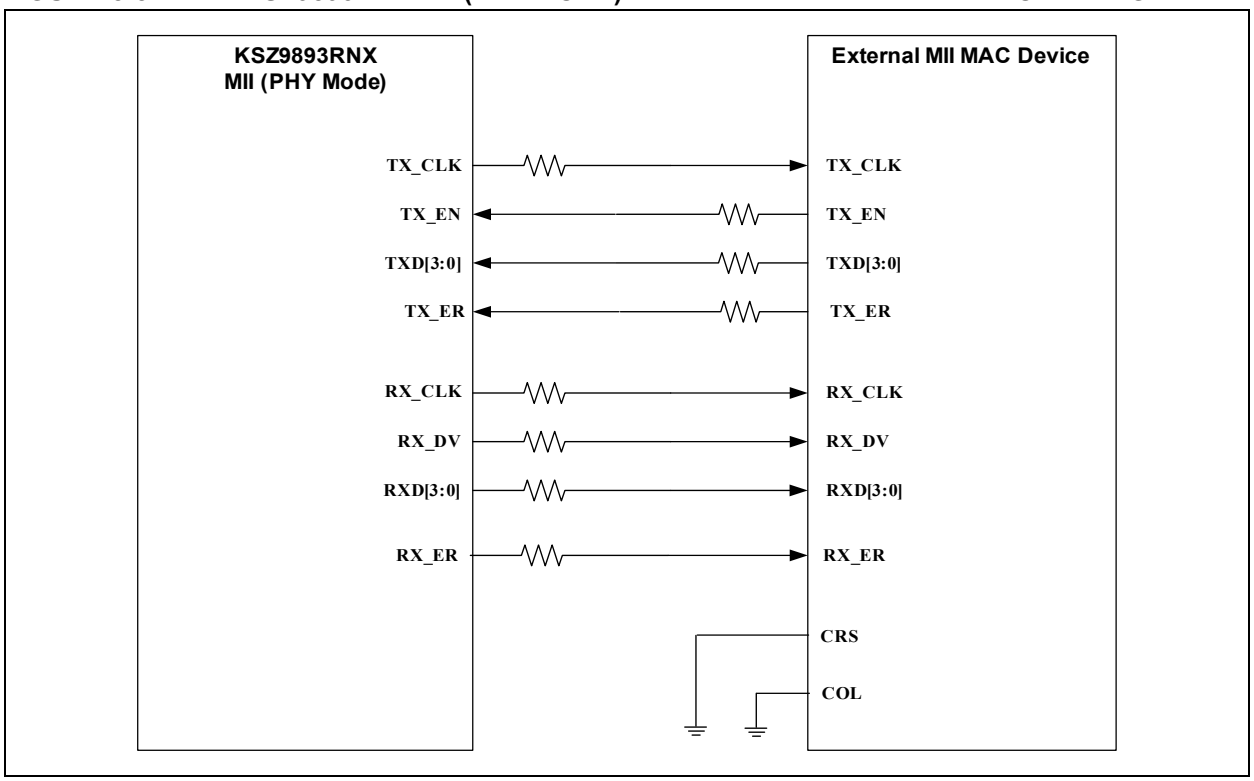


TABLE 8-6: KSZ9893RNX MII (PHY MODE) AND EXTERNAL MII MAC – PIN CONNECTIONS

KSZ9893RNX MII (PHY Mode)			External MII MAC Device	
Pin Number	**Pin Name**	**Pin Type**	**Pin Names**	**Pin Type**
33	TX_CLK	Output	TX_CLK	Input
35	TX_EN	Input	TX_EN	Output
29	TXD3	Input	TXD3	Output
30	TXD2	Input	TXD2	Output
31	TXD1	Input	TXD1	Output
32	TXD0	Input	TXD0	Output
36	TX_ER	Input	TX_ER	Output
25	RX_CLK	Output	RX_CLK	Input
27	RX_DV	Output	RX_DV	Input
21	RXD3	Output	RXD3	Input
22	RXD2	Output	RXD2	Input
23	RXD1	Output	RXD1	Input
24	RXD0	Output	RXD0	Input
28	RX_ER	Output	RX_ER	Input
—	<NO CONNECTION>	—	CRS	Output
—	<NO CONNECTION>	—	COL	Output

9.0 LED INDICATOR PINS

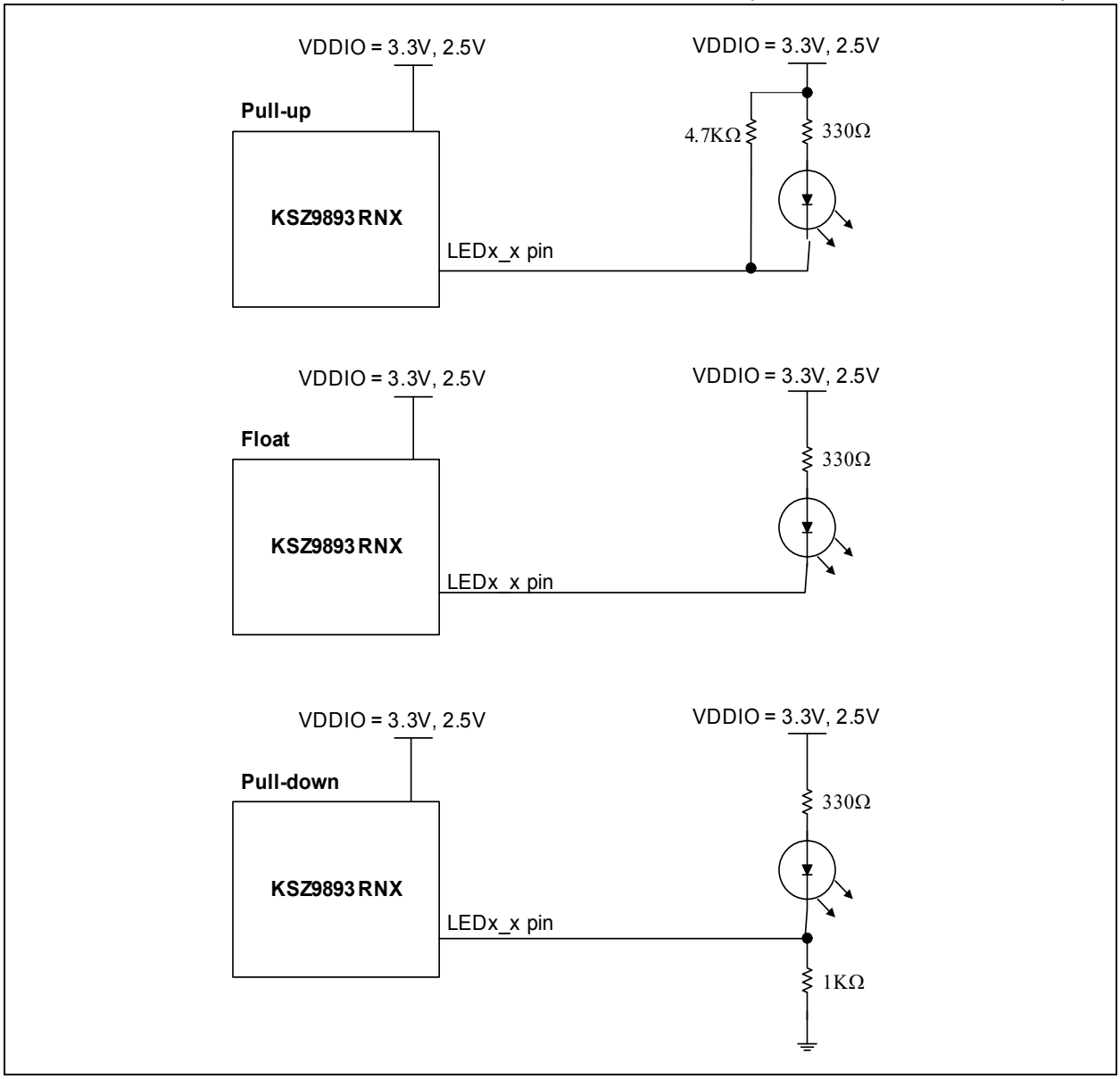
The LEDx_x pins are inputs and function as the multiplexed strapping pins (See Section 2.3, "Configuration Strap Pins".) during chip power-up or hardware pin reset when the RESET_N input (pin 46) is asserted (driven low).

The LEDx_x pins are totem pole outputs to drive LED indicators to indicate the PHY ports' speed, link, and activity status when the RESET_N input is not asserted (driven high).

9.1 PHY Port LED Status and Pin Strapping (for VDDIO = 3.3V or 2.5V)

Figure 9-1 shows the pull-up, float and pull-down reference circuits for the multiplexed PHY port LED status and pin strapping for 3.3V and 2.5 VDDIO.

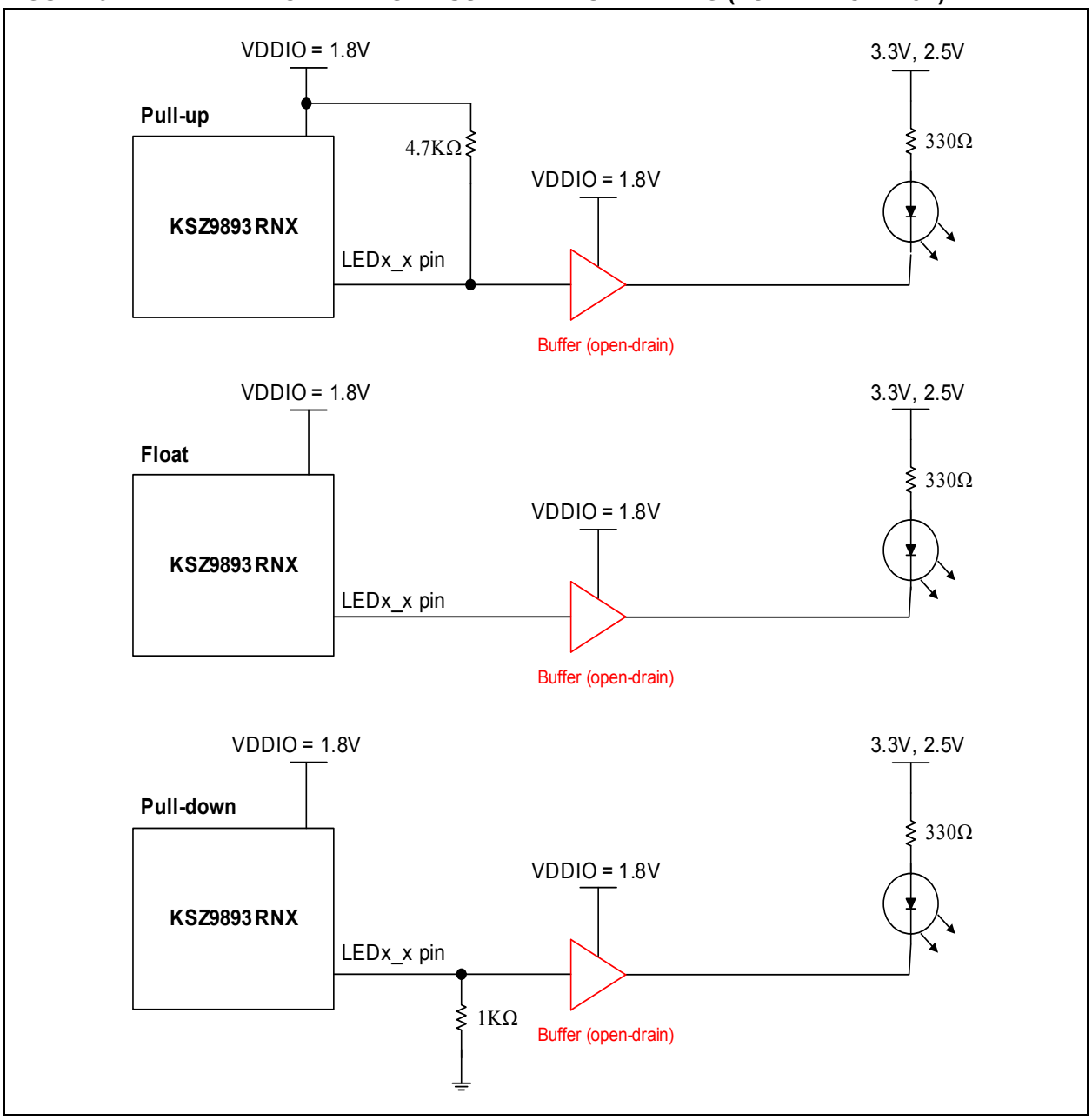
FIGURE 9-1: PHY PORT LED STATUS AND PIN STRAPPING (FOR VDDIO = 3.3V OR 2.5V)



9.2 PHY Port LED Status and Pin Strapping (for VDDIO = 1.8V)

Figure 9-2 shows the pull-up, float, and pull-down reference circuits for the multiplexed PHY port LED status and pin strapping for 1.8V VDDIO. The open-drain buffers serve as level shifters and are needed to turn on the LED indicators which requires voltage drops of 1.6V to 2.2V, depending on the LED color.

FIGURE 9-2: PHY PORT LED STATUS AND PIN STRAPPING (FOR VDDIO = 1.8V)



10.0 MISCELLANEOUS

10.1 INTRP_N Output

The INTRP_N (pin 45) is the interrupt output. It is active low and requires an external 1.0-kΩ-to-4.7-kΩ pull-up resistor to the KSZ9893RNX VDDIO power rail.

Refer to the *KSZ9893 Data Sheet* for configurable interrupt events.

10.2 PME_N Output

The PME_N (pin 44) output provides the Power Management Event (PME) interrupt output for the Wake-on-LAN (WoL) function. When the PME_N pin is asserted, it indicates the KSZ9893RNX device has detected an energy event and is outputting the interrupt to wake up the system from a Low-power mode.

The PME_N asserted polarity is programmable (default is active low). An external pull-up resistor is required for active-low operation, while an external pull-down resistor is required for active-high operation. For both cases, the external resistor value is 1.0 kΩ to 4.7 kΩ.

Refer to *KSZ9893 Data Sheet* for further details and usage on the PME_N signal and WoL function.

10.3 EMI Consideration

Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leaving the footprint open will allow the two grounds to remain separate. Shorting them together with a zero-ohm resistor will connect them. For best performance, short them together with a cap or a ferrite bead.

11.0 REFERENCE MATERIALS

Check the Microchip website, www.microchip.com, for the latest version of the following KSZ9893RNX collaterals:

- *KSZ9893RNX Data Sheet*
- *KSZ9893RNX Silicon Errata and Data Sheet Clarification*
- KSZ9893R IBIS Model
- EVB-KSZ9563 Board Schematic and PCB Layout
- *EVB-KSZ9563 Evaluation Board User's Guide*

12.0 HARDWARE CHECKLIST SUMMARY

TABLE 12-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "Package and Pin Considerations"	Section 2.1, "Package Orientation and Pin Numbering"	Verify if the schematic drawing matches the package orientation and pin number of *KSZ9893RNX Datasheet*.		
	Section 2.2, "Pin Type"	Ensure that pin type is compatible to all pins between KSZ9893RNX device and interfacing components (e.g., ensure input is not connected to input).		
	Section 2.3, "Configuration Strap Pins"	Ensure that the intended pin strapping is selected. Add external pull-ups/pull-downs (as needed) to prevent connecting components from overriding the intended high/low value.		
Section 3.0, "Reference Clock Circuits and Connections"	Section 3.1, "Crystal Circuit"	If selected, follow crystal circuit recommendation and crystal specifications (25 MHz, +/–50 ppm, less than 100 ps total period jitter peak-to-peak)		
	Section 3.2, "External Clock Source/Oscillator Circuit"	If selected, follow external clock/oscillator recommendation and clock specifications (25 MHz, +/–50 ppm, less than 100 ps total period jitter peak-to-peak)		
Section 4.0, "Power/ Ground Connections"	Section 4.1.1, "Power pins"	Ensure that each power pin has a 0.1 uF decoupling capacitor and each power rail (AVDDH, VDDIO, AVDDL, and DVDDL) has sufficient bulk storage capacitance for less than 50 mVp-p ripple. Use ferrite beads to provide further filtering for analog power rails (AVDDH and AVDDL).		
	Section 4.1.2, "Ground pin and exposed pad"	Ensure that ground and exposed pad are tied directly to a common ground plane. Use recommended land pattern and thermal vias for the exposed pad.		
Section 5.0, "ISET Resistor"	Section 5.0, "ISET Resistor" (Pin connection and resistor value)	Ensure that resistor value is 6.04 kΩ 1% and is placed close to ISET pin.		
Section 6.0, "Ethernet PHY Ports"	Section 6.1, "Ethernet Signal Pins"	Ensure that no external termination is placed on the differential signals for the PHY ports and the magnetic center taps on the KSZ9893RNX device side are not shorted together and are not connected to any external power rail.		
	Section 6.2, "Magnetics Selection"	Ensure selected magnetic has separated center taps for the four differential pairs on the KSZ9893RNX device side.		
	Section 6.3, "Magnetic and RJ45 Plug Connections"/Section 6.3.1, "10/100/1000 Mbps (Gigabit) Ethernet"	If selected, ensure that magnetic and RJ45 connections match FIGURE 6-1: Gigabit Ethernet Connections on page 7.		
	Section 6.3, "Magnetic and RJ45 Plug Connections"/Section 6.3.2, "10/100 Mbps (Fast) Ethernet only"	If selected, ensure that magnetic and RJ45 connections match FIGURE 6-2: Fast Ethernet Magnetic Connections (MDI Mode) on page 9, or FIGURE 6-3: Fast Ethernet Magnetic Connections (MDI-X Mode) on page 10.		

TABLE 12-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 7.0, "Management Bus Selection"	Section 7.1, "SPI Slave Management"	If selected, ensure pin strapping and SPI pin connections match FIGURE 7-1: SPI Block Diagram on page 12.		
	Section 7.2, "I²C Slave Management"	If selected, ensure pin strapping and I²C pin connections match FIGURE 7-2: I²C Block Diagram on page 13.		
	Section 7.3, "In-Band Access (IBA) Management"	If selected, ensure pin strapping and IBA pin connections match FIGURE 7-3: IBA Block Diagram on page 13		
	Section 7.4, "MII Management (MIIM)"	If selected, ensure pin strapping and MIIM pin connections match FIGURE 7-4: MII Management Block Diagram on page 14. Note that MIIM is limited to PHY register access only.		
Section 8.0, "MAC Port 3 – Digital Data Bus Interfaces"	Section 8.1, "RGMII Interface"/ Section 8.1.1, "RGMII Functional Configuration"	If selected, determine the KSZ9893RNX RGMII functional configuration (RGMII-ID mode, Hybrid mode, or RGMII mode) to be used with the external RGMII device using FIGURE 8-1: KSZ9893RNX and External RGMII Device (MAC Pin Definition) – RGMII Functional Configuration with On-chip Clock Delay Options on page 16.		
	Section 8.1, "RGMII Interface" / Section 8.1.2, "RGMII Skew Calculation"	If selected, determine the RGMII skew using FIGURE 8-2: RGMII Clock Skew Diagram on page 17.		
	Section 8.1, "RGMII Interface" / Section 8.1.3, "RGMII Interface with External RGMII Device"	If selected, ensure that RGMII connections match either FIGURE 8-3: KSZ9893RNX RGMII and External RGMII Device (MAC Pin Definition) – Block Diagram on page 18, or FIGURE 8-4: KSZ9893RNX RGMII and External RGMII Device (PHY Pin Definition) – Block Diagram on page 19.		
	Section 8.2, "RMII (Clock Mode) Interface"	If selected, ensure that RMII connections match Section FIGURE 8-5:, "KSZ9893RNX RMII (Clock Mode) and External RMII Device (MAC pin definition) – Block Diagram".		
	Section 8.3, "RMII (Normal Mode) Interface"	If selected, ensure that RMII connections match FIGURE 8-6: KSZ9893RNX RMII (Normal Mode) and External RMII DEVICE (PHY PIN DEFINITION) – Block Diagram on page 22.		
	Section 8.4, "MII (MAC Mode) Interface"	If selected, ensure that MII connections match FIGURE 8-7: KSZ9893RNX MII (MAC Mode) and External MII PHY – Block Diagram on page 23.		
	Section 8.5, "MII (PHY Mode) Interface"	If selected, ensure that MII connections match FIGURE 8-8: KSZ9893RNX MII (PHY Mode) and External MII MAC – Block Diagram on page 25.		
Section 9.0, "LED Indicator Pins"	Section 9.1, "PHY Port LED Status and Pin Strapping (for VDDIO = 3.3V or 2.5V)"	If selected, ensure that LED connections match FIGURE 9-1: PHY Port LED Status and Pin Strapping (for VDDIO = 3.3V or 2.5V) on page 27.		
	Section 9.2, "PHY Port LED Status and Pin Strapping (for VDDIO = 1.8V)"	If selected, ensure that LED connections match FIGURE 9-2: PHY Port LED Status and Pin Strapping (for VDDIO = 1.8V) on page 28.		
Section 10.0, "Miscellaneous"	Section 10.1, "INTRP_N Output"	If used, ensure that there is a 1.0-kΩ-to-4.7-kΩ pull-up resistor to the VDDIO power rail.		
	Section 10.2, "PME_N Output"	If used, ensure that there is a 1.0-kΩ-to-4.7-kΩ resistor pulled up to the VDDIO power rail for active low or pulled-down to ground for active high.		
	Section 10.3, "EMI Consideration"	Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level and Date	Section/Figure/Entry	Correction
DS00002756A (08-10-18)	All	Initial release

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