

**TrenchMOS™ transistor**  
**Logic level FET**

**BUK9528-100A**  
**BUK9628-100A**

**GENERAL DESCRIPTION**

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope available in TO220AB and SOT404 . Using 'trench' technology which features very low on-state resistance. It is intended for use in automotive and general purpose switching applications.

**QUICK REFERENCE DATA**

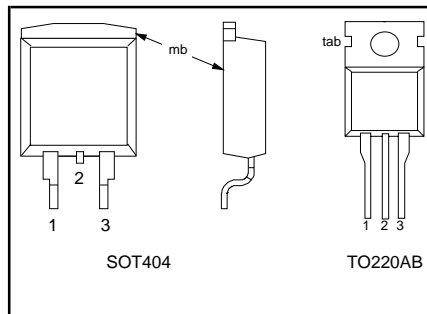
SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Drain-source voltage	100	V
$I_D$	Drain current (DC)	49	A
$P_{tot}$	Total power dissipation	166	W
$T_j$	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	28	mΩ
	$V_{GS} = 5 V$	27	mΩ
	$V_{GS} = 10 V$		

**PINNING**

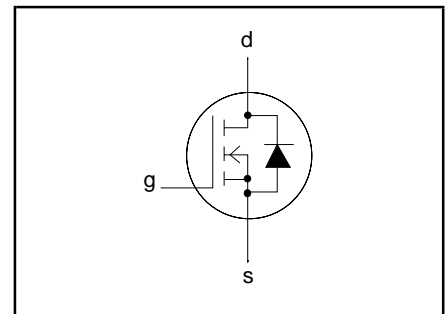
**TO220AB & SOT404**

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab/mb	drain

**PIN CONFIGURATION**



**SYMBOL**



**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	100	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20 k\Omega$	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \le 50 \mu S$	-	15	V
$I_D$	Drain current (DC)	$T_{mb} = 25 \text{ }^\circ C$	-	49	A
$I_D$	Drain current (DC)	$T_{mb} = 100 \text{ }^\circ C$	-	34	A
$I_{DM}$	Drain current (pulse peak value)	$T_{mb} = 25 \text{ }^\circ C$	-	195	A
$P_{tot}$	Total power dissipation	$T_{mb} = 25 \text{ }^\circ C$	-	166	W
$T_{stg}, T_j$	Storage & operating temperature	-	- 55	175	°C

**THERMAL RESISTANCES**

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th j-mb}$	Thermal resistance junction to mounting base	-	-	0.9	K/W
$R_{th j-a}$	Thermal resistance junction to ambient(TO220AB)	in free air	60	-	K/W
$R_{th j-a}$	Thermal resistance junction to ambient(SOT404)	Minimum footprint, FR4 board	50	-	K/W

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**STATIC CHARACTERISTICS**
 $T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}; T_j = -55^\circ\text{C}$	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$	89	-	-	V
			1	1.5	2.0	V
			0.5	-	-	V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_j = 175^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
			-	-	500	$\mu\text{A}$
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}; T_j = 175^\circ\text{C}$	-	2	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 175^\circ\text{C}$	-	18.5	28	m $\Omega$
			-	-	70	m $\Omega$
			-	17	27	m $\Omega$
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}$	-	18.8	31	m $\Omega$
		$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}$	-	-	-	m $\Omega$

**DYNAMIC CHARACTERISTICS**
 $T_{mb} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	3220	4293	pF
$C_{oss}$	Output capacitance		-	315	378	pF
$C_{rss}$	Feedback capacitance		-	187	256	pF
$t_{d\text{ on}}$	Turn-on delay time	$V_{DD} = 30\text{ V}; R_{load} = 1.2\Omega; V_{GS} = 5\text{ V}; R_G = 10\Omega$	-	11	16	ns
$t_r$	Turn-on rise time		-	58	87	ns
$t_{d\text{ off}}$	Turn-off delay time		-	250	350	ns
$t_f$	Turn-off fall time		-	106	148	ns
$L_d$	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
$L_d$	Internal drain inductance	Measured from contact screw on tab to centre of die(TO220AB)	-	3.5	-	nH
$L_d$	Internal drain inductance	Measured from upper edge of drain tab to centre of die(SOT404)	-	2.5	-	nH
$L_s$	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH

**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS**
 $T_j = 25^\circ\text{C}$  unless otherwise specified

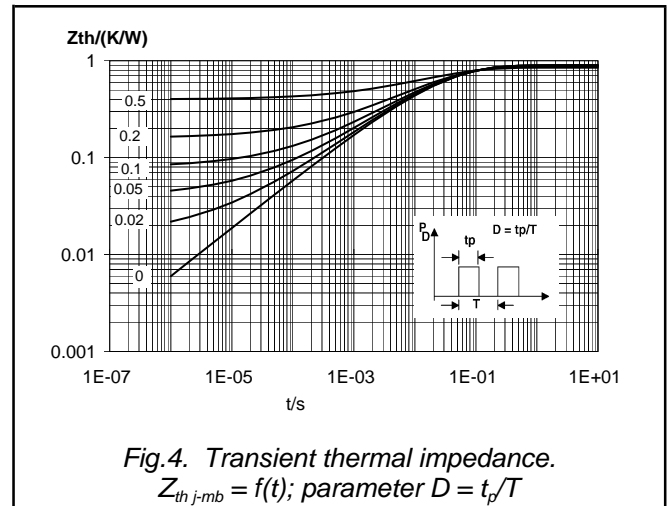
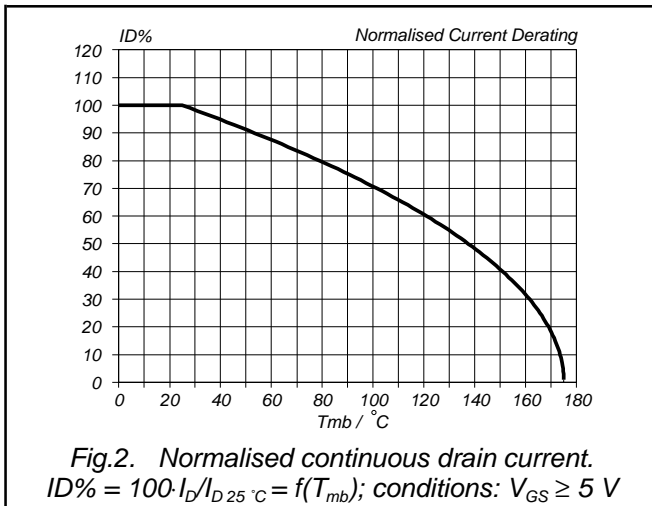
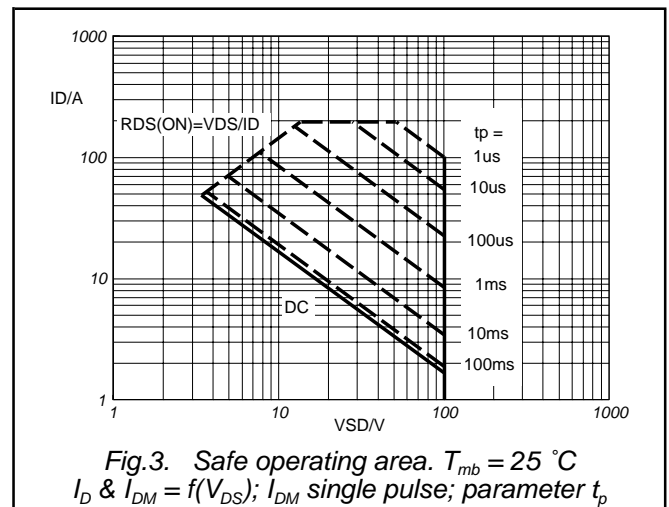
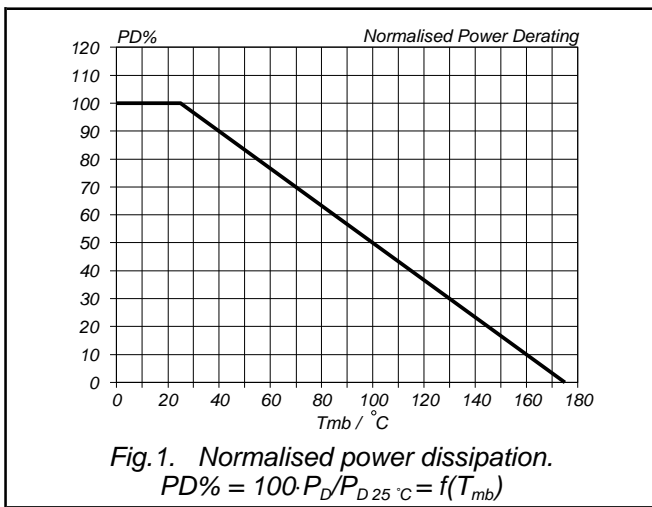
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current		-	-	49	A
$I_{DRM}$	Pulsed reverse drain current		-	-	195	A
$V_{SD}$	Diode forward voltage	$I_F = 25\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.2	V
		$I_F = 49\text{ A}; V_{GS} = 0\text{ V}$	-	1.1	-	V
$t_{rr}$	Reverse recovery time	$I_F = 49\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s}; V_{GS} = -10\text{ V}; V_R = 30\text{ V}$	-	63	-	ns
$Q_{rr}$	Reverse recovery charge		-	0.22	-	$\mu\text{C}$

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**AVALANCHE LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}^1$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 30\text{ A}; V_{DD} \leq 25\text{ V}; V_{GS} = 5\text{ V}; R_{GS} = 50\ \Omega; T_{mb} = 25\text{ }^\circ\text{C}$	-	-	45	mJ



1 For maximum permissible repetitive avalanche current see fig.18.

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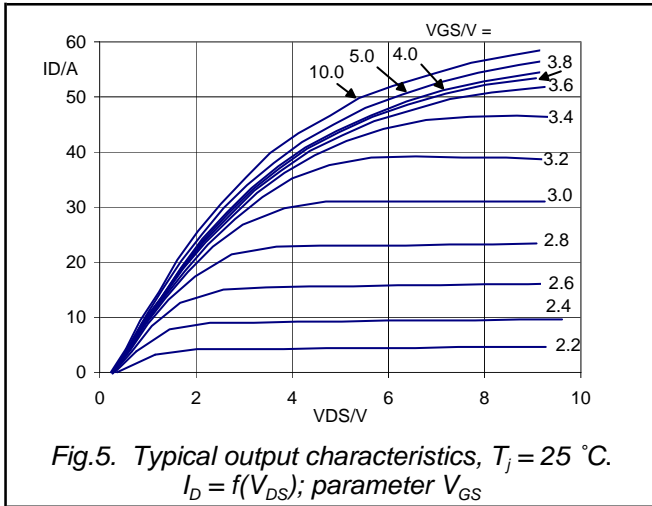


Fig.5. Typical output characteristics,  $T_j = 25\text{ }^\circ\text{C}$ .  
 $I_D = f(V_{DS})$ ; parameter  $V_{GS}$

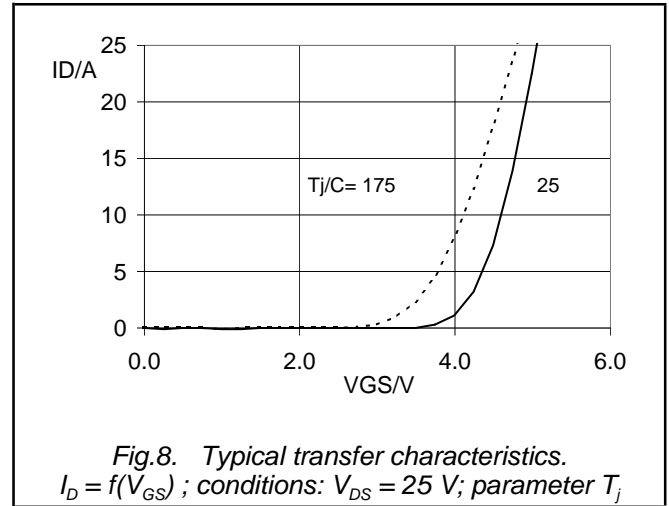


Fig.8. Typical transfer characteristics.  
 $I_D = f(V_{GS})$ ; conditions:  $V_{DS} = 25\text{ V}$ ; parameter  $T_j$

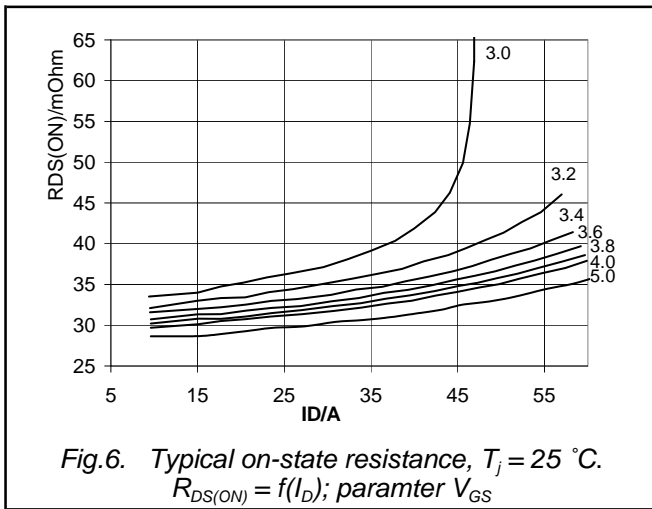


Fig.6. Typical on-state resistance,  $T_j = 25\text{ }^\circ\text{C}$ .  
 $R_{DS(ON)} = f(I_D)$ ; parameter  $V_{GS}$

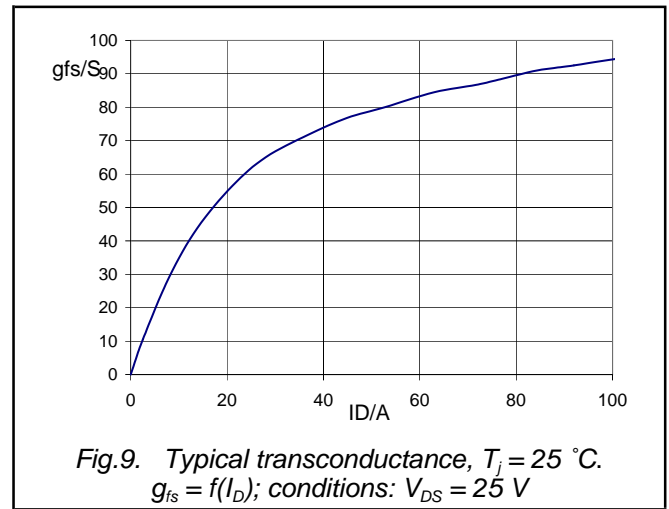


Fig.9. Typical transconductance,  $T_j = 25\text{ }^\circ\text{C}$ .  
 $g_{fs} = f(I_D)$ ; conditions:  $V_{DS} = 25\text{ V}$

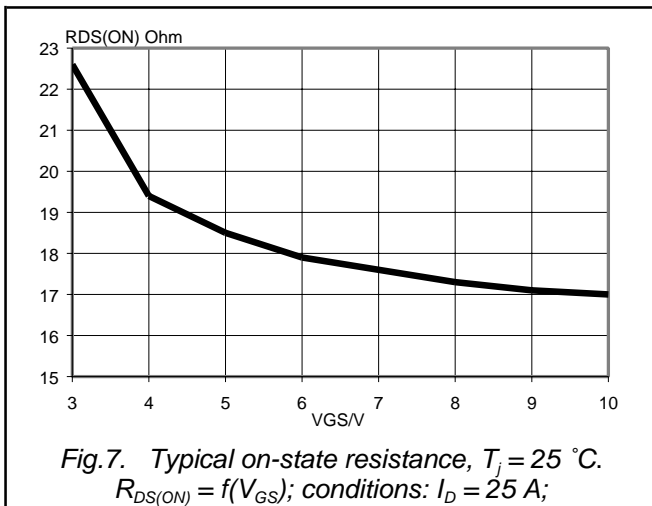


Fig.7. Typical on-state resistance,  $T_j = 25\text{ }^\circ\text{C}$ .  
 $R_{DS(ON)} = f(V_{GS})$ ; conditions:  $I_D = 25\text{ A}$ ;

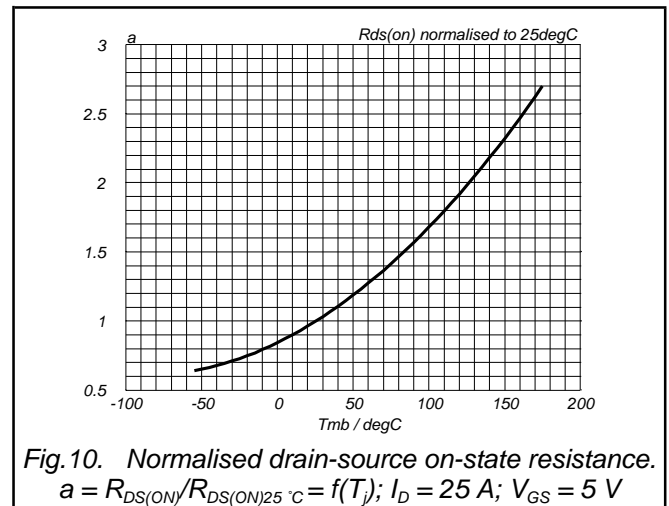
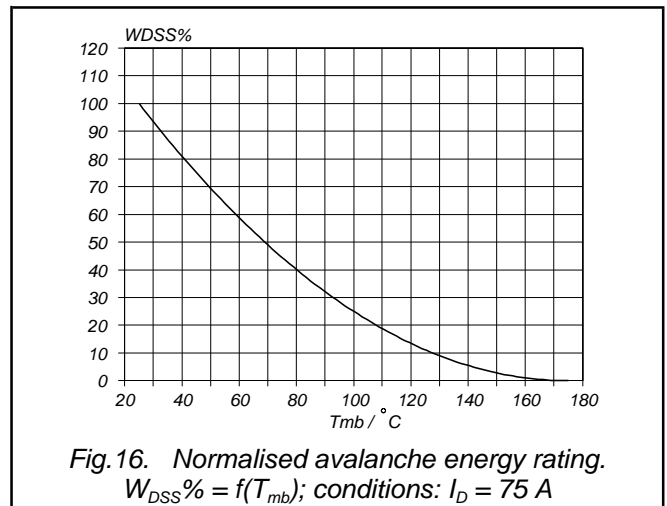
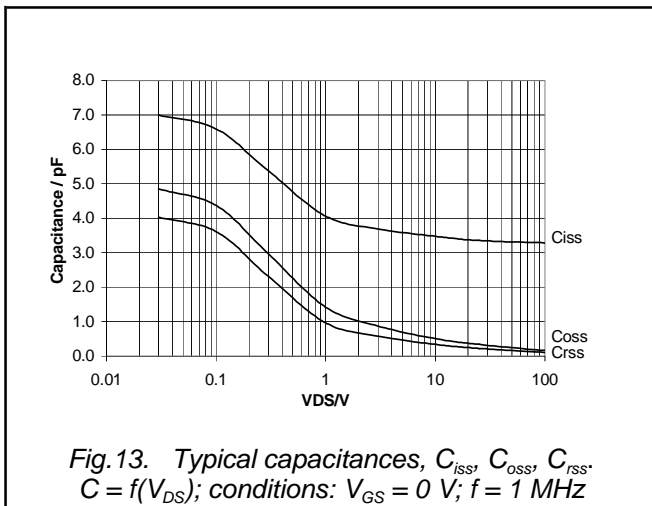
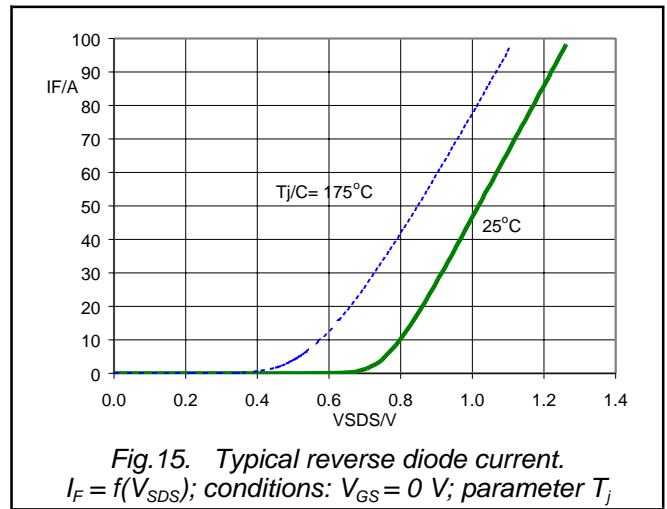
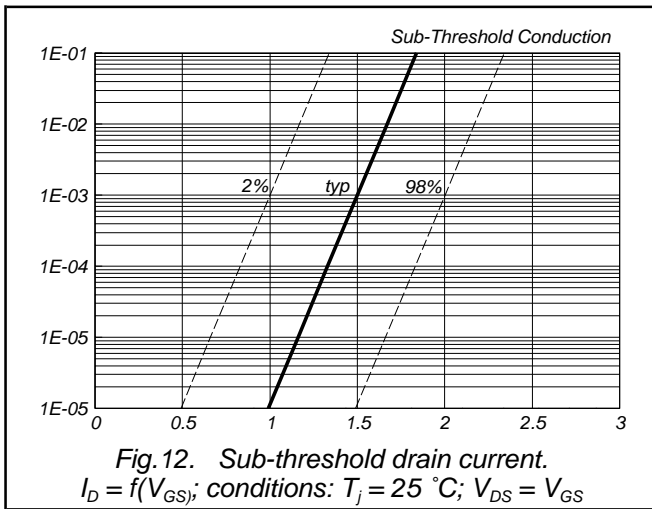
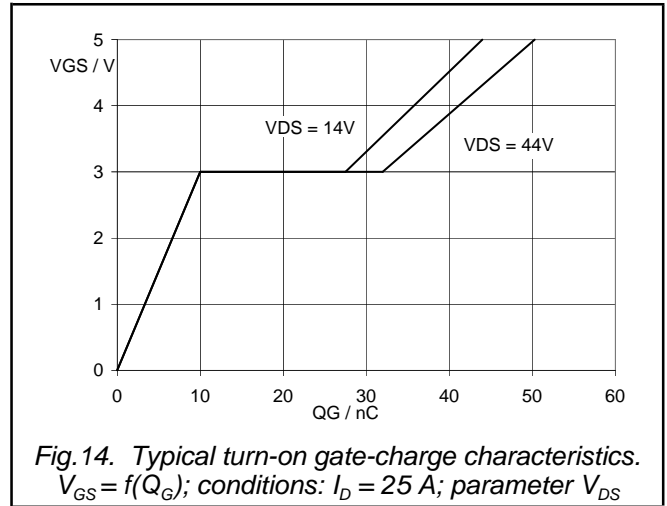
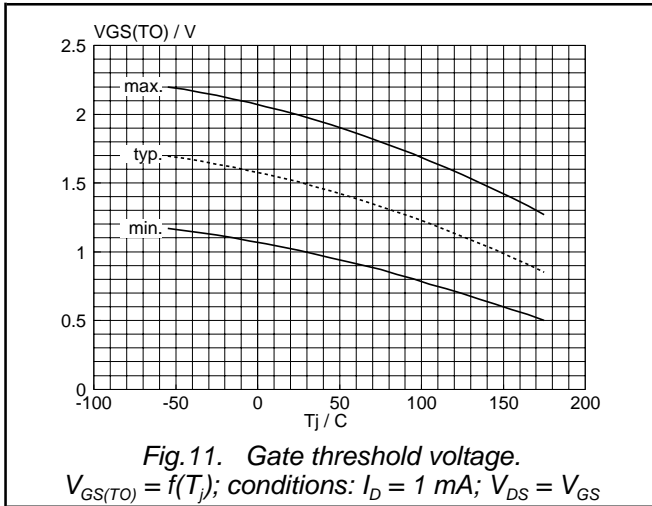


Fig.10. Normalised drain-source on-state resistance.  
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ }^\circ\text{C}} = f(T_j)$ ;  $I_D = 25\text{ A}$ ;  $V_{GS} = 5\text{ V}$

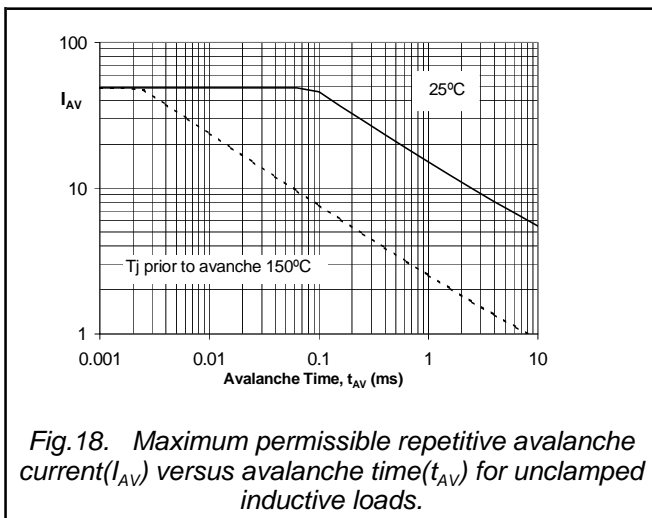
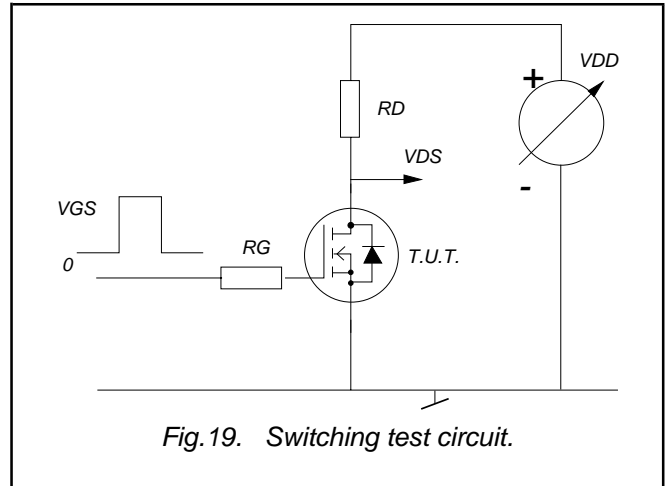
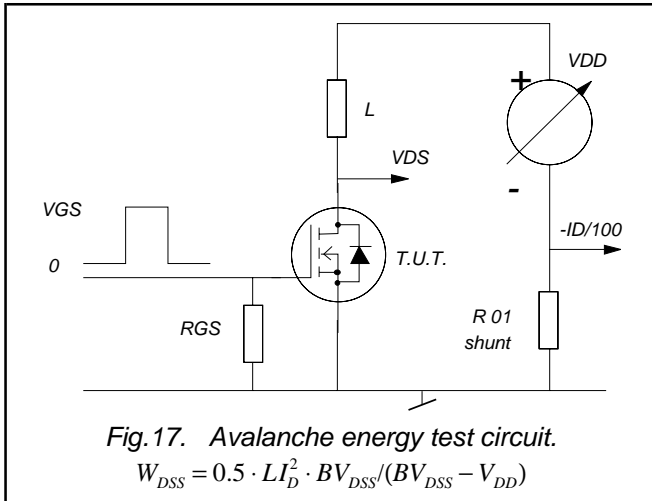
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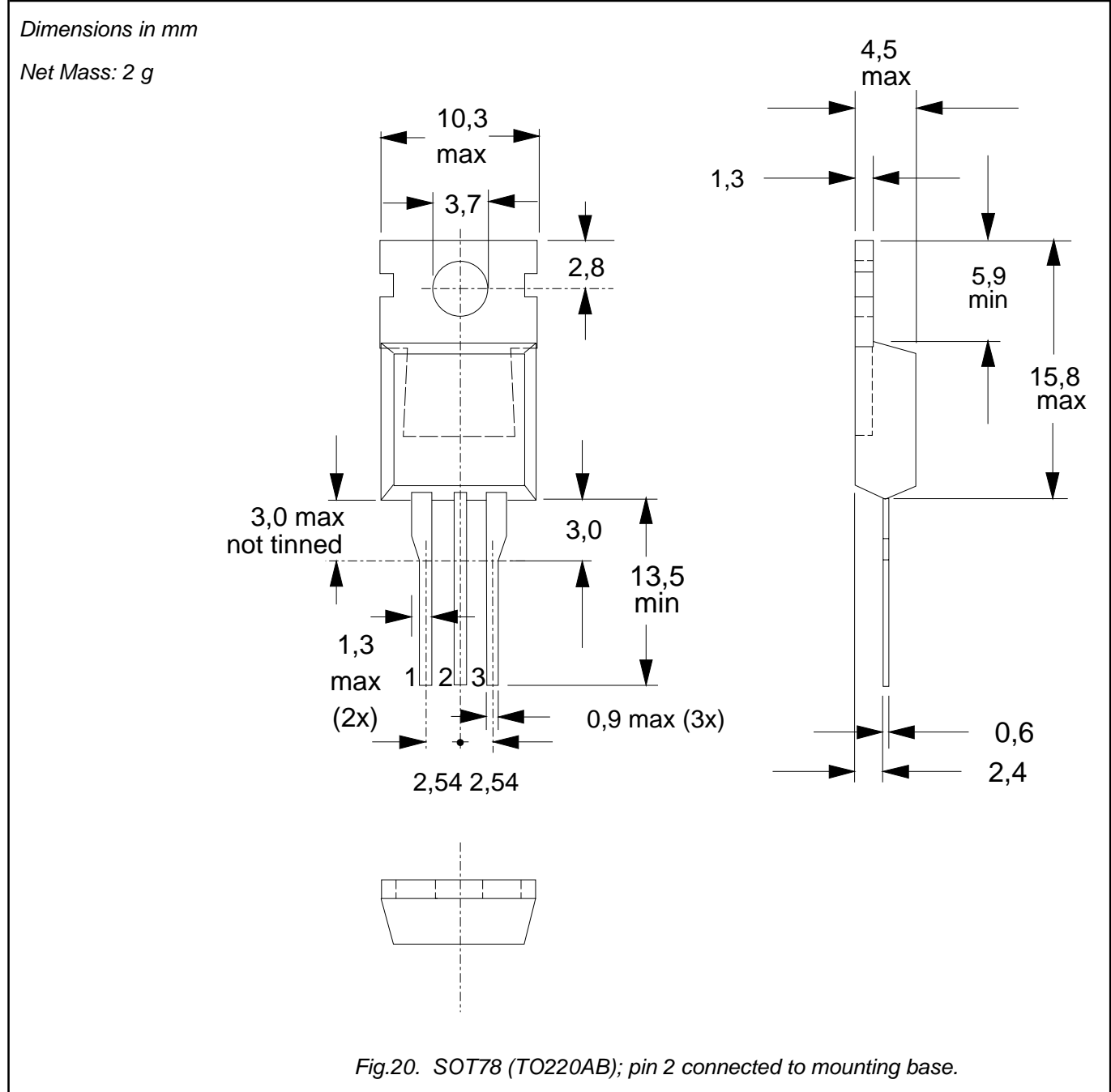
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BUK9528-100A  
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**MECHANICAL DATA**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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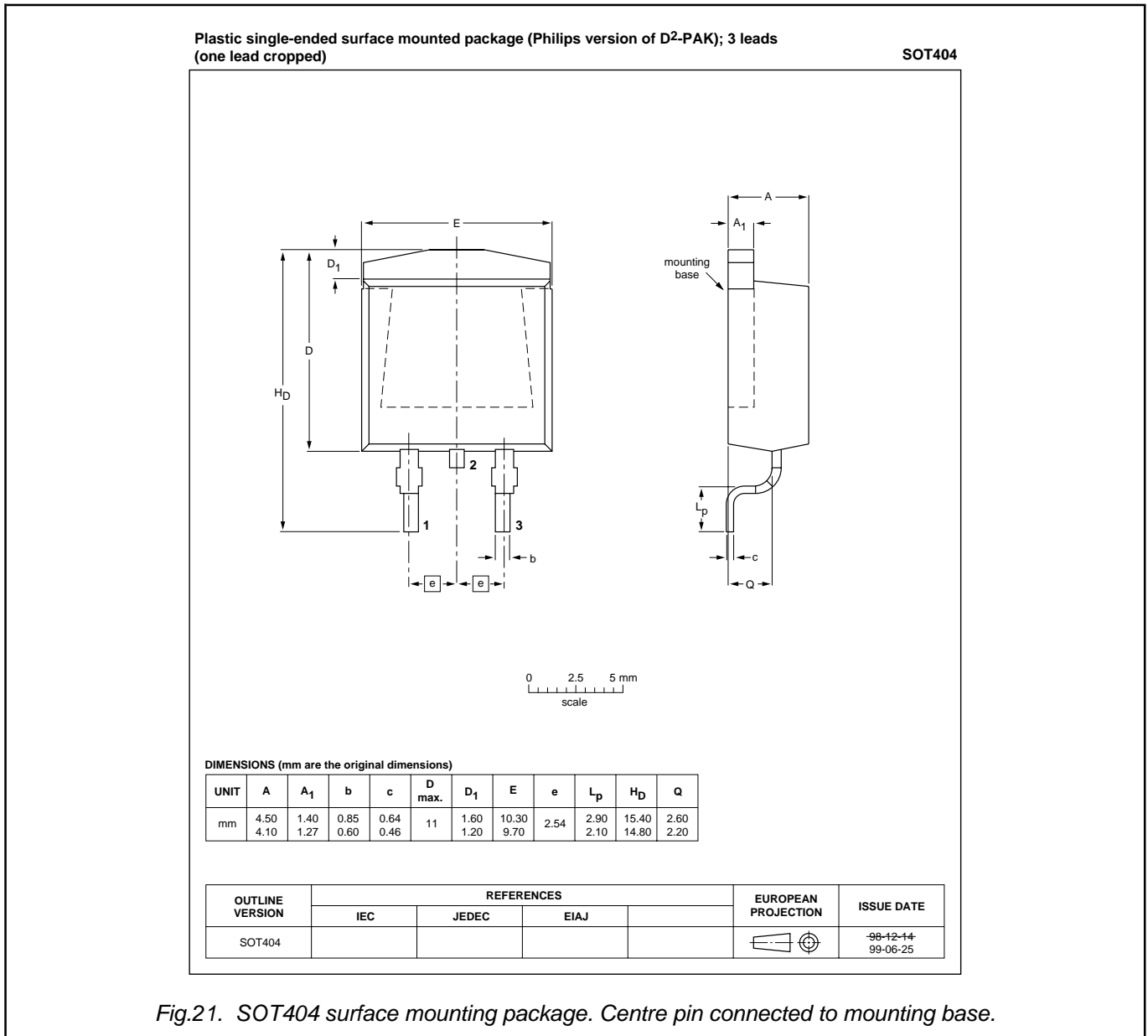


Fig.21. SOT404 surface mounting package. Centre pin connected to mounting base.

**Notes**

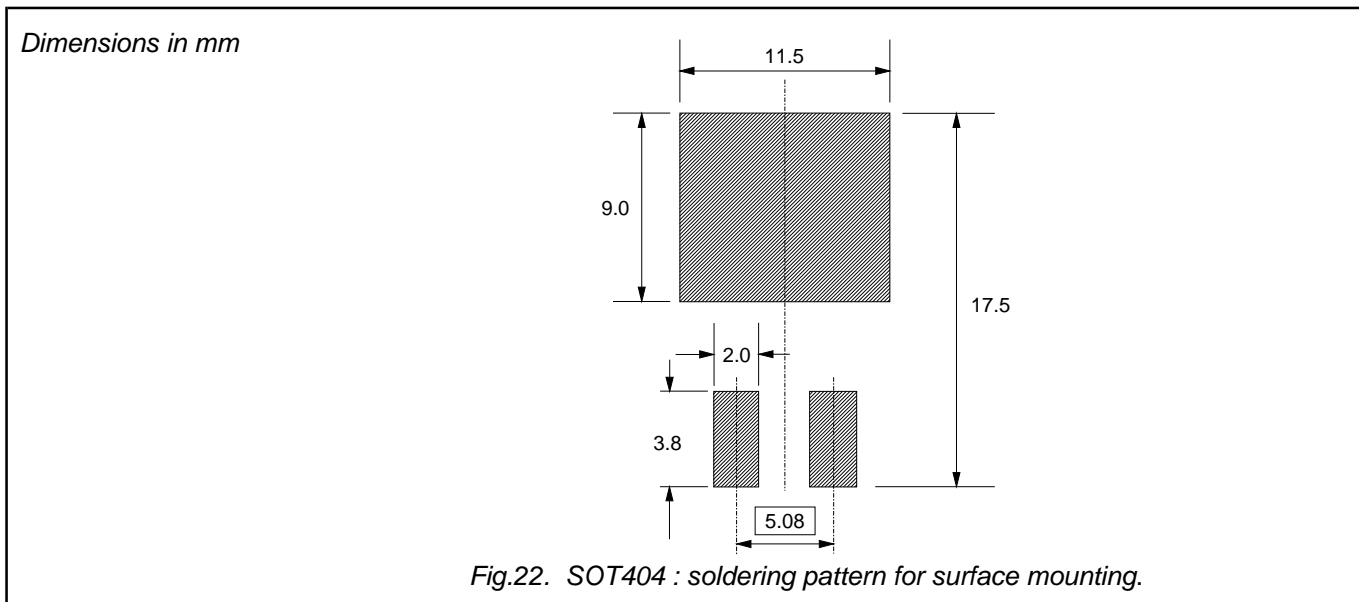
1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".



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**MOUNTING INSTRUCTIONS**



**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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