Dual N-Channel Power MOSFET

40V, 37A, 15mΩ

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Logic level
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

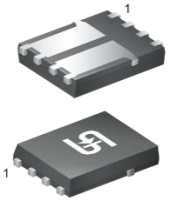
KEY PERFORMANCE PARAMETERS			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		40	V
$R_{DS(on)}$ (max)	V_{GS} = 10V	15	mΩ
	V_{GS} = 4.5V	19	
Q_g		9	nC

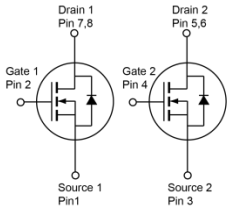
APPLICATIONS

- BLDC Motor Control
- Battery Power Management
- DC-DC Converter
- Secondary Synchronous Rectification

Pb-Free RoHS COMPLIANT HALOGEN FREE

PDFN56 Dual





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	37	A
	T_A = 25°C		8	
Pulsed Drain Current		I_{DM}	148	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	14	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	29	mJ
Total Power Dissipation	T_C = 25°C	P_D	40	W
	T_C = 125°C		8	
Total Power Dissipation	T_A = 25°C	P_D	2	W
	T_A = 125°C		0.4	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	3.1	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	61	°C/W

Thermal Performance Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. The $R_{\Theta JA}$ limit presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	40	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	1	1.7	2.5	V
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 40V	I_{DSS}	--	--	1	μA
	V_{GS} = 0V, V_{DS} = 40V T_J = 125°C		--	--	100	
Drain-Source On-State Resistance (Note 3)	V_{GS} = 10V, I_D = 8A	$R_{DS(on)}$	--	10	15	mΩ
	V_{GS} = 4.5V, I_D = 7A		--	14	19	
Forward Transconductance (Note 3)	V_{DS} = 10V, I_D = 8A	g_{fs}	--	32	--	S
Dynamic (Note 4)						
Total Gate Charge	V_{GS} = 10V, V_{DS} = 20V, I_D = 8A	Q_g	--	18	--	nC
Total Gate Charge	V_{GS} = 4.5V, V_{DS} = 20V, I_D = 7A	Q_g	--	9	--	
Gate-Source Charge		Q_{gs}	--	3	--	
Gate-Drain Charge		Q_{gd}	--	5	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = 20V, f = 1.0MHz	C_{iss}	--	966	--	pF
Output Capacitance		C_{oss}	--	108	--	
Reverse Transfer Capacitance		C_{rss}	--	64	--	
Gate Resistance	f = 1.0MHz	R_g	0.6	1.9	3.8	Ω
Switching (Note 4)						
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 20V, I_D = 8A, R_G = 2Ω	$t_{d(on)}$	--	1	--	ns
Turn-On Rise Time		t_r	--	19	--	
Turn-Off Delay Time		$t_{d(off)}$	--	10	--	
Turn-Off Fall Time		t_f	--	12	--	
Source-Drain Diode						
Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 8A	V_{SD}	--	--	1.2	V
Reverse Recovery Time	I_S = 8A, dI/dt = 100A/μs	t_{rr}	--	12	--	ns
Reverse Recovery Charge		Q_{rr}	--	5	--	nC

Notes:

1. Silicon limited current only.
2. L = 0.3mH, V_{GS} = 10V, V_{DD} = 25V, R_G = 25Ω, I_{AS} = 14A, Starting T_J = 25°C
3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

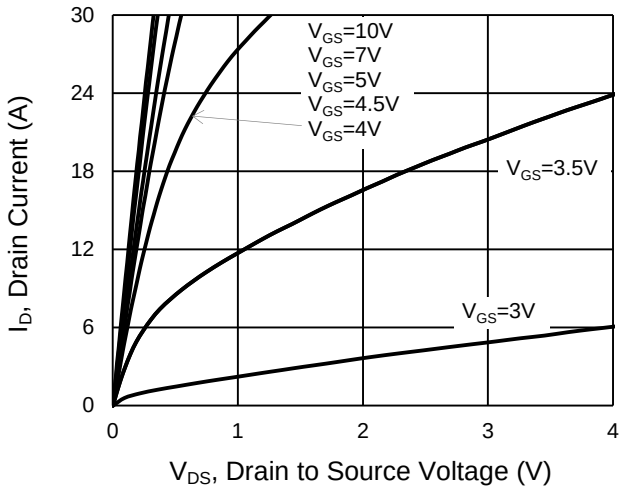
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM150NB04LDCR RLG	PDFN56 Dual	2,500pcs / 13” Reel

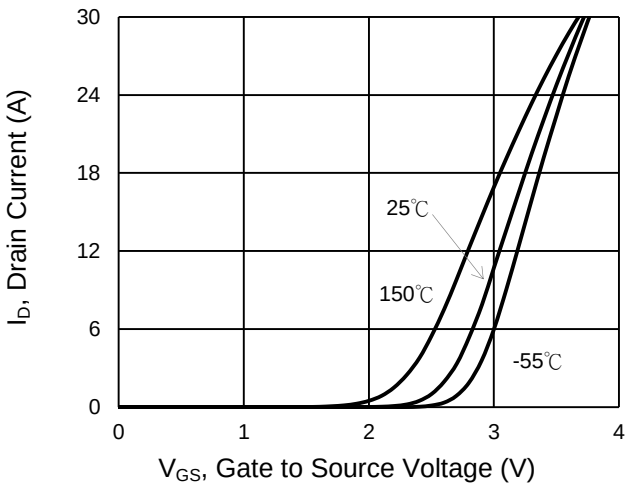
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

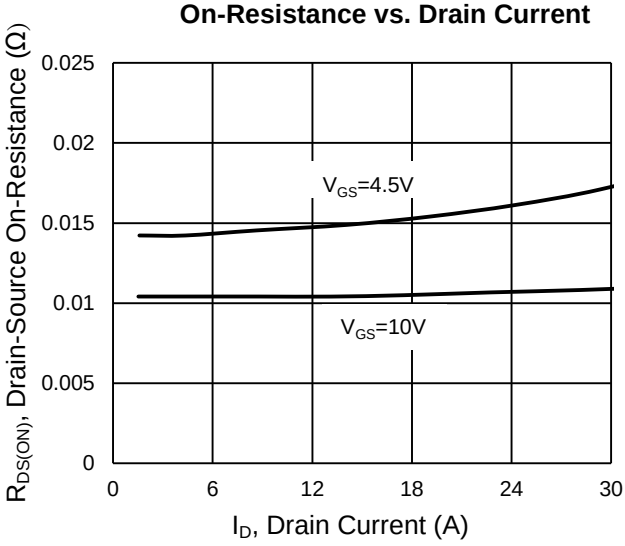
Output Characteristics



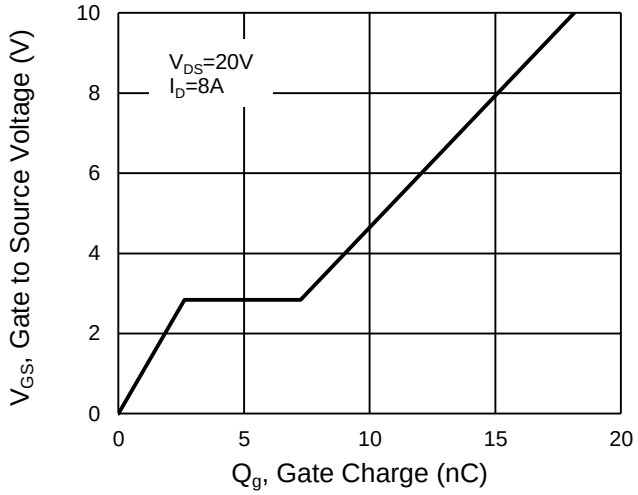
Transfer Characteristics



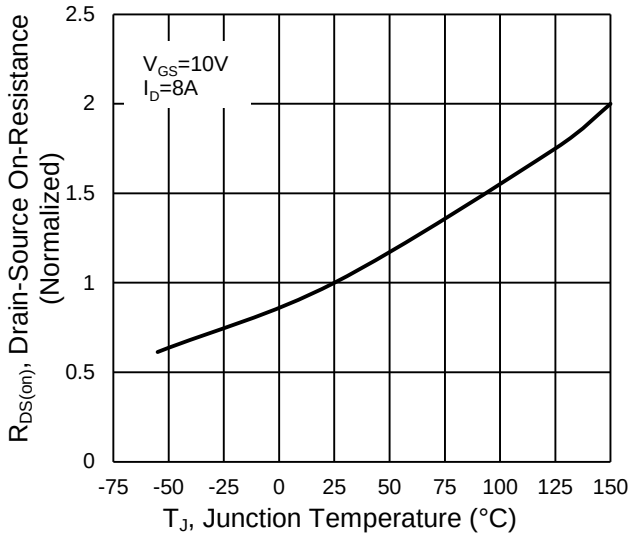
On-Resistance vs. Drain Current



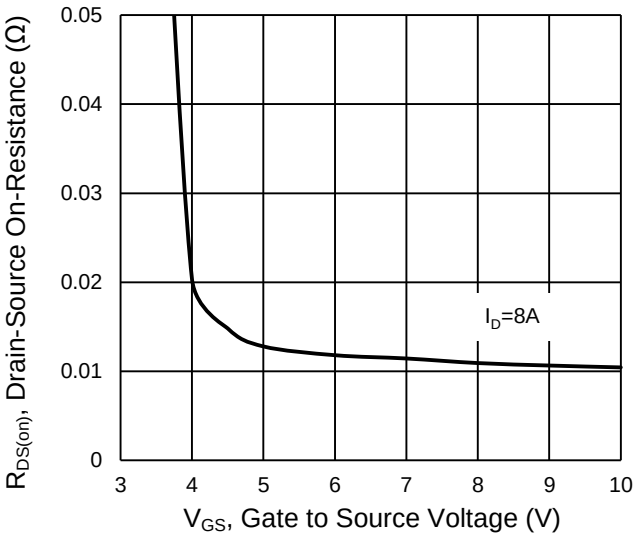
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



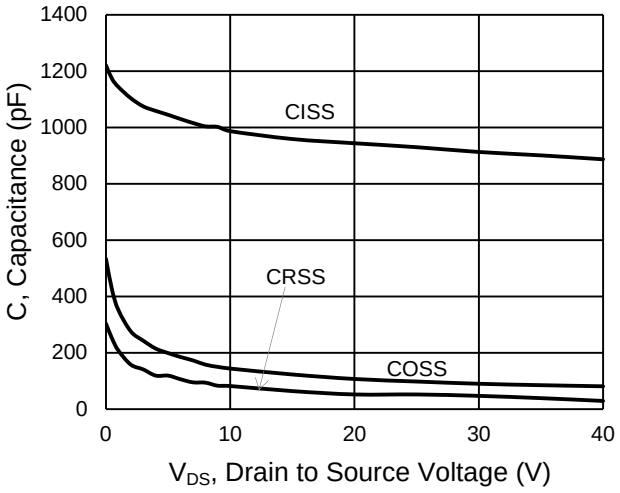
On-Resistance vs. Gate-Source Voltage



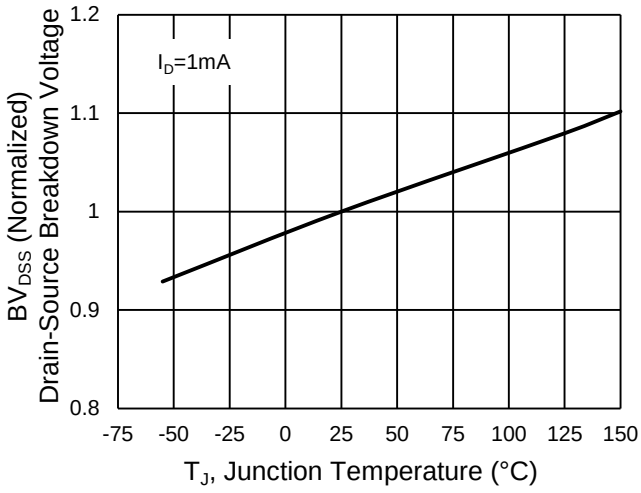
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

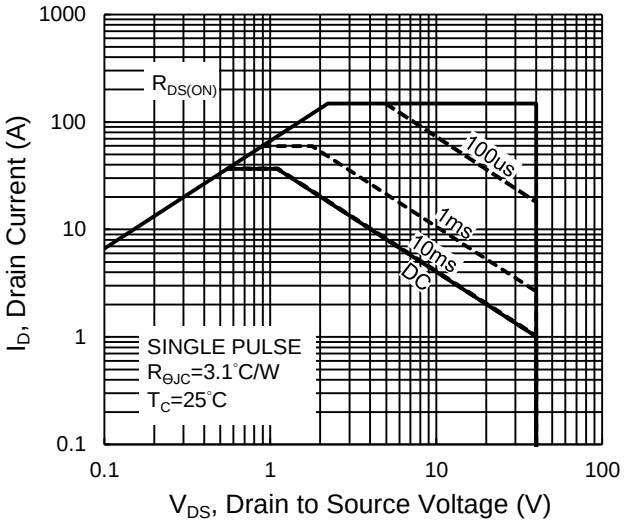
Capacitance vs. Drain-Source Voltage



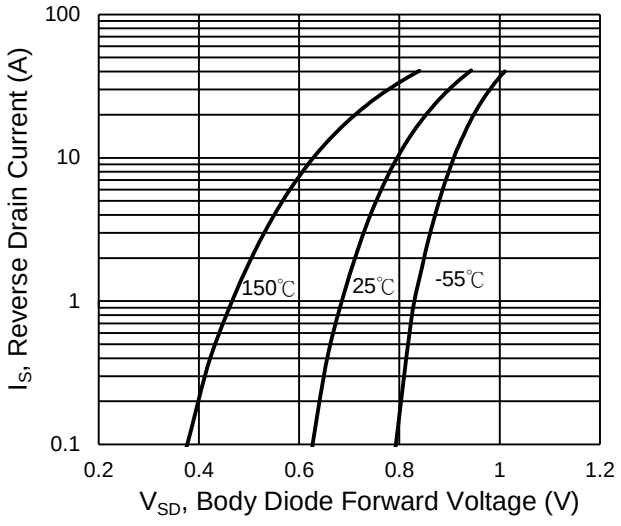
BV_{DSS} vs. Junction Temperature



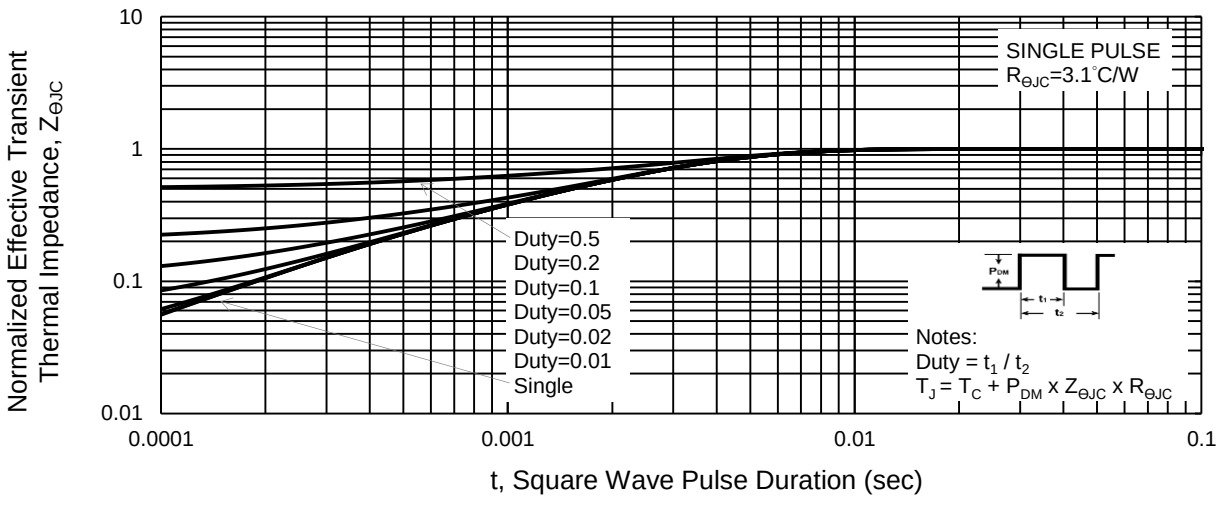
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

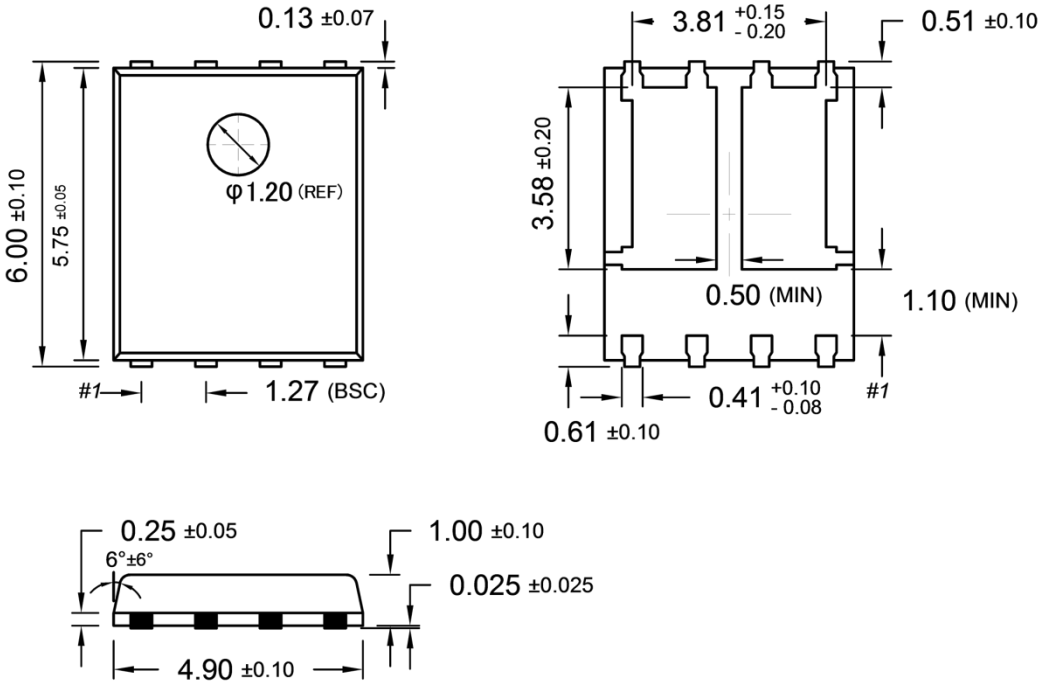


Normalized Thermal Transient Impedance, Junction-to-Case

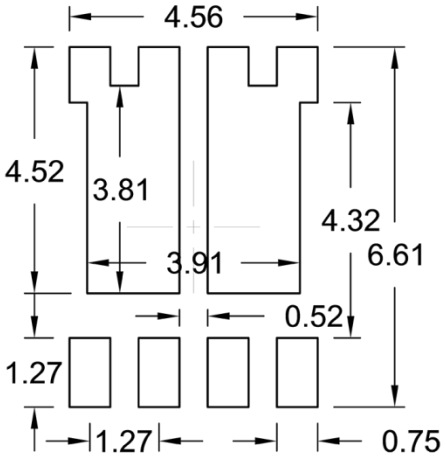


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

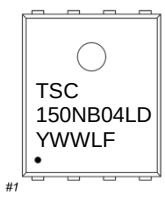
PDFN56 Dual



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code
WW = Week Code (01~52)
L = Lot Code (1~9,A~Z)
F = Factory Code

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