MC74VHCT574A

Octal D-Type Flip-Flop with 3-State Output

The MC74VHCT574A is an advanced high speed CMOS octal flip−flop with 3−state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This 8−bit D−type flip−flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT574A input and output (when disabled) structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage−input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: f_{max} = 140 MHz (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- TTL−Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 1.6 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
    Human Body Model > 2000 V;
    Machine Model > 200 V
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant

ON Semiconductor®
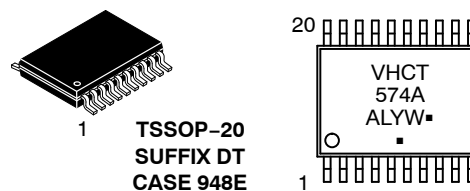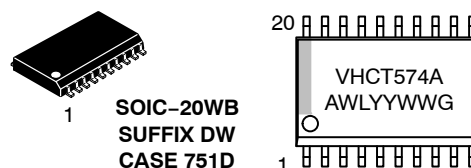
http://onsemi.com

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CP	D	Q
L	⌐	H	H
L	⌐	L	L
L	L, H, ⌐	X	No Change
H	X	X	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.
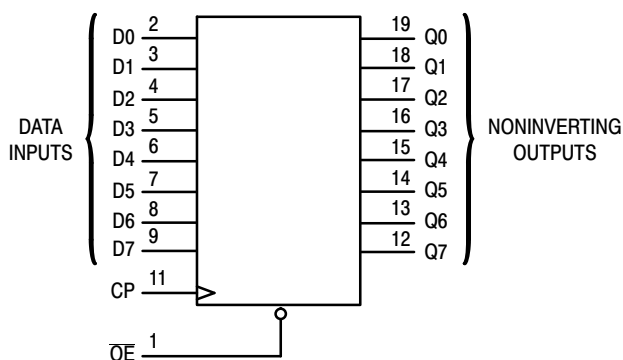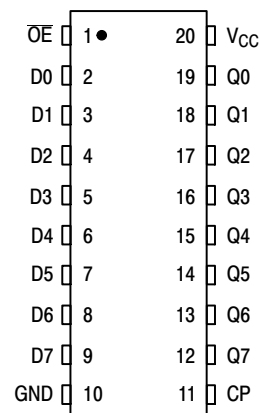
MC74VHCT574A

Figure 1. Logic Diagram

Figure 2. Pin Assignment

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		− 0.5 to + 7.0	V
V_{in}	DC Input Voltage		− 0.5 to + 7.0	V
V_{out}	DC Output Voltage	Outputs in 3−State High or Low State	− 0.5 to + 7.0 − 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current		− 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})		± 20	mA
I_{out}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 75	mA
P_D	Power Dissipation in Still Air,	SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature		− 65 to + 150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
†Derating − SOIC Packages: − 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage	Outputs in 3−State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature		− 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} =5.0V ±0.5V	0	20	ns/V

MC74VHCT574A

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25°C$ Min	Typ	Max	$T_A = -40$ to $85°C$ Min	Max	Unit
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -50µA$	4.5	4.4	4.5		4.4		V
		$I_{OH} = -8mA$	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage $V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 50µA$	4.5		0.0	0.1		0.1	V
		$I_{OL} = 8mA$	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	$V_{in} = 5.5$ V or GND	0 to 5.5			± 0.1		± 1.0	µA
I_{OZ}	Maximum 3–State Leakage Current	$V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	5.5			± 0.25		± 2.5	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			4.0		40.0	µA
I_{CCT}	Quiescent Supply Current	Per Input: $V_{IN} = 3.4V$ Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5V$	0			0.5		5.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	Typ	Max	$T_A = -40$ to $85°C$ Min	Max	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 5.0 ± 0.5V$	$C_L = 15pF$ $C_L = 50pF$	90 85	140 130		80 95		MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q	$V_{CC} = 5.0 ± 0.5V$	$C_L = 15pF$ $C_L = 50pF$		4.1 5.6	9.4 10.4	1.0 1.0	10.5 11.5	ns
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{OE}$ to Q	$V_{CC} = 5.0 ± 0.5V$ $R_L = 1kΩ$	$C_L = 15pF$ $C_L = 50pF$		6.5 7.3	10.2 11.2	1.0 1.0	11.5 12.5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to Q	$V_{CC} = 5.0 ± 0.5V$ $R_L = 1kΩ$	$C_L = 50pF$		7.0	11.2	1.0	12.0	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 5.0 ± 0.5V$ (Note 1)	$C_L = 50pF$			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance, Output in High–Impedance State				9				pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 2)	25	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$ (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 5.0$V)

Symbol	Parameter	$T_A = 25°C$ Typ	Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

MC74VHCT574A

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C Typ	T_A = 25°C Limit	T_A = − 40 to 85°C Limit	Unit
t_{su}	Minimum Setup Time, D to CP	V_{CC} = 5.0 ± 0.5 V		6.5	8.5	ns
t_h	Minimum Hold Time, CP to D	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns
t_w	Minimum Pulse Width, CP	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns

ORDERING INFORMATION

Device	Package	Shipping†
MC74VHCT574ADWG	SOIC−20WB (Pb−Free)	38 Units / Rail
MC74VHCT574ADWRG	SOIC−20WB (Pb−Free)	1000 / Tape & Reel
MC74VHCT574ADTG	TSSOP−20*	75 Units / Rail
MC74VHCT574ADTRG	TSSOP−20*	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.
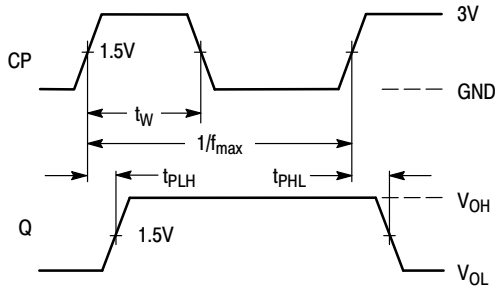
Figure 3. Switching Waveform
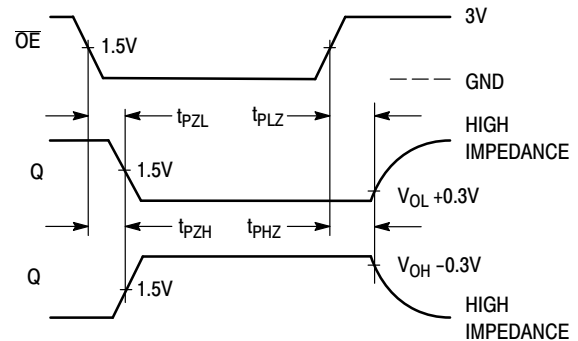
Figure 4. Switching Waveform
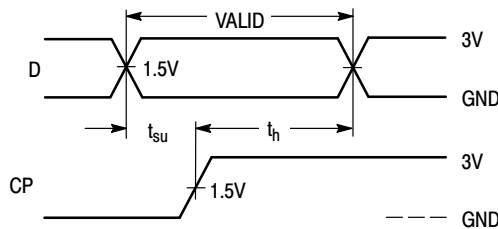
Figure 5. Switching Waveform

MC74VHCT574A
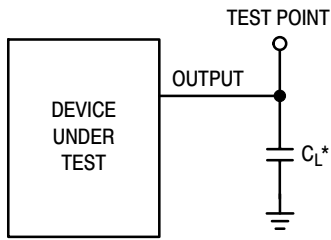
*Includes all probe and jig capacitance

Figure 6. Test Circuit

CONNECT TO V_{CC} WHEN
TESTING t_{PLZ} AND t_{PZL}.
CONNECT TO GND WHEN
TESTING t_{PHZ} AND t_{PZH}.
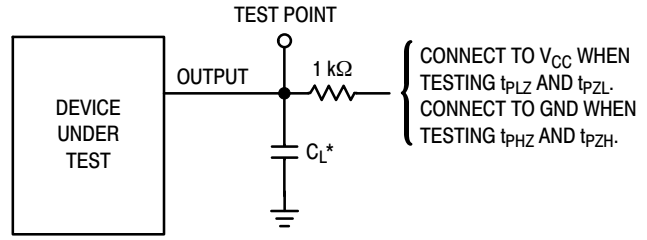
*Includes all probe and jig capacitance

Figure 7. Test Circuit
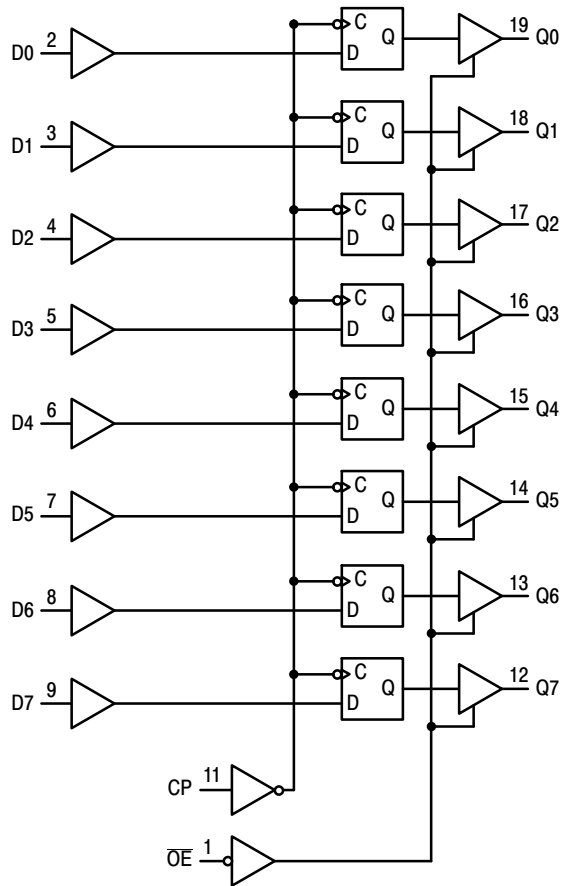
Figure 8. Expanded Logic Diagram

onsemi

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015

SCALE 1:1

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

20X b

⊕ | 0.25 Ⓜ | T | A Ⓢ | B Ⓢ

0.25 Ⓜ | B Ⓜ

SEATING PLANE

18X e

RECOMMENDED SOLDERING FOOTPRINT*

20X 0.52

20X 1.30

11.00

1.27 PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXXXXXXX
XXXXXXXXXX
AWLYYWWG

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42343B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−20 WB		PAGE 1 OF 1

TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1

| 0.15 (0.006) | T | U | Ⓢ |

20X **K** REF

| 0.10 (0.004) | Ⓜ | T | U | Ⓢ | V | Ⓢ |

2X **L/2**

L

PIN 1 IDENT

20   11

B

−U−

10

A

−V−

SECTION N−N

K
K1

J **J1**

0.25 (0.010)

N

M

N

F

DETAIL E

| 0.15 (0.006) | T | U | Ⓢ |

C

D **G** **H**

| 0.100 (0.004) |

−T− **SEATING PLANE**

−W−

DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT

7.06

1

0.65 PITCH

16X 0.36

16X 1.26

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

XXXX
XXXX
ALYW■

A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
■   = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ■", may or may not be present.

DOCUMENT NUMBER:	98ASH70169A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**TSSOP−20 WB**		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

◊