CHANGE NOTIFICATION

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900

October 30, 2015

Dear Sir/Madam: PCN# 103015

Subject: Notification of Change to LTC3114-1

Please be advised that Linear Technology Corporation has made a minor change to the LTC3114-1 die for improved application performance. The die change reduces the product's noise susceptibility during certain adverse operating conditions and has no effect on normal device operation or electrical specifications. Additional applications circuit guidance is added to the product data sheet in concert with the die change and is detailed in the attached pages of the marked up data sheet.

An unrelated electrical specification limit change to the VIN Operating Voltage range specification was made to the LTC3114-1 data sheet to improve manufacturing capability. This change is also shown on the attached pages of the marked up datasheet.

No other functional or parametric specifications are affected. The change was qualified by performing characterization over the full operating temperature range and rigorous engineering evaluation across a broad range of application conditions. In addition, the revised die has passed 168 hours High Temperature Operating Life stress and will successfully complete 1000 hours before being released for sale. Product shipped after December 30, 2015 will be of the new die tested to the new limits.

Should you have any further questions or concerns please contact your local Linear Technology Sales person or you may contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@LINEAR.COM. If I do not hear from you by December 30, 2015, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

Edits # 1A

Insert new line in Vin Operating voltage and edits as shown

VLDO ≥ 2.7V, -55°C to 0°C	*	2.3	40	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 24V, V_{OUT} = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage	V_{LDO} ≥ 2.7V , 0°C to 150°C	●	2.2		40	V
Output Operating Voltage	(Note 5)	●	2.7		40	V
Undervoltage Lockout Threshold on LDO	V_{LDO} Rising	●	2.3	2.5	2.7	V
V_{IN} Quiescent Current in Shutdown				3		µA
V_{IN} Quiescent Current in Burst Mode Operation	FB = 1.4V, Non-Bootstrapped (Note 6)			50		µA
Oscillator Frequency		●	1000	1200	1400	kHz
Oscillator Frequency Variation	V_{IN} = 12V to 36V			0.1		%/V
Feedback Voltage	Measured on FB	●	0.98	1.0	1.02	V
Feedback Voltage Line Regulation	V_{IN} = 2.7V to 40V, Measured on FB			0.2		%
Error Amplifier Transconductance	VC Current = ±5µA			120		µS
FB Pin Input Current	FB = 1V			1	50	nA
VC Source Current	VC = 0.6V			–12		µA
VC Sink Current	VC = 0.6V			12		µA
RUN Pin Threshold—Accurate	RUN Pin Rising	●	1.185	1.205	1.29	V
RUN Pin Hysteresis				140		mV
Run Pin Threshold—Logic		●	0.3	0.7	1.1	V
PROG Current	Switch D Current = 1A Switch D Current = 500mA Switch D Current = 100mA (Note 3)		38 18 2	40 20 4	42 22 6	µA µA µA
PROG Current Gain	Ratio of PROG Current to SWD Current			40		µA/A
PROG Voltage Threshold			0.90	0.925	0.95	V
Inductor Current Limit	(Note 3)	●	1.3	1.7	2.3	A
Overload Current Limit	V_{OUT} = 0V (Note 3)			2.6		A
I_{ZERO} Inductor Current Limit	(Note 3)			100		mA
Maximum Duty Cycle	Percentage of Period SW2 is Low in Boost Mode Percentage of Period SW1 is High in Boost Mode	● ●	90 85	95 88		% %
Minimum Duty Cycle	Percentage of Period SW1 is High in Buck Mode	●			0	%
N-Channel Switch Resistance	Switch A (from PV_{IN} to SW1) Switch B (from SW1 to PGND) Switch C (from SW2 to PGND) Switch D (from PV_{OUT} to SW2)			250 250 250 250		mΩ mΩ mΩ mΩ
N-Channel Switch Leakage				0.1	10	µA
LDO Output Voltage	I_{LDO} = 10mA	●	4.2	4.4	4.6	V
LDO Load Regulation	I_{LDO} = 1mA to 10mA			0.8		%
LDO Line Regulation	I_{LDO} = 1mA, V_{IN} = 10V to 40V			0.2		%
LDO Current Limit	V_{LDO} = 2.5V		40	65		mA
Soft-Start Time				2		ms
SW1 and SW2 Forced Low Time				100		ns
MODE Pin Logic Threshold	H = PWM Mode, L = Burst Mode Operation	●	0.5	0.9	1.3	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3114-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3114E-1 is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3114I-1 specifications are guaranteed over the –40°C to 125°C

EDIT # 1B.

VOUT is determined by the following relationship:

VOUT (V) = 1+ RTOP/RBOT

Where RTOP is connected from PVOUT to FB and RBOT is connected from FB to GND.

PIN FUNCTIONS

PGND (Pin 1, Exposed Pad Pin 17): Power Ground Connections. The PGND pin must be electrically connected to a power ground plane in the application. The exposed pad is an additional power ground connection in parallel with Pin 1. Optimal thermal performance requires that the exposed pad be soldered to the PC board and preferably to a ground plane.

SW2 (Pin 2): Buck-Boost Converter Power Switch Pin. This pin is connected to one side of the buck-boost inductor.

PV_{OUT} (Pin 3): Buck-Boost Converter Power Output. This pin should be connected to a low ESR capacitor of at least 10µF. The capacitor should be placed as close to the IC as possible and should have a short return path to PGND.

RUN (Pin 4): Input to Enable and Disable the IC and Set Custom Input Undervoltage Lockout (UVLO) Thresholds. The RUN pin can be driven by an external logic signal to enable and disable the IC. In addition, the voltage on this pin can be set by a resistive voltage divider connected to the input voltage in order to provide accurate turn-on and turn-off (UVLO) thresholds. The IC is enabled if RUN exceeds 1.2V nominally. Once enabled, the UVLO threshold has built-in hysteresis of approximately 100mV, so turn-off will occur when the voltage on RUN drops to below 1.1V nominally. To continuously enable the IC, RUN can be tied directly to the input voltage up to the absolute maximum rating.

PROG (Pin 5): Output Current Programming Pin and Output of the Switch D Current Sense Amplifier. A current proportional to the current in switch D, the buck-boost converter output current, is delivered from PROG. The PROG current magnitude is approximately $I_{SWD}/25000$. Connect a parallel resistor and capacitor from PROG to GND to generate a voltage proportional to output current. In applications where this voltage is used to control average output current, the resistor value should be set such that the desired average output current produces 1V on PROG and is given by:

$$R_{PROG}(\Omega) = \frac{1V \cdot 25000}{I_{OUT}(A)}$$

Alternatively, the voltage on PROG can be connected to an A/D converter and used for system diagnostic functions. Refer to the Applications Information section for complete details on how to select the proper values for R_{PROG} and C_{PROG}.

VC (Pin 6): Error Amplifier Output. A frequency compensation network must be connected between VC and GND to stabilize the buck-boost converter. Refer to the Applications Information section for details.

FB (Pin 7): Feedback Voltage Input. A resistor divider connected to this pin sets the output voltage for the buck-boost converter. The nominal FB voltage is 1V. Care should be taken in the routing of the connection to this pin to minimize the possibility of stray coupling from the SW pins.

GND (Pin 8): Signal Ground. This pin is the ground connection for the control circuitry of the IC and must be tied to ground in the application.

LDO (Pin 9): Low Voltage Supply Input for the IC Control Circuitry. This pin powers internal IC control circuitry and must be connected to the LDO pin in the application. A 4.7µF or larger bypass capacitor must be connected between this pin and ground. **Pins LDO and PLDO must be connected together in the application.**

V_{IN} (Pin 10): LDO Supply Connection. This pin provides power to the internal V_{CC} regulator. **Pins V_{IN} and PV_{IN} must be connected together in the application.** If the trace connecting V_{IN} and PV_{IN} is of substantial length, a 1µF capacitor should be connected from V_{IN} to GND as close to the IC pins as possible.

PLDO (Pin 11): Internal LDO Regulator Output. PLDO is the output of the internal linear regulator that generates the LDO rail from V_{IN}. PLDO is also used as the supply connection to the power switch gate drivers. **Pins PLDO and LDO must be connected together in the application.**

BST2 (Pin 12): Flying Capacitor Pin for SW2. This pin must be connected to SW2 through a 68nF capacitor. BST2 is used to generate the gate driver rail for power switch D.

BST1 (Pin 13): Flying Capacitor Pin for SW1. This pin must be connected to SW1 through a 68nF capacitor. BST1 is used to generate the gate driver rail for power switch A.

Make the pcb trace from BST1 to the boost capacitor as short and direct as possible.

Edit # 3.

Make the pcb trace from BST2 to the boost capacitor as short and direct as possible.

Edit # 2.

OPERATION

THERMAL CONSIDERATIONS

The power switches of the LTC3114-1 are designed to operate continuously with currents up to the internal current limit thresholds. However, when operating at high current levels, there may be significant heat generated within the IC. In addition, the LDO regulator can generate a significant amount of heat when V_{IN} is very high. This adds to the total power dissipation of the IC. As described elsewhere in this data sheet, bootstrapping of the LDO for 5V output applications can essentially eliminate the LDO power dissipation term and significantly improve efficiency. As a result, careful consideration must be given to the thermal environment of the IC in order to provide a means to remove heat from the IC and ensure that the LTC3114-1 is able to provide its full rated output current. Specifically, the exposed die attach pad of both the DHC and FE packages must be soldered to a copper layer on the PCB to maximize the conduction of heat out of the IC package. This can be accomplished by utilizing multiple vias from the die attach pad connection underneath the IC package to other PCB layer(s) containing a large copper plane. A typical board layout incorporating these concepts is shown in Figure 4.

If the IC die temperature exceeds approximately 165°C, overtemperature shutdown will be invoked and all switching will be inhibited. The part will remain disabled until the die temperature cools by approximately 10°C. The soft-start circuit is re-initialized in overtemperature shutdown to provide a smooth recovery when the IC die temperature cools enough to resume operation.

Start-Up Into a Pre-Biased V_{OUT}

Some applications require the LTC3114-1 to start up into an output voltage (V_{OUT}), that is pre-biased by an external source to some level. It is desirable at LTC3114-1 start-up to minimize current taken from the pre-bias voltage source and V_{OUT} storage capacitor to prevent V_{OUT} glitches and currents fed backwards into the V_{IN} power source of the LTC3114-1.

If the LTC3114-1 V_{IN} voltage is higher than the pre-biased V_{OUT}, indicating buck mode operation, then there will be minimal reverse current at start-up. However, if the LTC3114-1 V_{IN} voltage is lower than the pre-biased V_{OUT}, indicating boost mode operation, then it is possible for a brief, but substantial reverse current to be taken by the LTC3114-1 from V_{OUT}. The duration of this reverse current is approximately 100µs to 200µs. The magnitude is inversely proportional to the V_{IN} voltage and dependent upon external component values.

Prevention of pre-biased V_{OUT} reverse current in boost mode can be achieved in two ways. The preferred method is to ensure that the pre-biased V_{OUT} voltage level is set higher than the nominal V_{OUT} regulation level. For example, if V_{OUT} is pre-biased to 13V, then setting the V_{OUT} regulation voltage of the LTC3114-1 to less than 13V, taking into account error margins, will result in negligible or zero reverse current at start-up. If this is not possible, then a Schottky diode can be connected in series between V_{OUT} of the LTC3114-1 and the converter output to block reverse current .

Edit# 4

New Paragraph title →

High Transient Input Voltage Applications.

Two-layer printed circuit board (PCB) applications that are subject to ≤ 100µs low to high dV/dT transitions on VIN, where the maximum VIN can exceed 20V, require a 1A or higher current Schottky diode connected from SW1 to PGND for robust performance. The Schottky diode is optional, but not required, with four-layer PCB designs similar to the example in figure 4. Refer to the typical applications schematics for examples using this Schottky diode.

The largest recommended PROG pin resistor is 100K. Values of RPROG larger than 100K may latch-off the LTC3114-1 if VOUT is forced to less than 2V by an external load. This is generally not an issue for battery charging applications, but may prevent the charging of very large capacitors. In some general purpose power supply applications, this latch-off behavior may be desirable and in these cases, values of RPROG > 100K are acceptable to use.

Edit # 5

APPLICATIONS INFORMATION

A simplified diagram of the average output current programming circuitry is shown in the Block Diagram. An internal sense resistor, R_S, and low offset amplifier directly measure current in the V_{OUT} path and produce a small fraction of this current out of the PROG pin. Accordingly, a resistor and filtering capacitor connected from PROG to ground produce a voltage proportional to average output current on PROG. An internal transconductance amplifier compares the PROG voltage to the fixed 1V internal reference. If the PROG voltage tries to exceed the 1V reference level, this amplifier will pull down on VC and take command of the PWM. As described earlier, VC is the current command voltage, so limiting VC in this manner will also limit output current. The resulting average output current is given by the following equation:

$$I_{OUT(AVG)} \cong 25{,}000 \bullet \frac{1V}{R_{PROG}}$$

Where: RProg = 24.9K to 100K

The gain of 25,000 is generated internal to the LTC3114-1 and is factory trimmed to provide the best accuracy at 500mA of output current. The accuracy of the programmed output current is best at the high end of the range as the residual internal current sense amplifier offset becomes a smaller percentage of the total current sense signal amplitude with increasing current. The provided electrical specifications define the PROG pin current accuracy over a range of output currents.

Selecting the capacitor, C_{PROG}, to put in parallel with R_{PROG} is a trade-off between response time, output current ripple and interaction with the normal output voltage control loop. In general, if speed is not a concern as is the case for most current sourcing applications, then C_{PROG} should be made at least 3 times higher than the voltage error amplifier compensation capacitor, C_{P1}, described in the Compensation section of this data sheet. This will ensure minimal to no interaction when the transition occurs between voltage regulation mode and output current regulation mode.

In current sourcing applications, the maximum output compliance voltage of the LTC3114-1 is set by the voltage error amplifier dividers resistors as it is for standard voltage regulation applications. For LED drivIng applications, select the V_{OUT} divider resistors for a clamping level 1V to 2V higher than the expected forward voltage drop of the LED string. The average output current circuitry can also be used to monitor, rather than control the output current. To do this, select an R_{PROG} value that will limit the voltage on the PROG pin to 0.8V or less at the highest output current expected in the application.

Connect a 20k resistor and 33nF capacitor from PROG to ground if the function is not going to be used to provide a higher level of protection against inadvertent short-circuit conditions on V_{OUT}.

Compensation of the Buck-Boost Converter

The LTC3114-1 utilizes average current mode control to regulate the output voltage. Average current mode control has two loops that require frequency compensation, the inner average current loop and the outer voltage loop. The compensation for the inner average current loop is fixed within the LTC3114-1 in order to provide the highest possible bandwidth over the wide operating range of the LTC3114-1. Therefore, the only control loop that requires compensation design is the outer voltage loop. As will be shown, compensation design of the outer loop is similar to the techniques used in well known peak current mode control devices.

The LTC3114-1 utilizing average current mode control can be conceptualized in its simplest form as a voltage-controlled current source (V_{CCS}), driving the output load formed primarily by R_{LOAD} and C_{OUT}, as shown in Figure 6.

The error amplifier output (VC), provides the command input to the V_{CCS}. The full-scale range of VC is 0.865V (135mV to 1V). With a full-scale command on VC,

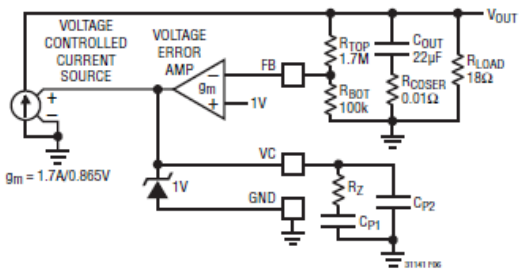
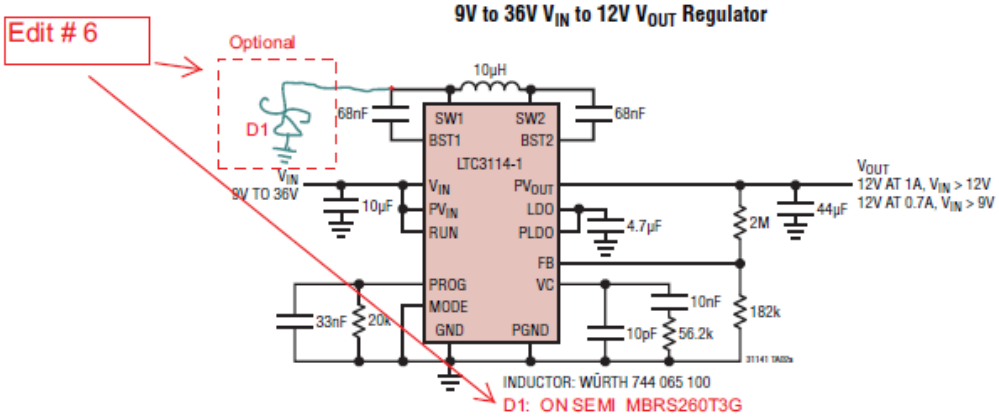


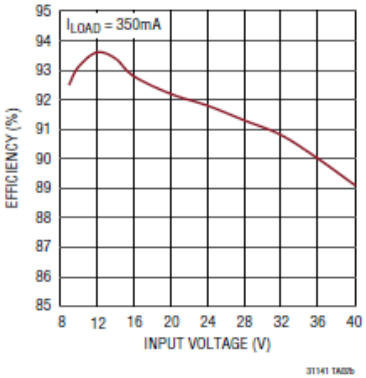
Figure 6. Simplified Representation of Average Current Mode Control Loop

TYPICAL APPLICATIONS

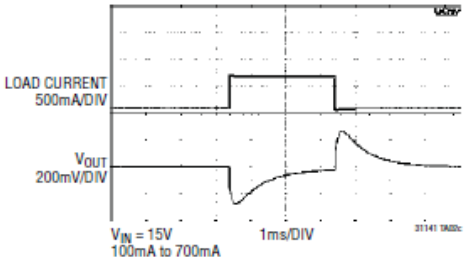
9V to 36V V_{IN} to 12V V_{OUT} Regulator



Efficiency vs Input Voltage



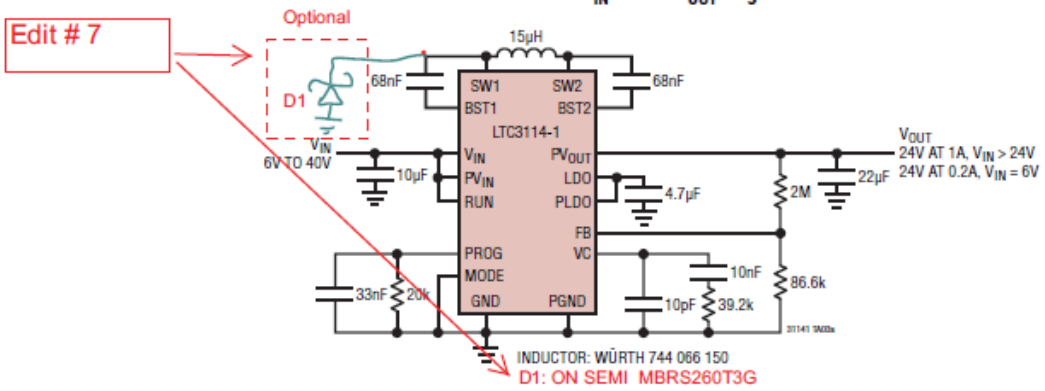
Load Step Response



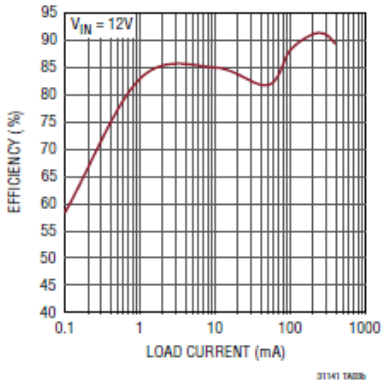
TYPICAL APPLICATIONS

Edit # 7

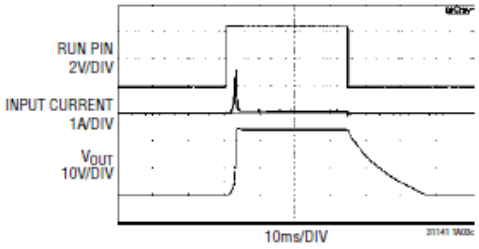
6V to 40V V_{IN} to 24V V_{OUT} Regulator



Efficiency vs Load Current



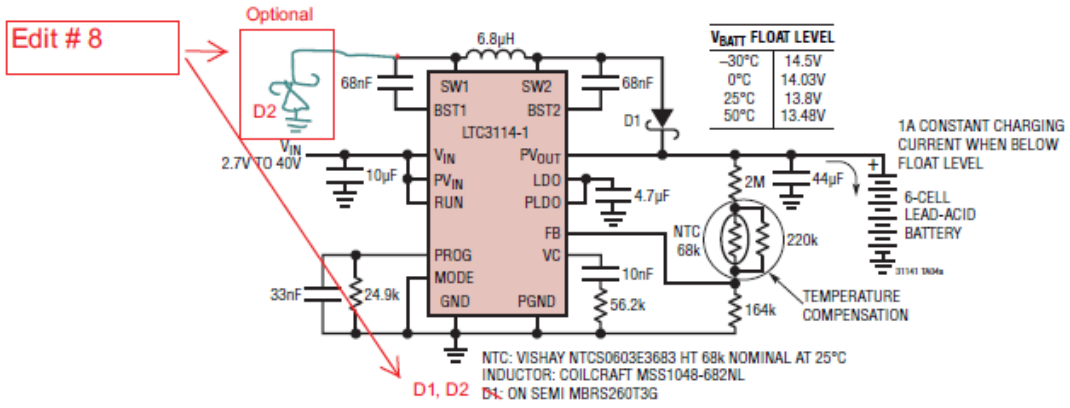
12V V_{IN} Synchronous Boost Operation with Inrush Current Limiting at Start-Up and Output Disconnect in Shutdown



TYPICAL APPLICATIONS

Constant Current/Constant Voltage Lead-Acid Battery Charger

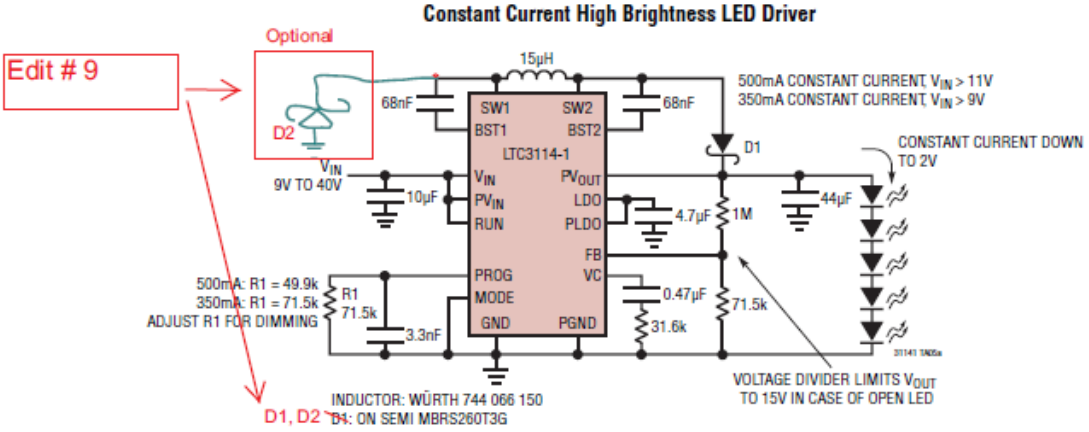
Edit # 8



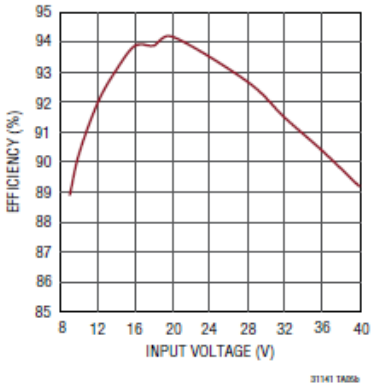
V_{BATT} FLOAT LEVEL	
–30°C	14.5V
0°C	14.03V
25°C	13.8V
50°C	13.48V

TYPICAL APPLICATIONS

Constant Current High Brightness LED Driver



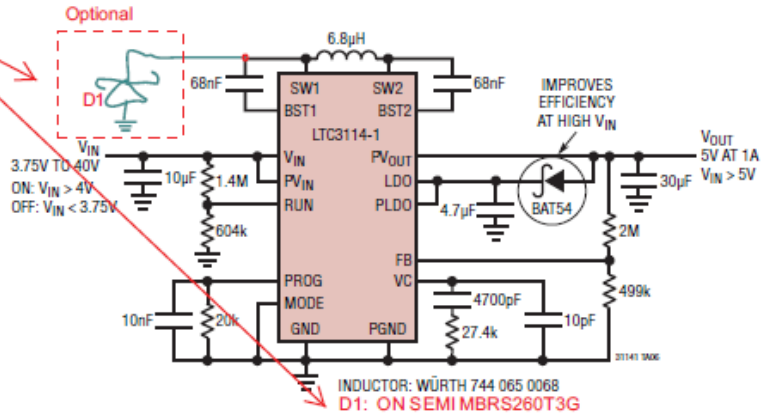
Efficiency vs Input Voltage, 350mA Drive Current



TYPICAL APPLICATION

Wide V_{IN} Range 5V, 1A Regulator with Bootstrapped LDO and Custom UVLO Threshold

Edit # 10



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3534	7V, 500mA (I_{OUT}), 1MHz Synchronous Buck-Boost DC/DC Converter	94% Efficiency, V_{IN}: 2.4V to 7V, V_{OUT}: 1.8V to 7V, I_Q = 25µA, I_{SD} < 1µA, DFN and GN Packages
LTC3112	2.5A (I_{OUT}), Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.7V to 15V, V_{OUT}: 2.5V to 14V, I_Q = 40µA, I_{SD} < 1µA, DFN and TSSOP Packages
LTC3115-1	40V, 2A Synchronous Buck-Boost DC/DC Converter	V_{IN}, V_{OUT}: 2.7V to 40V, I_Q = 30µA, I_{SD} = 3µA, DFN and TSSOP Packages
LTC3785	≤10A (I_{OUT}), High Efficiency, 1MHz Synchronous, No R_{SENSE}™ Buck-Boost DC/DC Controller	V_{IN}: 2.7V to 10V, V_{OUT}: 2.7V to 10V, I_Q = 86µA, I_{SD} < 15µA, QFN Package
LTC3789	Buck-Boost DC/DC Controller	96% Efficiency, V_{IN}: 4.5V to 38V, V_{OUT}: 0.8V to 38V, 4mm × 5mm QFN and SSOP Packages
LTM®4605	4.5V to 20V, 10A Buck-Boost µModule® Regulator	High Power Buck-Boost µModule Regulator
LTC3129	15.75V, 200mA Buck-Boost DC/DC Converter with 1.3µA I_Q	V_{IN}: 2.42V to 15.75V, V_{OUT}: 1.4V to 15V, I_Q = 1.3µA, I_{SD} = 10nA, DFN and MS Packages
LTC3129-1	15.75V, 200mA Buck-Boost DC/DC Converter with 1.3µA I_Q and Programmable Output Voltages	V_{IN}: 2.42V to 15.75V, V_{OUT}: Pin Programmable 2.5V to 15V, I_Q = 1.3µA, I_{SD} = 10nA, DFN and MS Packages

Edit # 11 Add LTC3118

Part	Description	V_{IN} Min (V)	V_{IN} Max (V)	V_{OUT} Min (V)	I_Q(µA)	I_{SD}	Package
LTC3118	18V, 2A Synchronous Buck-Boost DC/DC Converter with Low Loss Dual Input PowerPath	2.2	18	2.0V to 18V	50uA	<1µA	4 x 5 QFN-24 TSSOP-28E