Click here to ask about the production status of specific part numbers.

MAX77597

36V, 300mA, Buck Converter with 1.1µA I_Q

General Description

The MAX77597 is a small, synchronous buck converter with integrated switches. The device is designed to deliver up to 300mA with input voltages from 3.5V to 36V, while using only 1.1µA quiescent current at no load (fixed-output version). Voltage quality can be monitored by observing the $\overline{\text{RESET}}$ signal. The device can operate near dropout by running at 98% duty cycle, making it ideal for battery-powered applications.

The device offers fixed 3.3V. Frequency is fixed at 1.7MHz, which allows for small external components and reduced output ripple. The device offers both forced-PWM and skip modes of operation, with ultra-low quiescent current of 1.1µA in skip mode.

The MAX77597 is available in a small (2mm x 2.5mm) 10-pin TDFN package and operates across the -40°C to +85°C temperature range.

Applications

- Portable Devices Powered from 2s, 3s, or 4s Li+ Batteries
- USB Type-C Devices
- Point-of-Load Applications

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Flexible Power for Systems That Require a Wide Input Voltage Range
  - V_{IN} Range: 3.5V to 36V
  - Up to 300mA Output Current
  - Fixed 3.3V, Output Voltage
  - 98% (Max) Duty Cycle Operation with Low Dropout
  - Operates from 5V, 12V, or 20V USB Type-C Input Power
  - Operates from 2S, 3S, or 4S Li-Ion Battery
- Minimizes Power Consumption and Extends Battery Life
  - 1.1µA Quiescent Current (3.3V Fixed Output Voltage)
  - 86% Peak Efficiency at $12V_{IN}$, 3.3 V_{OUT}
- Minimizes Solution Size
  - 1.7MHz Operating Frequency
  - Small 2.0mm x 2.5mm x 0.75mm 10-Pin TDFN Package
- Robust Solution
  - Short-Circuit, Thermal Protections
  - 6.67ms Internal Soft-Start Minimizes Inrush Current
  - Current-Mode Control Architecture
  - Up to 42V Input Voltage Tolerance

19-100785; Rev 1; 4/20

maxim integrated™

Absolute Maximum Ratings

(Voltages Referenced to PGND)

SUP .....-0.3V to +42V
EN.....-0.3V to MIN (24V, V_{SUP} + 0.3V)
BST to LX .....+6V
BST.....-0.3V to +47V
MODE, OUT/FB, $\overline{RESET}$..... .....-0.3V to V_{BIAS} + 0.3V
AGND.....-0.3V to +0.3V
BIAS..... .....-0.3V to +6.0V

OUT/FB Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
(derate 9.8mW/°C above +70°C) 784mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....300°C
Soldering Temperature (reflow).....+260°C

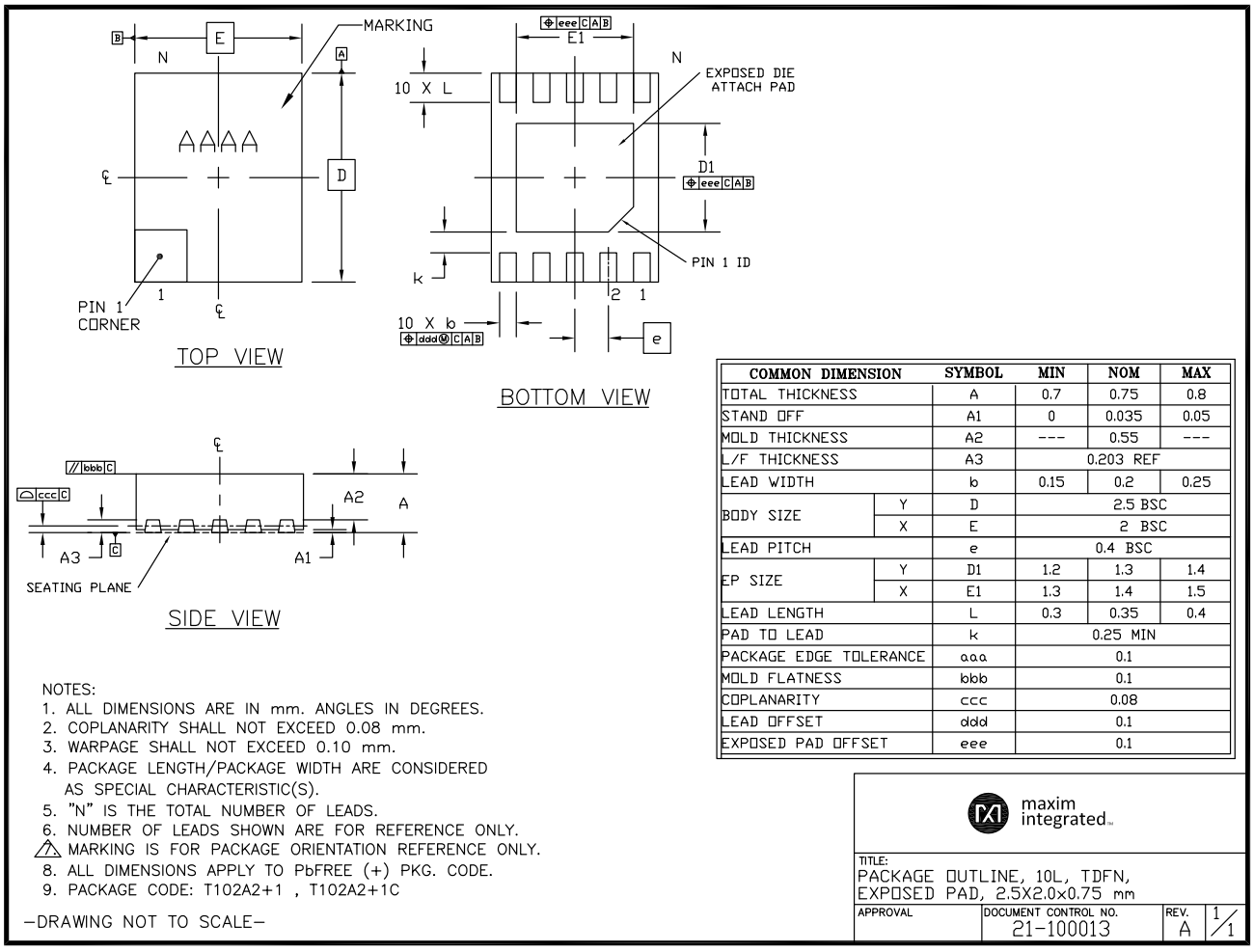
Package Information

20-TDFN

PACKAGE CODE	T102A2+1C
Outline Number	21-100013
Land Pattern Number	—
Thermal Resistance:	
Junction to Ambient (θ_{JA})	102ºC/W
Junction to Case (θ_{JC})	2.9ºC/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.



COMMON DIMENSION		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	Y	D		2.5 BSC	
	X	E		2 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	Y	D1	1.2	1.3	1.4
	X	E1	1.3	1.4	1.5
LEAD LENGTH		L	0.3	0.35	0.4
PAD TO LEAD		k		0.25 MIN	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. "N" IS THE TOTAL NUMBER OF LEADS.
6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. ALL DIMENSIONS APPLY TO PbFREE (+) PKG. CODE.
9. PACKAGE CODE: T102A2+1 , T102A2+1C

—DRAWING NOT TO SCALE—

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TITLE:
PACKAGE OUTLINE, 10L, TDFN,
EXPOSED PAD, 2.5X2.0x0.75 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-100013	A	1/1

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, V_{MODE} = 0V, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{SUP}		3.5		36	V
Supply Voltage	V_{SUP}	t < 500ms (Note 2)			42	V
Supply Current	I_{SUP}	Shutdown (V_{EN} = 0V)		0.75	3.0	µA
		No load, fixed 3.3V V_{OUT}		1.1	3.0	
		V_{MODE} = V_{BIAS} , no load, FPWM, no switching	0.5	1	1.5	mA
UV Lockout	V_{UVLO}	V_{BIAS} rising	3.0	3.2	3.4	V
		Hysteresis		0.4		
BIAS Regulator Voltage	V_{BIAS}	V_{SUP} = 5.5V to 36V		5		V
BIAS Current Limit			10			mA
BUCK CONVERTER						
Voltage Accuracy	$V_{OUT,3.3V}$	V_{OUT} = 3.3V, 6V ≤ V_{SUP} ≤ 36V, I_{LOAD} = 0 to 300mA	3.1	3.3	3.4	V
High-Side DMOS R_{DSON}	$R_{ON,HS}$	V_{BIAS} = 5V, I_{LX} = 200mA		1000	2200	mΩ
Low-Side DMOS R_{DSON}	$R_{ON,LS}$	V_{BIAS} = 5V, I_{LX} = 200mA		500	1200	mΩ
DMOS High-Side Current-Limit Threshold	I_{MAX}		425	500	575	mA
DMOS High-Side Skip-Mode Peak-Current Threshold	I_{SKIP}		70	100	130	mA
DMOS Low-Side Zero-Crossing Threshold	I_{ZX}			40		mA
DMOS Low-Side Negative Current-Limit Threshold	I_{NEG}	FPWM mode		-320		mA
Soft-Start Ramp Time	t_{SS}			6.67		ms
LX Rise Time	$t_{RISE,LX}$	(Note 2)		6		ns
Minimum On-Time	t_{ON_MIN}			34		ns
Maximum Duty Cycle	DC_{MAX}			98		%
PWM Switching Frequency	f_{SW}		1.58	1.7	1.82	MHz
RESET OUTPUT ($\overline{RESET}$)						
$\overline{RESET}$ Threshold	V_{THR_RES}	V_{OUT} rising	88	92	96	%V_{OUT}
	V_{THF_RES}	V_{OUT} falling	86	90	94	
$\overline{RESET}$ Debounce	t_{DEB}			12		µs
$\overline{RESET}$ High Leakage Current	$I_{LEAK,RES}$	T_A = +25°C			1	µA
$\overline{RESET}$ Low Level	$V_{OUT,RES}$	Sinking 1mA			0.4	V

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, V_{MODE} = 0V, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVELS						
EN Input High Threshold	$V_{IH,EN}$		2.4			V
EN Input Low Threshold	$V_{IL,EN}$				0.4	V
EN Input Current	$I_{IN,EN}$			0.1		µA
MODE Input High Threshold	$V_{IH,MODE}$		1.4			V
MODE Input Low Threshold	$V_{IL,MODE}$				0.4	V
MODE Internal Pulldown	$R_{PD,MODE}$			1000		kΩ
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}	(Note 2)		+175		°C
Thermal-Shutdown Hysteresis	$T_{SHDN,HYS}$	(Note 2)		+15		°C

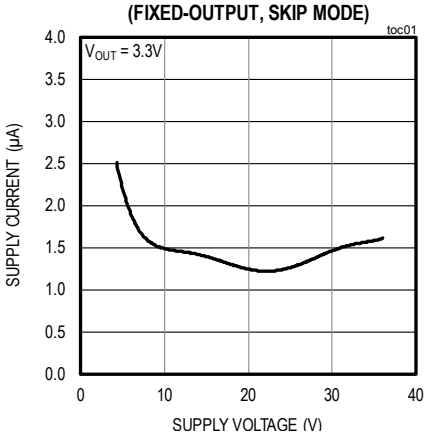
Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Guaranteed by design; not production tested.

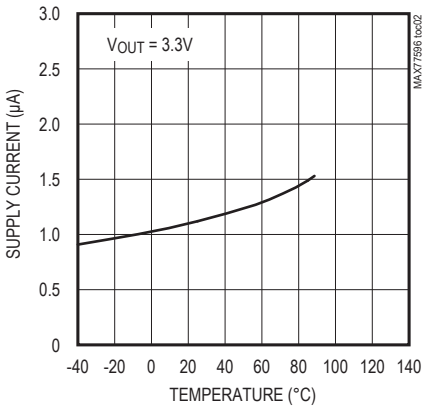
Typical Operating Characteristics

(V_{SUP} = V_{EN} = 12V, T_A = +25°C, unless otherwise noted.)

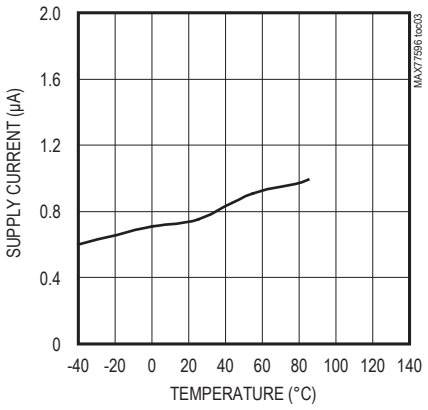
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE (FIXED-OUTPUT, SKIP MODE)



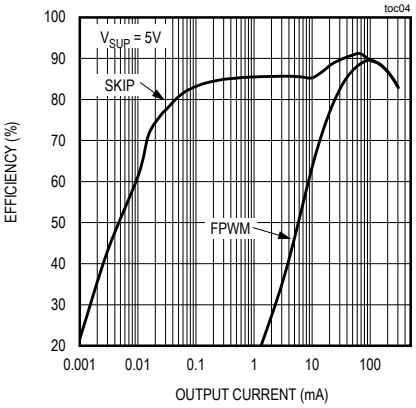
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE (SKIP MODE)



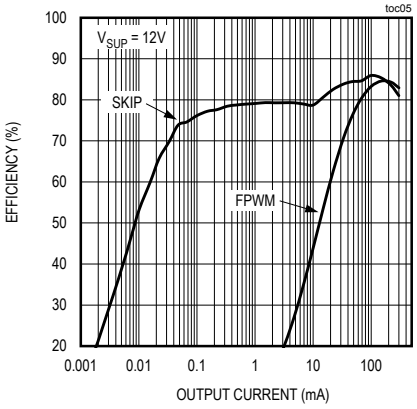
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



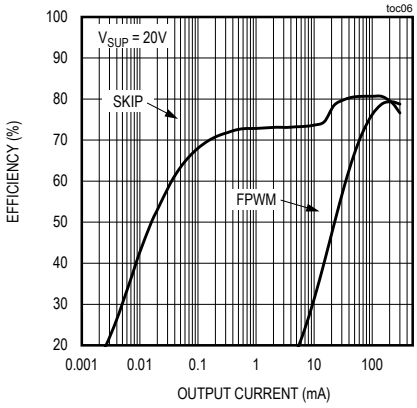
EFFICIENCY vs. LOAD 3.3V FIXED-OUTPUT



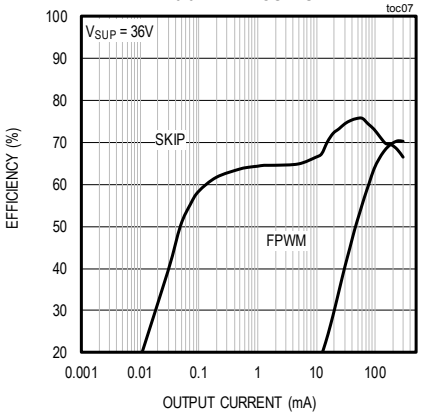
EFFICIENCY vs. LOAD 3.3V FIXED-OUTPUT



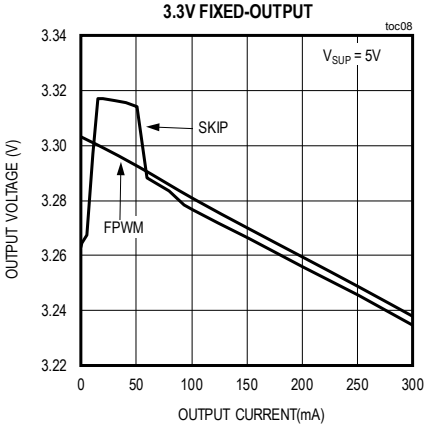
EFFICIENCY vs. LOAD 3.3V FIXED-OUTPUT



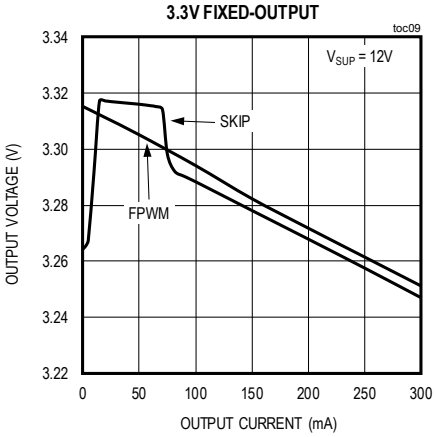
EFFICIENCY vs. LOAD 3.3V FIXED-OUTPUT



LOAD REGULATION 3.3V FIXED-OUTPUT



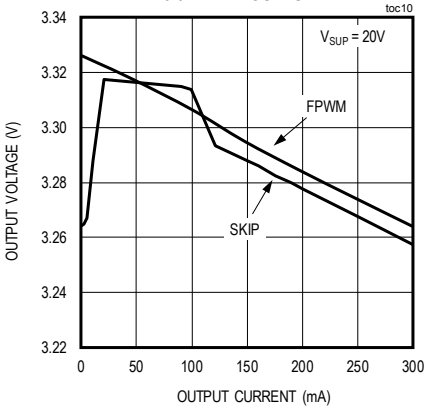
LOAD REGULATION 3.3V FIXED-OUTPUT



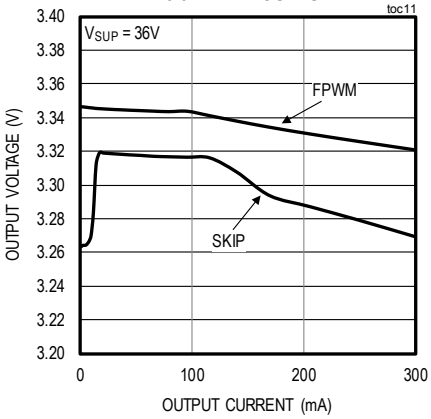
Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = 12V, T_A = +25°C, unless otherwise noted.)

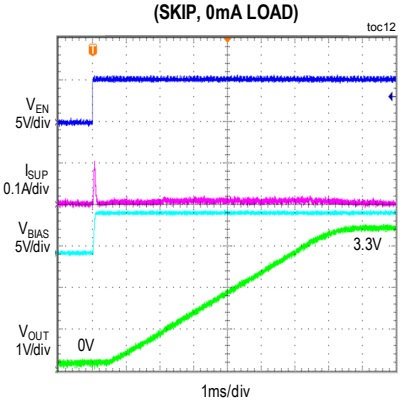
LOAD REGULATION
3.3V FIXED-OUTPUT



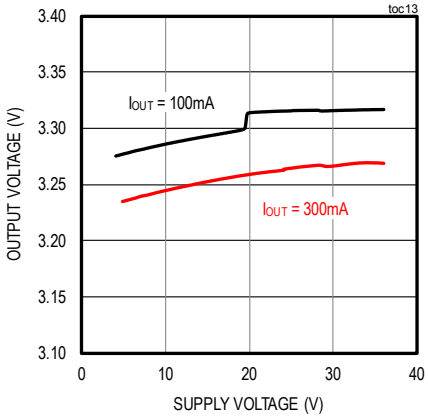
LOAD REGULATION
3.3V FIXED-OUTPUT



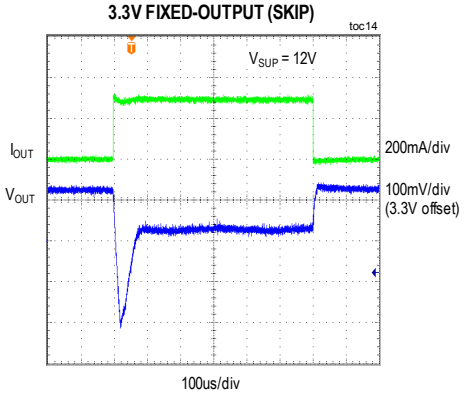
STARTUP WAVEFORM
3.3V ADJUSTABLE-OUTPUT
(SKIP, 0mA LOAD)



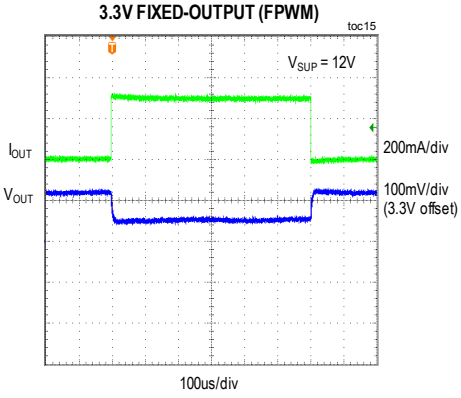
LINE REGULATION
3.3V FIXED-OUTPUT



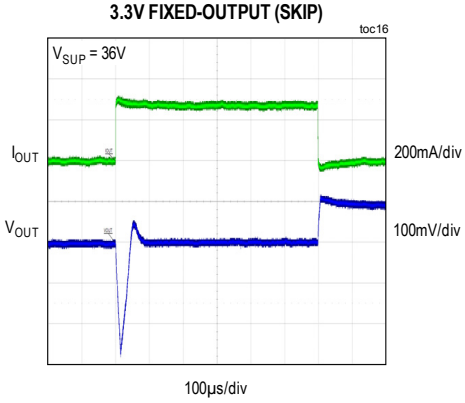
LOAD TRANSIENT RESPONSE
3.3V FIXED-OUTPUT (SKIP)



LOAD TRANSIENT RESPONSE
3.3V FIXED-OUTPUT (FPWM)



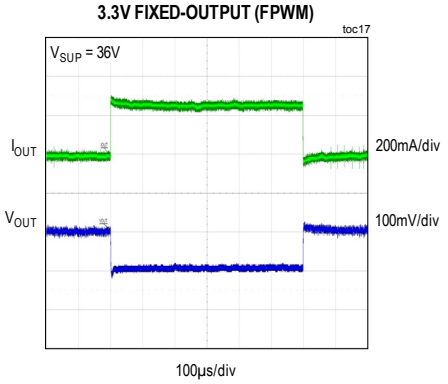
LOAD TRANSIENT RESPONSE
3.3V FIXED-OUTPUT (SKIP)



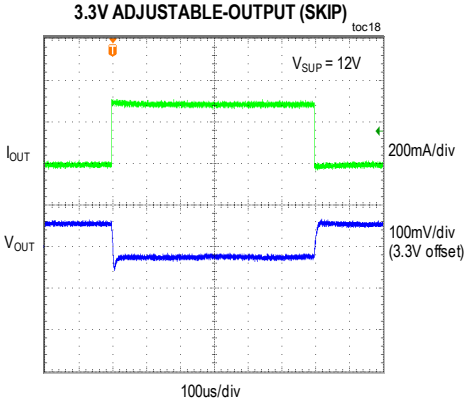
Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = 12V, T_A = +25°C, unless otherwise noted.)

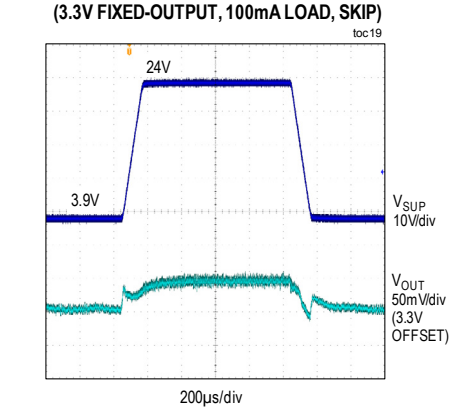
LOAD TRANSIENT RESPONSE 3.3V FIXED-OUTPUT (FPWM)



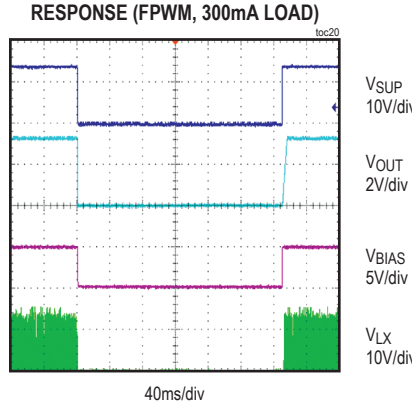
LOAD TRANSIENT RESPONSE 3.3V ADJUSTABLE-OUTPUT (SKIP)



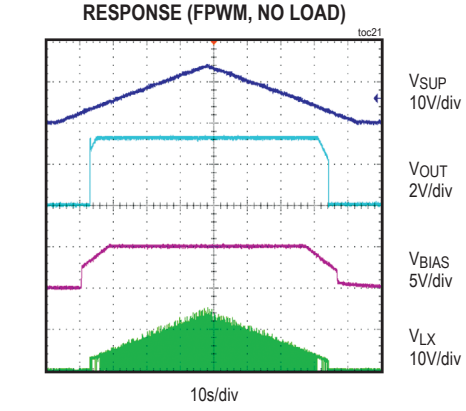
LINE TRANSIENT RESPONSE (3.3V FIXED-OUTPUT, 100mA LOAD, SKIP)



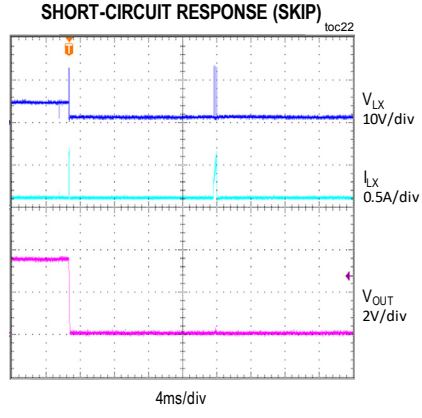
3.3V FIXED-OUTPUT V_{SUP} ON/OFF RESPONSE (FPWM, 300mA LOAD)



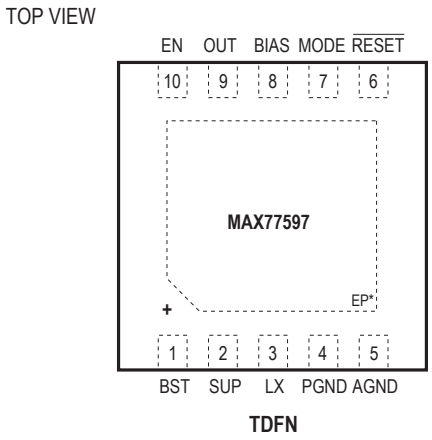
3.3V FIXED-OUTPUT SLOW V_{SUP} RESPONSE (FPWM, NO LOAD)



SHORT-CIRCUIT RESPONSE (SKIP)



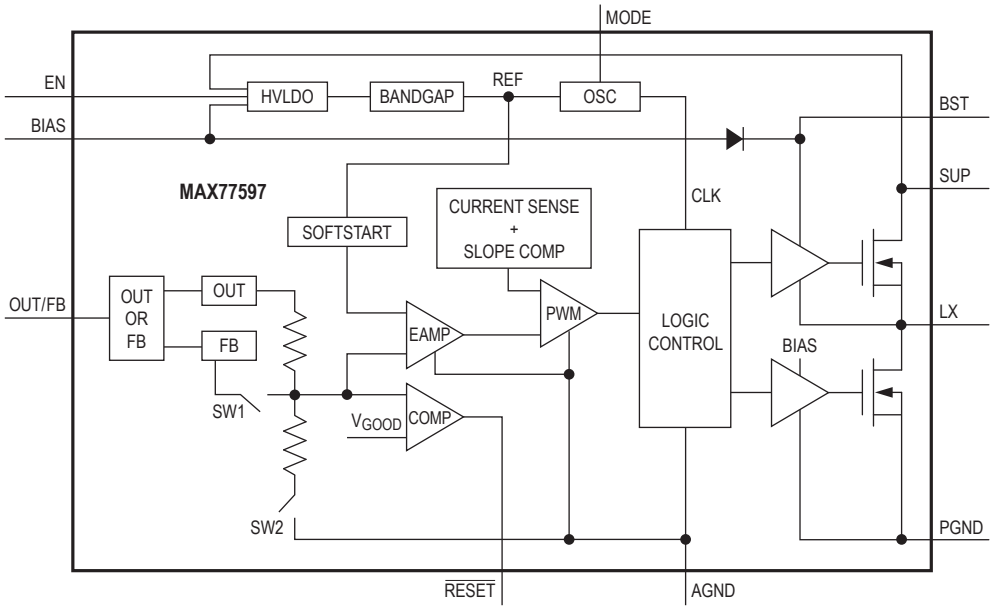
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	BST	High-Side Driver Supply. Connect a 0.1µF bootstrap capacitor between LX and BST.
2	SUP	IC Supply Input. Connect a minimum of 4.7µF ceramic capacitor from SUP to PGND.
3	LX	Buck Switching Node. LX is high impedance when the device is off.
4	PGND	Power Ground. Connect to AGND under the device in a star configuration.
5	AGND	Analog Ground. Connect to PGND under the device in a star configuration.
6	$\overline{\text{RESET}}$	Open-Drain Reset Output. An external pullup resistor is required.
7	MODE	Mode Switch-Control Input. Connect to ground or leave open to enable skip-mode operation under light loads. Connect to BIAS to enable forced-PWM mode. MODE has a 1MΩ internal pulldown.
8	BIAS	5V Internal Logic Supply. Connect a 1µF ceramic capacitor to AGND. Do not load this pin externally.
9	OUT	MAX77597ETBB+ (Fixed Output): Buck Regulator Voltage-Sense Input. Bypass OUT to PGND with a minimum 22µF X5R ceramic capacitor.
10	EN	Enable Input. Drive EN low to disable the device. Drive EN high to enable the device.
—	EP	Exposed Pad. Connect EP to a large copper ground plane for effective power dissipation. Do not use EP as the only IC ground connection. EP must be connected to PGND.

Block Diagram



NOTE: FOR INTERNAL FEEDBACK VERSION, SW1 IS OPEN AND SW2 CLOSED. EXTERNAL PIN IS CALLED OUT.

Detailed Description

The MAX77597 is a small, current-mode buck converter that features synchronous rectification and requires no external compensation network. The device operates from a 3.5V to 36V supply voltage and can deliver up to 300mA output current. Frequency is fixed at 1.7MHz, which allows for small external components and reduced output ripple.

The device offers fixed 3.3V output Voltage quality can be monitored by observing the $\overline{\text{RESET}}$ signal. The device offers both forced-PWM and skip mode, with ultra-low-quiescent current of 1.1µA in skip mode.

DC-DC Converter Control Architecture

The step-down converter uses a PWM peak current-mode control scheme with a load-line architecture. Peak current-mode control provides several advantages over voltage-mode control, including precise control of the inductor current on a cycle-by-cycle basis, simpler compensation, and inherent compensation for line voltage variation.

An internal transconductance amplifier establishes an integrated error voltage. The heart of the PWM controller is an open-loop comparator: one input is the integrated voltage-feedback signal; the other consists of the amplified current-sense signal plus slope-compensation ramp. Integrated high-side current sensing is used, which reduces component count and layout risk by eliminating the need to carefully route sensitive external signals. Error-amplifier compensation is also integrated, once again simplifying the power-supply designer's task while eliminating external components.

The controller features a load-line architecture. The output voltage is positioned slightly above nominal regulation at no load and slightly below nominal regulation at full load. As output load changes, a small but controlled amount of load regulation ("load-line") error occurs on the output voltage. This voltage positioning architecture allows the output voltage to respond to sudden load transients in a critically damped manner, and effectively reduces the amount of output capacitance needed when compared to classical integrating controllers. See the *Typical Operating Characteristics* section of the data sheet for information about the converter's typical voltage regulation behavior versus load.

The device can operate in either forced-PWM or skip mode. In forced-PWM mode, the converter maintains a constant switching frequency, regardless of load, to allow for easier filtering of the switching noise. The device includes proprietary circuitry that dramatically reduces quiescent current consumption in skip mode, improving light-load efficiency. See the *Forced PWM/Skip Modes* section for further details.

System Enable (EN)

An enable control input (EN) activates the device from its low-power shutdown mode. EN is compatible with inputs from levels down to 2.4V. EN can be connected directly to SUP for voltage level up to 24V. For self-enable operations with SUP voltages above 24V, connect EN using an external resistor divider to maintain EN below 24V.

Linear Regulator Output (BIAS)

The device includes a 5V linear regulator output (BIAS) that provides power to the internal circuit blocks. Connect a 1µF ceramic capacitor from BIAS to AGND. Do not load this pin externally.

Undervoltage Lockout

When V_{BIAS} drops below the undervoltage-lockout (UVLO) level of V_{UVLO} = 2.8V (typ), the device assumes that the supply voltage is too low for proper operation, so the UVLO circuitry inhibits switching. When V_{BIAS} rises above the UVLO rising threshold, the controller enters the startup sequence and then resumes normal operation.

Startup and Soft-Start

The device features an internal soft-start timer. The output-voltage soft-start ramp time is 6.67ms (typ). If a short circuit or undervoltage is encountered after the soft-start timer has expired, the device is disabled for 16.5ms (typ) and then reattempts soft-start again. This pattern repeats until the short circuit has been removed.

$\overline{\text{RESET}}$ Output

The device features an open-drain $\overline{\text{RESET}}$ output to monitor the output voltage. The $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) after the regulator output increases above 92% of the nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output drops to below 90% of the nominal regulated voltage.

Forced PWM/Skip Modes

The device features a logic-level input (MODE) to switch between forced-PWM and skip modes. Connecting MODE to BIAS enables the forced-PWM operation. Connecting MODE to ground, or leaving unconnected, enables skip-mode operation with ultra-low-quiescent current of 1.1µA. In skip-mode operation, the converter's switching frequency is load dependent until the output load reaches the skip threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the forced-PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch the MOSFETs on and off as often as is the case in the forced-PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Current Limit/Short-Circuit Protection

The device has fault protection designed to protect itself from abnormal conditions. If the output is soft shorted (meaning the output is overloaded but over 25% of regulation), cycle-by-cycle current limit limits how high the inductor current goes for any cycle. If the output is hard shorted to ground and the output falls to less than 25% of regulation, the part goes into a mode where it switches until 15 cycles are ended by current limit, then waits for 16.5ms before trying to soft-start again. This mode of operation limits the amount of power dissipated by the device under these conditions. The device also has overtemperature protection. If the die temperature exceeds approximately 175°C, the device stops switching until the die temperature drops by approximately 15°C and then resumes operation, including going through soft-start again.

Applications Information

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determines the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{SUP} - V_{OUT})}{V_{SUP} \times f_{SW} \times I_{OUT} \times LIR}$$

where V_{SUP}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is 1.7MHz. Table 1 lists some of the inductor values for 300mA output current and several output voltages.

Table 1. Inductor Values for 300mA Output Current

V_{SUP}/V_{OUT} (V)	14V/3.3V
INDUCTOR (µH) I_{LOAD} = 300mA	10µH (typ) 22µH (max)

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{SUP} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{OUT}}{V_{SUP}}$$

where I_{OUT} is the maximum output current and D is the duty cycle.

Output Capacitor

The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output voltage ripple. Therefore, the size of the output capacitor depends on the maximum ESR required to meet the output voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Therefore, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent voltage droop and voltage rise from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising-load edge is no longer a problem.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low-switching power losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) The input capacitor (4.7µF, see Figures 3 and 4) should be placed immediately next to the SUP pin of the device. Since the device operates at 1.7MHz switching frequency, this placement is critical for effective decoupling of high-frequency noise from the SUP pin.
2) Solder the exposed pad to a large copper plane area under the device. To effectively use this copper area as heat exchanger between the PCB and ambient, expose the copper area on the top and bottom sides. Add a few small vias or one large via on the copper pad for efficient heat transfer. Connect the exposed pad to PGND, ideally at the return terminal of the output capacitor.
3) Isolate the power components and high-current path from the sensitive analog circuitry. Doing so is essential to prevent any noise coupling into the analog signals.
4) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
5) Connect PGND and AGND together at the return terminal of the output capacitor. Do not connect them anywhere else.
6) Keep the power traces and load connections short. This practice is essential for high efficiency.
7) Place the BIAS capacitor ground next to the AGND pin and connect with a short and wide trace.

Typical Application Circuits

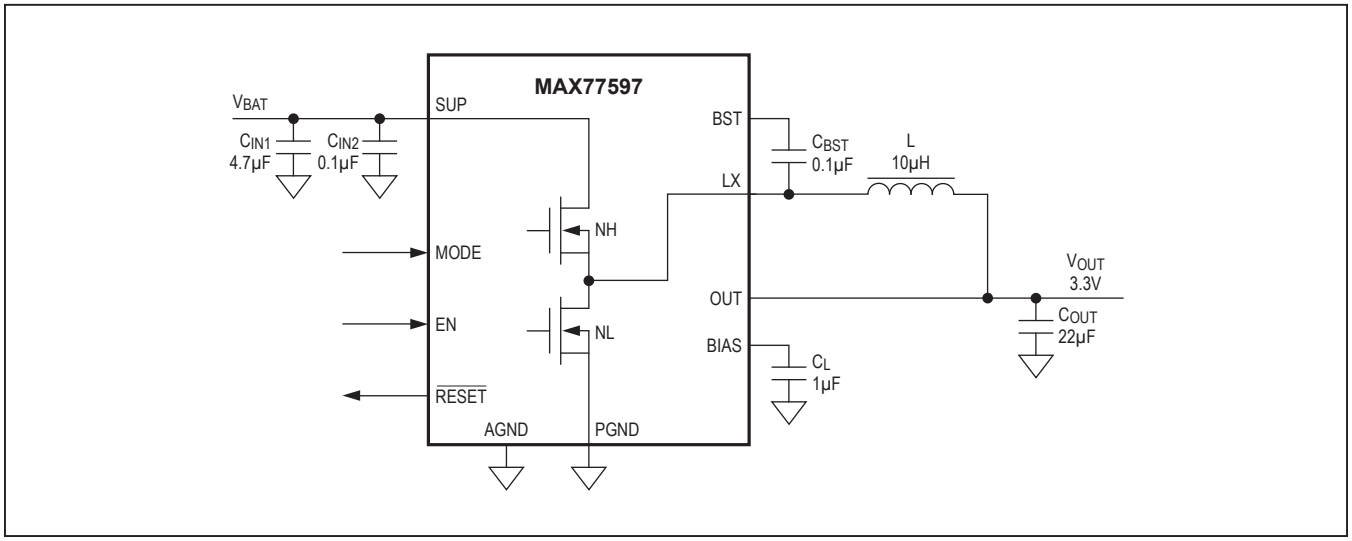


Figure 1. MAX77597ETBB+, Fixed Output Voltage (3.3V), 10-Pin TDFN

Ordering Information

PART	V_{OUT}	PIN-PACKAGE
MAX77597ETBB+	Fixed 3.3V	10 TDFN-EP*

**EP = Exposed pad.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/20	Initial release	—
1	4/20	Updated the *Detailed Description* section	11

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