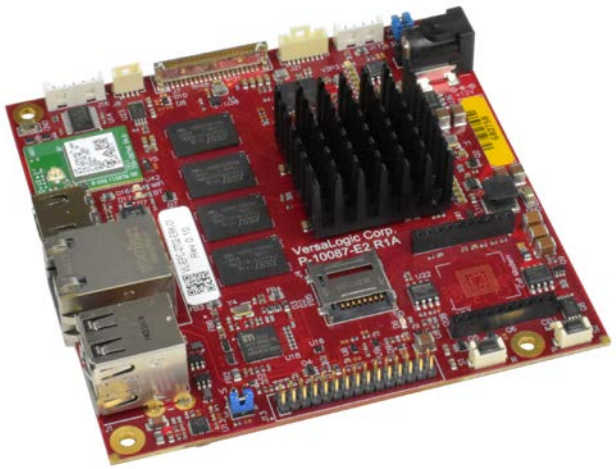


Hardware Reference Manual

REV. January 2021

Swordtail (VL-EPC-2702)

Arm* i.MX6 Single Board Computer with Gigabit Ethernet, Video, USB, Bluetooth, Wi-Fi, Cellular, Digital I/O, CAN Bus and I^2C

VERSALOGIC CORPORATION

WWW.VERSALOGIC.COM

12100 SW Tualatin Road
Tualatin, OR 97062-7341
(503) 747-2261
Fax (971) 224-4708

Notice:

Although every effort has been made to ensure this document is error-free, VersaLogic makes no representations or warranties with respect to this product and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose.

VersaLogic reserves the right to revise this product and associated documentation at any time without obligation to notify anyone of such changes.

* Other names and brands may be claimed as the property of others.

Product Release Notes

Rev 1.00 Initial draft

Rev 1.01 Updated cable information for J13 in table 2

Rev 1.02 Updated pin 27 and 28 information in table 15

Rev 1.5 Updated Table 2 with the following:

- Removed the dash from Transition Cable column for the following Connectors: J1 (added "USB", J6 (added "HDMI")
- Changed the Transition Cable dash to "N/A" for J4 and J20 For J6, added to Mating Connector "Standard HDMI Plug" and added "Standard HDMI Cable" to the Cable Description column
- For J13, changed the Mating Connector gender to "Female," moved the cable part number over to the Transition Cable column, and added "Serial Interface Ribbon Cable" and "User Input/Output Interface Ribbon Cable" to the Cable Description column respectively
- For J15, changed the Mating Connector info from "Jack" to "Plug", moved the appropriate "VL-PS-WALL*" cable part number to the Transition Cable column, and added in the Cable Description "AC/DC *(12 or 5)V Power Adapter"
- For J16, added to Mating Connector column, "Housing = Molex 51065-0500 and Pin Crimps = Molex 050212-8000," moved the "VL-CBR-0504" over to the Transition Cable column, and added "DB9 COM Port Interface Cable" to the Cable Description column
- For J17, added to Mating Connector column: Housing = Molex 51065-0400 and Pin Crimps = Molex 050212-8000
- For J20 in the Device Description, added "When selecting an add-on board, reference the pinout information to determine compatibility."
- Added Wi-Fi and Bluetooth content in the Network Interfaces section
- Added Wi-Fi and Bluetooth information to the "Initial Configuration" and "Basic Setup" sections
- Added Wi-Fi/BT U.FL connector information to Figure 3 and Table 2
- Added References for Wi-Fi and Bluetooth parts

Rev 1.6 Added a note to table 10 regarding backdrive power

Rev 1.7 Added illustration depicting opening the MicroSD cover (Figure 4)

Support Page

The Swordtail Product Page contains additional information and resources for this product including:

- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- U-Boot information and upgrades

Customer Support

If you are unable to solve a problem after reading this manual, visiting the product support page, contact VersaLogic Technical Support at (503) 747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

Repair Service

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261. Be ready to provide the following information:

- Your name, the name of your company, your phone number, and e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- The quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair: All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses. For international address the customer is fully responsible for shipping (including taxes and duties) to and from the factory.

Non-warranty Repair: All approved non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Mark the RMA number clearly on the outside of the box before returning.

Contents

Figures

Tables

Introduction 1

Description

Features and Construction

The Swordtail single-board computer is a complete Wi-Fi and Bluetooth* enabled, Arm*-based embedded computer. Models are available with power-efficient, dual-core or quad-core i.MX6 CPUs. These boards are designed for applications that demand rugged, power-efficient solutions such as industrial machine automation, transportation, medical, kiosk, and industrial IoT applications. Swordtail boards have been designed to enable transactions and transmission of maintenance or diagnostic information without the presence of a wired data connection. Both Wi-Fi and Bluetooth radios are included on board, and a NimbleLink Skywire* socket supports a wide range of optional cellular and other wireless plug-ins.

Swordtail is a complete board- level computer. Additional carrier boards, connector boards, or I/O expansion boards are not required for operation. Swordtail boards are delivered with on-board soldered-down RAM, ready to plug-in and run. To simplify mounting and future upgrades, the Swordtail leverages the COM-Express standard for its footprint and mounting points.

- Arm* i.MX6 dual or quad-core processors
- 95 x 95 mm size
- Low power draw
- Fanless operation
- Up to 4 GB soldered-on RAM
- Gigabit Ethernet
- HDMI video
- LVDS video
- CAN Bus
- Cellular support
- Bluetooth
- Wi-Fi
- USB 2.0 ports
- MicroSD card socket
- RS-232
- I^2C with interrupt input support
- Optional eMMC Flash. Up to 32 GB
- Linux support

VL-EPC-2702 boards receive complete functional testing and are backed by a limited five-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service, and product longevity for this exceptional single-board computer (SBC).

Technical Specifications

See the Swordtail Data Sheet for complete specifications.

Thermal Considerations

The operating temperature for the Swordtail is -40°C to +85°C, de-rated -1.1°C per 305m (1,000 ft.) above 2,300m (7,500 ft.).

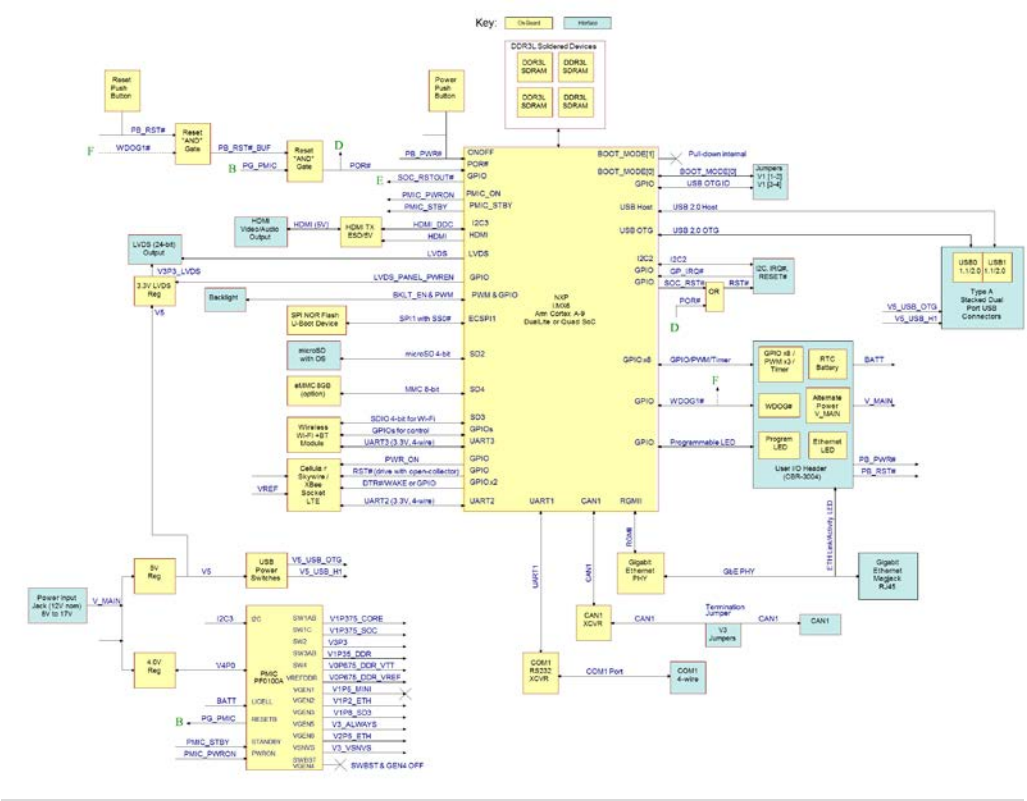
Table 1. Environmental Specifications

Characteristic	Value
Operating Temperature	Ext Temp *(-40°C to +85°C)*
Storage Temperature	-40°C to +85°C
Cooling	Fanless. Heatsink for SoC
Airflow Requirements	100 Linear Feet per Minute
Thermal Shock	5ºC/min. over operating temperature
Humidity	Less than 95%, noncondensing
Vibration, Sinusoidal Sweep	MIL-STD-202H Sinusoidal sweep: Method 204, Modified Condition A, 2g constant acceleration from 5 to 500 Hz, 20 minutes per axis
Vibration, Random	Random vibration: Method 214A, Condition A, 5.35g rms, 5 minutes per axis
Mechanical Shock	Shock: Method 213B, Condition G, 20g half-sine, 11 msec duration per axis

Note: Cellular modules may become unseated during vibrations and mechanical shock. Evaluate for each usage case.

Block Diagram

Figure 1. Swordtail Board Block Diagram



Cautions

Electrostatic Discharge

CAUTION:

Electrostatic discharge (ESD) can damage circuit boards, disk drives, and other components. Handle circuit board at an ESD workstation. If an approved station is not available, wearing a grounded antistatic wrist strap provides some measure of protection. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

Ship and store the board inside a closed metallic antistatic envelope for protection.

Note: The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom side of the Swordtail.

Handling Care

CAUTION:

Avoid touching the exposed circuitry with your fingers when handling the board. Though it will not damage the circuitry, it is possible that small amounts of oil or perspiration on the skin could have enough conductivity to cause the contents of CMOS RAM to become corrupted through careless handling, resulting in CMOS resetting to factory defaults.

Earth Ground Requirement

CAUTION:

All mounting standoffs for EPC boards should be connected to earth ground (chassis ground). This provides proper grounding for EMI purposes.

Configuration and Setup 2

Initial Configuration

Use the following components for a typical development system:

- Swordtail (VL-EPC-2702) computer
- VL-PS-WALL12-24 wall mount 12V 24W power supply
- VL-F41-8SBN-LINUX3 – 8GB MicroSD card with bootable Linux, standard temp
- VL-CBR-0205 cable and VL-CBR-ANT04 antenna – shared for Wi-Fi and Bluetooth
- USB keyboard and mouse
- HDMI monitor and cable

Note: VL-CKR-Swordtail includes VL-F41-8SBN-LINUX3, CBR-0205, CBR-ANT04, CBR-0504, CBR-3004 and PS-WALL12-24.

Basic Setup

1. Attach Cables and Peripherals

- Attach the VL-PS-WALL12-24 to a wall outlet but DO NOT connect it to the computer yet
- Attach a HDMI display to the HDMI connector at J6
- Plug in a USB keyboard, and a USB mouse into the USB connectors at J1

  Note: If using the top USB port, you must install the jumper on V1 pins 3-4 for the OTG USB port to be placed in Host mode. Alternatively, you can use an external USB Hub to provide separate mouse and keyboard connections for the bottom USB port. Make sure the upstream USB Hub port (connecting to the EPC-2702 host port) does not provide VBUS power, but the downstream USB Hub port(s) can be externally powered to ease the loading on the EPC-2702 power supply.
- Attach the CBR-ANT04 to the CBR-0205 cable, and then attach the U.FL end to the Wi-Fi / Bluetooth module U42's U.FL connector. This cable and antenna combination provides the approved wireless communications interface for both Wi-Fi and Bluetooth simultaneously at 2.4 GHz
- Insert a VL-F41-8SBN-LINUX3 MicroSD card into the MicroSD slot located at J4

  Note: The top of the MicroSD socket slides down and then the lid rotates open. Use caution when opening.

2. Review Configuration

- Before you power up the system, double-check all the connections. Make sure all cables are oriented correctly and that there is adequate power to the VL-EPC-2702 and peripheral devices.

3. Power On

- Turn on the video monitor, and then plug the power adapter cable VL-PS-WALL12-24 into the computer power jack J15. The presence of a video signal indicates proper configuration of the system.

Note: Booting and operating the Yocto Linux operating system is covered in the VersaLogic Yocto Linux User Guide.

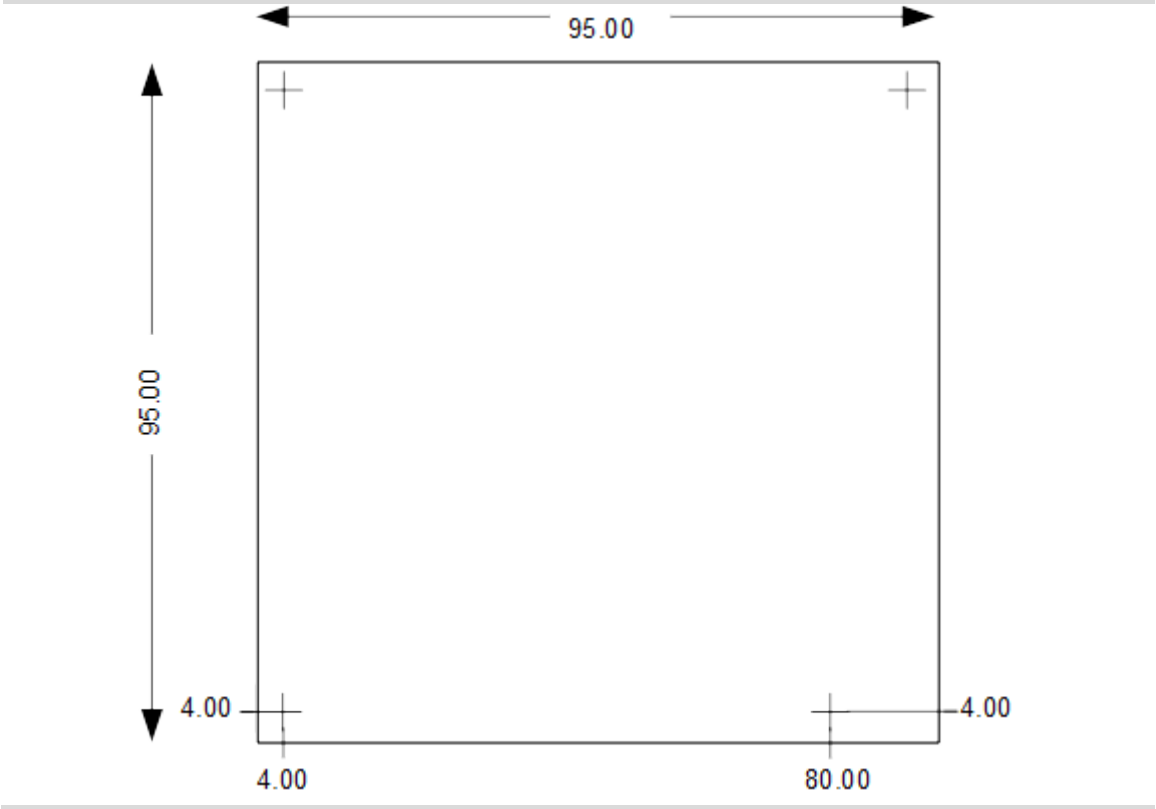
Physical Layout

Swordtail Dimensions

The figure below shows board dimensions to help with pre-production planning and layout.

Figure 2. Swordtail Board Dimensions and Mounting Holes

(Not to scale. All dimensions in millimeters.)

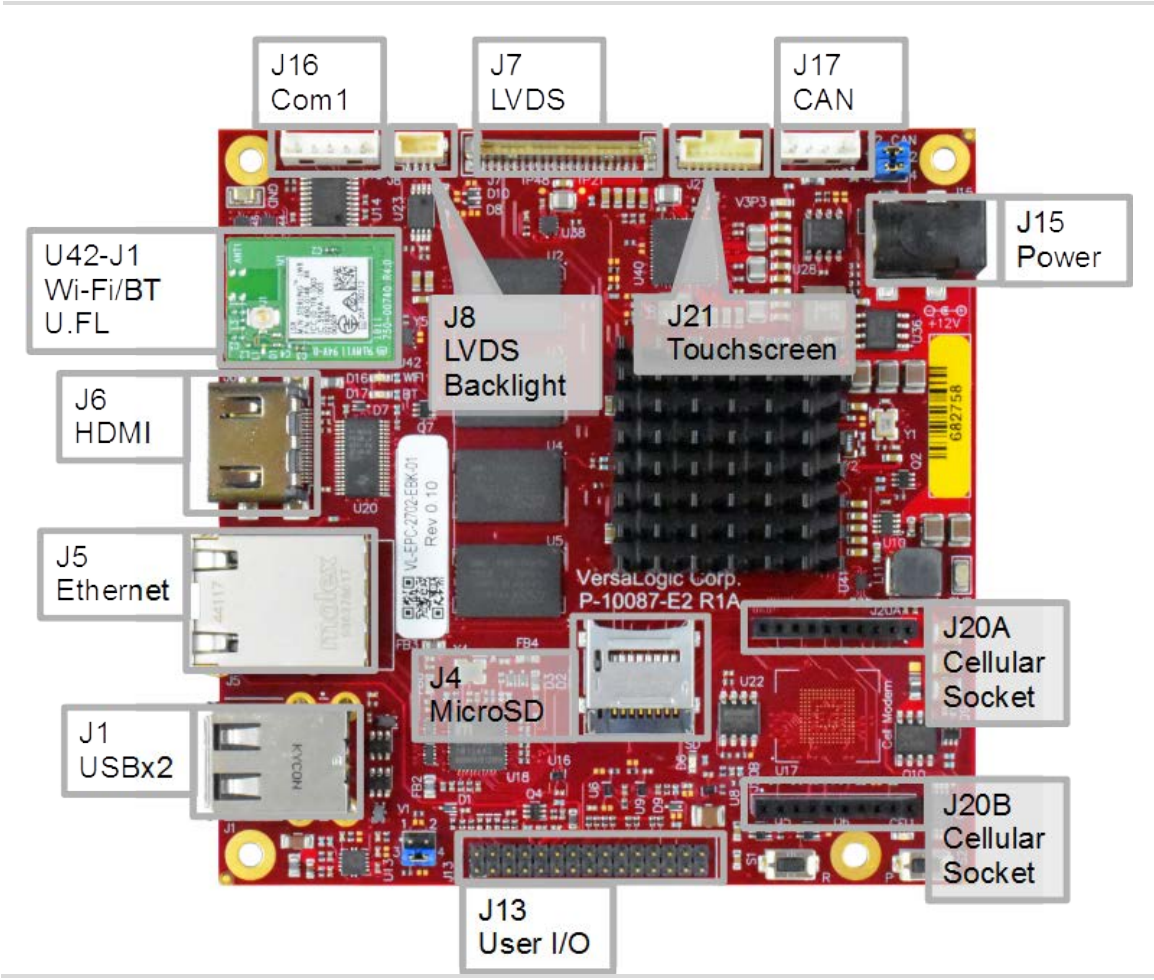


Hardware Assembly

The entire assembly can fit on a tabletop. When bolting the unit down, make sure to secure all standoffs to the mounting surface to prevent circuit board flexing. Standoffs secure the top circuit board using four pan head screws.

External Connectors

Figure 3. Connector Locations



Swordtail Connector Functions and Interface Cables

The table below provides information about the function, mating connectors, and transition cables for Swordtail connectors.

Table 2. Connector Functions and Interface Cables

Connector	Function	Mating Connector/Device	Transition Cable	Cable/Device Description
U42-J1	U.FL Antenna	U.FL	VL-CBR-0205 (Laird 080-0001)	U.FL to RP-SMA connects to VL-CBR-ANT04 (Wi-Fi/BT Antenna – Laird 001-0001)
J1	USB (dual stacked)	Standard USB Type A	USB	Male Type A USB 2.0 to Male Type B for downstream devices, Male Type A USB 2.0 to Male Type A USB 2.0 for top port only when OTG port is set as Device mode (V1 jumper off).
J4	MicroSD	8GB microSD card with bootable Linux 2GB microSD card 4GB microSD card 8GB microSD card	N/A	VL-F41-8SBN-LINUX3 (MLC, Standard Temperature) VL-F41-2EBN (SLC, Extended Temperature) VL-F41-4EBN (SLC, Extended Temperature) VL-F41-8EBN (SLC, Extended Temperature)
J5	Ethernet	RJ45 Crimp-on Plug	Cat5e	Cat5e Ethernet Patch Cable
J6	HDMI	Standard HDMI Plug	HDMI	Standard HDMI Cable
J7	LVDS Panel	Housing = Hirose DF19G-20S-1C Pin Crimps = Hirose DF19-2830SCFA	VL-CBR-2015 VL-CBR-2016 VL-CBR-2017	20-pin Hirose 1mm to Hirose 1mm 24-bit cable 20-pin Hirose 1mm to JAE 1.25mm 18-bit cable 20-pin Hirose 1mm to 20-pin Hirose 1.25mm 24-bit cable
J8	Backlight	Housing = Molex 501330-0400 Pin Crimps = Molex 501193-2000	VL-CBR-0404	20" 12V LED Backlight Control Cable
J13	User I/O	0.5m 30-pin 2mm IDC to Ribbon Cable	VL-CBR-3004	User Input/Output Interface Ribbon Cable
J15	Power	DC Power Plug for.0mm positive center pin	VL-PS-WALL12-24	AC/DC 12V Power Adapter
J16	COM1	Housing = Molex 51065-0500 Pin Crimps = Molex 050212-8000	VL-CBR-0504	DB9 COM Port Interface Cable
J17	CAN1	Housing = Molex 51065-0400 Pin Crimps = Molex 050212-8000	VL-CBR-0405 VL-CBR-0406	(Micro-Latch to Micro-Latch) (Micro-Latch to DB9)
J20A/J20B	Cellular Socket	20-pin NimbleLink Skywire socket	N/A	When selecting an add-on board, reference the pinout information to determine compatibility.
J21	Touchscreen	Housing = Molex 501330-0800 Pin Crimps = Molex 501193-3000	VL-CBR-0811	Touchscreen Support (20" 8-pin Pico-Clasp / 8-pin Pico-Clasp)

Table 3. Jumper Information

EPC-2702 Reference Designator	EPC-2702 Signal Name	Control/Description
V1	Pins 1-2 - BOOT_MODE0 Pin 3-4 - USB_OTG_ID	Default: One jumper stored on pin 4 With jumper installed on pins 1-2, BOOT_MODE0 = 1, to allow use of USB OTG Device communications using the NXP i.MX6 Serial Downloader method. When this jumper is installed V1 pins 3-4 should not have a jumper installed. With the jumper installed on pins 3-4, the USB OTG port behaves as a Host Port and will enable the power switch to the Type A connector (top socket of J1), ensure that the cable connection goes to a Device and not another Host.
V2	Pins 1-2 - CAN1_SPLIT / CAN1_R_P Pins 3-4 - CAN1_SPLIT / CAN1_R_N	Default: One jumper on pins 1-2 and one jumper on pins 3-4 sets 120 Ohm termination for end node and split termination capacitor connections between CAN1_P/N. Remove both jumpers to disconnect all termination. Place one jumper across pins 2-4 to bypass capacitor to have 120 Ohms resistor termination only.

System Features 3

Power Supply

Power Connectors

Main power may be applied to the Swordtail through a DC Power Jack (J15) or through alternate power input pins on the User I/O Interface connector (J13). For pin details on using the alternate power input method, please see the User I/O section later in this document. Use only one power input method.

The VersaLogic VL-PS-WALL12-24 plugs into an AC outlet and provides a 12V DC input for the Swordtail via a 2.1 mm center positive DC plug. See the table below for the connector interface.

CAUTION:

To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. The power connector is not fuse or diode protected. Proper polarity must be followed otherwise damage will occur.

Table 4. DC Power Jack Interface

Signal	Description
V_MAIN	Center Pin Voltage
Ground	Ground Sleeve

Table 5. Power Requirements

Model	Idle	Typical	Max.
VL-EPC-2702-EBK-01	1.74W	2.25W	2.75W
VL-EPC-2702-EDK-02	2.03W	2.97W	3.9W

Note: The power measurements reflect the Ethernet (eth0) down and Wi-Fi (wlan0) producing the connected values while running a benchmark test in Linux called Himeno with 4 threads. The test was run at room temperature.

CPU

The Swordtail uses a low power Arm i.MX 6 DuaLite or Quad-core processor.

- NXP i.MX 6Dual/**6Quad** Arm processors - Specification
- NXP i.MX 6Solo/**6DualLite** Arm processors – Specification

System RAM

The Swordtail ships with 1 GB with the DualLite or 2 GB with the Quad of soldered-on DDR3L RAM. Both processors allow for customization of memory device capacities providing 1 GB, 2 GB, or 4 GB.

RTC Battery

There are two pins dedicated for an RTC Battery input on the User I/O connector J13 (See Table 15. User I/O Pinouts).This 3.0V battery (or power supply) connection allows the real time clock in the i.MX 6 to remain powered and running while the board input power is turned off. In order to size the battery appropriately for your application, please use the following information:

At 25°C ambient operation, each year of RTC battery power requires 8760 hrs x 73.4µA = 643mAh.

Note: The PMIC will power the i.MX 6 RTC circuits from the board power whenever it is available, so the battery would only need to cover the expected percentage of time that the board input power is not on and it switches over to the battery power source.

Interfaces and Connectors 4

Headers and Jumpers

V1 – BOOT_MODE0/USB_OTG_ID Jumper

The EPC-2702 uses a 4-pin jumper to provide access to two required boot modes as well as providing a control setting for the USB OTG block to function as either an OTG port set to device mode or set to host mode.

The jumper ships in a storage position, with the boot mode defaulting to boot from the eFuses and the USB OTG port set to Device mode (top USB port on J1). Putting the jumper on pins 1-2 allows the board to run in Serial Download mode waiting to boot from a USB Host connection (local USB set to device mode by default). Putting the jumper on pins 3-4 sets the USB OTG port to Host mode, allowing the user to connect a downstream device. Never use more than one jumper on this header as there is no case where that would be useful.

Note: For custom product designs, there are placeholders to bypass and hard strap the jumper settings.

Table 6. V1 Pinout

Pin	Signal Name
1	PU_BOOT_MODE0
2	BOOT_MODE0
3	USB_OTG_ID
4	GND

V2 - CAN1 Termination Jumper

The EPC-2702 uses two jumpers to provide two 60 Ohm bus termination resistors. There is a split termination capacitor to GND between them for the CAN1 bus termination solution when a jumper is installed each on pins 1-2 and pins 3-4. The split termination capacitor can be removed from the path by removing these two jumpers and placing one of them on pins 2-4 to provide only the 120 Ohm bus termination.

If no termination enabled is preferred (when the bus is mid-point on a CAN bus network), both jumpers can be removed to open the termination path for the bus signals.

Note: For custom product designs, there are placeholders to bypass the jumper and still provide any combination of terminations.

Table 7. V2 Pinout

Pin	Signal Name
1	CAN1_SPLIT (tied to pin 3)
2	CAN1_R_P (CAN1_P)
3	CAN1_SPLIT (tied to pin 1)
4	CAN1_R_N (CAN1_N)

Storage Interfaces

Up to 32GB of eMMC Flash storage is available with customization.

MicroSD Interface (J4)

The table below lists the pinout of the 8-pin MicroSD connector.

Supported VersaLogic SLC extended temperature cards:

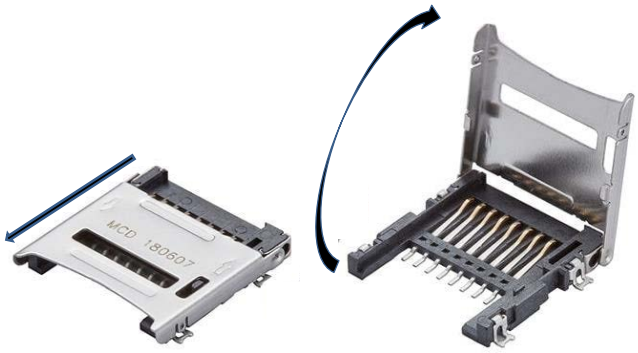
- VL-F41-2EBN (2 GB)
- VL-F41-4EBN (4 GB)
- VL-F41-8EBN (8 GB)

Note: MicroSD card number VL-F41-8SBN-LINUX3 is an 8 GB MLC MicroSD card with bootable Linux, standard temperature

Table 8. J4 MicroSD Pinout

Pin	Signal
1	DAT2
2	CD/DAT3
3	CMD
4	VDD (+3.3V)
5	CLK
6	VSS (GND)
7	DAT0
8	DAT1

Figure 4. Opening the MicroSD Cover



Network Interfaces

Wi-Fi and Bluetooth

Wi-Fi and Bluetooth support is provided via the Laird Connectivity Sterling-LWB module. The Sterling-LWB is a 2.4 GHz Wi-Fi and Bluetooth Smart Ready Multi-Standard Module that is soldered on the VL-EPC-2702 as component U42. There is a U.FL antenna connector on the module (U42-J1) that supports both the Wi-Fi and Bluetooth communications simultaneously. The module is pre-certified with the use of Laird's 080-0001 U.FL to RP-SMA cable adapter and Laird's 001-0001 2.4 GHz Dipole Antenna.

There are other antennas that have been certified with the Sterling-LWB module. Refer to the Application Guide (referenced in Appendix A - References - section 7.2). There is more certification information in the Sterling LWB/LWB5 Certification Guide (https://connectivity-staging.s3.us-east-2.amazonaws.com/2019-03/LWBCert.pdf).

To certify different antennas and/or U.FL cables for Wi-Fi / Bluetooth:

https://connectivity-staging.s3.us-east-2.amazonaws.com/s3fs-public/2019-01/Application%20Note%20-%20Guidelines%20for%20Replacing%20Antennas%20v1_0.pdf

Note: End products containing the VL-EPC-2702 will require testing per this notification from Laird Connectivity:

http://go.pardot.com/webmail/647203/74547931/a66d3e0af3a350e4637b86a2e965b9556b44b5782f2b1880ccda219aca42d7b8

Ethernet Interface (J5)

The table below lists the pinout of the Ethernet connector.

Table 9. J5 Ethernet RJ45 Pinout

J5 RJ45 Pin #	Wire-Color (CAT5E)	10/100 Signals	10/100/1000 Signals
1	White/Orange	+ Auto Switch (can be either Tx or Rx)	BI_DA+
2	Orange	- Auto Switch (can be either Tx or Rx)	BI_DA-
3	White/Green	+ Auto Switch (can be either Tx or Rx)	BI_DB+
4	Blue	+ Auto Switch (can be either Tx or Rx)	BI_DC+
5	White/Blue	- Auto Switch (can be either Tx or Rx)	BI_DC-
6	Green	- Auto Switch (can be either Tx or Rx)	BI_DB-
7	White/Brown	+ Auto Switch (can be either Tx or Rx)	BI_DD+
8	Brown	- Auto Switch (can be either Tx or Rx)	BI_DD-

Video Interfaces

HDMI (J6)

Table 10. HDMI Connector Pinout

Pin	Signal	Direction	Description
1	HDMI_D2_P	Out	HDMI Data 2 Differential Pair +
2	DATA2SHIELD	--	Ground
3	HDMI_D2_N	Out	HDMI Data 2 Differential Pair -
4	HDMI_D1_P	Out	HDMI Data 1 Differential Pair +
5	DATA1SHIELD	--	Ground
6	HDMI_D1_N	Out	HDMI Data 1 Differential Pair -
7	HDMI_D0_P	Out	HDMI Data 0 Differential Pair +
8	DATA0SHIELD	--	Ground
9	HDMI_D0_N	Out	HDMI Data 0 Differential Pair -
10	CLK_HDMI_P	Out	HDMI Clock Differential Pair +
11	CLKSHIELD	--	Ground
12	CLK_HDMI_N	Out	HDMI Clock Differential Pair -
13	HDMI_CEC_CON	I/O	HDMI CEC Line
14	HDMI_NC_CON	N/A	No Connect - Resistor to GND option
15	HDMI_SCL_CON_R	Out	DDC Serial Clock Line (5V signal)
16	HDMI_SDA_CON_R	I/O	DDC Serial Data Line (5V signal)
17	HDMI_CEC_GND	I/O	CEC_GND - 0 Ohm Resistor to GND
18	V5_HDMI_CON	Out	5V HDMI Cable Power
19	HDMI_HPD_CON	In	HDMI Hot Plug Detection Signal

Note: Some back-drive occurs when an HDMI panel has power and is connected to an unpowered board.

LVDS (J7)

Table 11. LVDS Connector Pinout

Pin	Signal	Description
1	GND	Signal Ground
2	GND	Signal Ground
3	LVDS_TX3_P	LVDS Data 3 (positive)
4	LVDS_TX3_N	LVDS Data 3 (negative)
5	GND	Signal Ground
6	CLK_LVDS_P	LVDS Clock (positive)
7	CLK_LVDS_N	LVDS Clock (negative)
8	GND	Signal Ground
9	LVDS_TX2_P	LVDS Data 2 (positive)

Pin	Signal	Description
10	LVDS_TX2_N	LVDS Data 2 (negative)
11	GND	Signal Ground
12	LVDS_TX1_P	LVDS Data 1 (positive)
13	LVDS_TX1_N	LVDS Data 1 (negative)
14	GND	Signal Ground
15	LVDS_TX0_P	LVDS Data 0 (positive)
16	LVDS_TX0_N	LVDS Data 0 (negative)
17	GND	Power Ground
18	GND	Power Ground
19	V3P3_LVDS_PANEL	LVDS Panel Power (+3.3V)
20	V3P3_LVDS_PANEL	LVDS Panel Power (+3.3V)

LVDS Backlight (J8)

Table 12. LVDS Backlight Connector Pinout

Pin	Signal	Description
1	LVDS_BKLT_EN	Backlight Enable for LVDS panel
2	GND	Ground
3	LVDS_BLKT_CTRL	Backlight Control for LVDS panel (PWM)
4	V_LVDS_BKLGT	Voltage for LVDS Backlight control

Touchscreen (J21)

Table 13. Touchscreen Pinout

Pin	Signal	Description
1	CLK_I2C2_SCL	I^2C Bus Clock
2	GND	Ground (black wire)
3	I2C2_SDA	I^2C Bus Data
4	GND	Ground (black wire)
5	GP_IRQ#	General Purpose Interrupt Request Input (active low)
6	GND	Ground (black wire)
7	SYSTEM_RST#	System Reset output (active low)
8	V3P3_LVDS	+3.3V Power

I/O Interfaces

USB Interfaces (J1)

Table 14. USBx2 2.0 Connector Pinout

Pin	Signal	Description
T1	V5_USB0_OTG	Top Connector Switched USB +5V Power
T2	USB0_OTG_N	USB OTG DN diff pair -
T3	USB0_OTG_P	USB OTG DP diff pair +
T4	GND	Top Connector Ground
TM1	V5_USB1_H1	Bottom Connector Switched USB +5V Power
TM2	USB1_H1_N	USB Host1 DN diff pair -
TM3	USB1_H1_P	USB Host1 DP diff pair +
TM4	GND	Bottom Connector Ground

User I/O (J13)

Table 15. User I/O Pinouts[1]

Pin	Signal	Description	Pin	Signal	Description
1	GPIO9	3.3V General Purpose I/O	2	GND	Ground
3	PB_CTL_PWR#	Open-Drain Push Button Control Power Input	4	GND	Ground (for PB_CTL_PWR#)
5	PB_CTL_RST#	Open-Drain Push Button Control Reset Input	6	GND	Ground (for PB_CTL_RST#)
7	PLED#	Open-Drain 3.3V max Programmable LED driver	8	V3P3	3.3V power for Programmable LED
9	LED_ETH_GRN#	Open-Drain 3.3V max Ethernet LED driver	10	V3P3	3.3V power for Ethernet LED
11	WDOG1#	Watch dog 1 Output	12	GND	Ground
13	GPIO1	3.3V General Purpose I/O	14	GPIO2	3.3V General Purpose I/O
15	GND	Ground	16	GPIO3	3.3V General Purpose I/O
17	GPIO4	3.3V General Purpose I/O	18	GND	Ground
19	GPIO5	3.3V General Purpose I/O	20	GPIO6	3.3V General Purpose I/O
21	GND	Ground	22	GPIO7	3.3V General Purpose I/O
23	GPIO8	3.3V General Purpose I/O	24	GND	Ground
25	V_BATT	Battery Input (3.0V Coin Cell)	26	RETURN_BATT/GND	Tied to GND on CPU board and direct to the battery minus terminal on a paddleboard or external battery connector.
27	GND	Ground (for V_MAIN)[2]	28	GND	Ground (for V_MAIN)[2]
29	V_MAIN	V_MAIN power. Can be supplied by this connector or provided to add-in cards through this connector. (bypassed to ground). Voltage can be 8V to 17V (default 12V).	30	V_MAIN	V_MAIN power. Can be supplied by this connector or provided to add-in cards through this connector. (bypassed to ground). Voltage can be 8V to 17V (default 12V).

Notes

[1] GPIO1, GPIO3, and GPIO7 can alternatively be setup as PWM outputs (Contact VersaLogic for details)

[2] : Keep current safely below 2A total

CAN Interface (J17)

Table 16. CAN Pinouts

Pin	J17 Signal	Description
1	CAN1_P	CANH signal for CAN bus
2	CAN1_N	CANL signal for CAN bus
3	GND	Ground
4	V5	5V power (for off-board use)

Note: Keep 5V signal under 0.5A.

COM1 Interface (J16)

Table 17. COM1 Pinout

Pin	Signal	Description
1	COM1_RTS	COM1 RS-232 Request to Send
2	COM1_TXD#	COM1 RS-232 Transmit Data (active low)
3	COM1_CTS	COM1 RS-232 Clear to Send
4	COM1_RXD#	COM1 RS-232 Receive Data (active low)
5	GND	Ground

Cellular Socket (J20A and J20B together form 20-pin socket)

The design of the cellular socket fully supports Skywire modems. With minimal board customizations, the socket can also support some Digi XBee or XBee3 modems or RF Modules.

Note: XBee and XBee3 are available via customization. For more information, please contact VersaLogic.

The end product manufacturer is responsible for compliance with FCC requirements.

Table 18. Cellular Socket Pinout

J20(A) Pin	Skywire Cellular Modems Socket Signal	XBee/XBee3 Cellular Modems (or Other RF) Socket Signal Custom Option	Skywire Description for Socket Default	XBee/XBee3 RF Modules Description for Customization Option
1	VCC	VCC	Main Power Supply for Modem (4.0V)	Main Power Supply for Modem (stuff option to change to 3.3V)
2	DOUT	DOUT (DIO13)	Cellular Modem UART data out	Same (GPIO on XBee3 RF)
3	DIN	DIN (CONFIG#/DIO14)	Cellular Modem UART data in	Same (GPIO on XBee3 RF)
4	GND	DIO12/SPI_MISO	Ground for socket on Skywire	GPIO/SPI data output line Defaults to disabled, so hard GND signal OK.

J20(A) Pin	Skywire Cellular Modems Socket Signal	XBee/XBee3 Cellular Modems (or Other RF) Socket Signal Custom Option	Skywire Description for Socket Default	XBee/XBee3 RF Modules Description for Customization Option
5	RESET#	RESET#	Modem active-low reset input, must be driven low for 20 msec minimum (on some modems) and then released to activate. Internally (on modem) pulled up to VCC or an I/O voltage rail. Must be driven with an open collector output without a pull resistor. After power-on, only use in emergency (not a "graceful" reset).	Same
6	VUSB	PWM0/RSSI/DIO10 or USB_VBUS	USB Power Detection Pin (4.5V to 5.5V). Used to turn on the USB interface. Disabled by default, but canbe electronically switched on along with the differential pair on pins 7 and 8 to provide the USB interface to the Skywire.	PWM Output 0 / RX Signal Strength Indicator / Digital I/O 10, defaults to output on all Digi modems. Can be configured on LTE-M modem for the USB interface use, but suggested use is 3.3V instead of 5V. Stuff option to connect switch to 3.3V.
7	USB_D+	USB_D+ (PWM1/DIO11)	USB differential Data + signal	Same on some. (PWM Output 1 / Digital I/O 11, defaults to disabled)
8	USB_D-	USB_D- or RSVD	USB differential Data - signal	Same on some. (Reserved on XBee/XBee3, defaults to disabled)
9	WAKE or DTR#	DTR# (SLEEP_RQ/DIO8)	Wakes up the modem from low power modes. Default configuration for wakeup is a low to high transition on this line. Data Terminal Ready (active low) on some modems. Pulled-down on board by default.	Data Terminal Ready (Sleep Control Line / Digital I/O 8)
10	GND	GND	Power/Signal Ground for socket	Same
11	GND	DIO4/SPI_MOSI	Ground for socket on Skywire	GPIO/SPI data input line Defaults to disabled, so hard GND signal OK.
12	CTS#	CTS# (DIO7)	Cellular Modem UART Clear to Send hardware flow control out	Same (Digital I/O 7)
13	ON_STATUS	ON/SLEEP# (DIO9)	Modem status indicating it is on and ready for commands when high (it can be idle, blink with activity, or off in sleep mode). NC if not used.	Module status indicator (Digital I/O 9)
14	VREF	Reserved/VREF	Voltage reference for I/O signals (set to 3.3V), drives input voltage side of modem buffers converting external I/O voltage from VREF to the I/O voltage used to drive the onboard modem module for Skywire.	Not supported on XBee or XBee3 Modems, but used on other XBee devices for analog voltage reference. Could be switched off for customs.

J20(A) Pin	Skywire Cellular Modems Socket Signal	XBee/XBee3 Cellular Modems (or Other RF) Socket Signal Custom Option	Skywire Description for Socket Default	XBee/XBee3 RF Modules Description for Customization Option
15	GND	Associate/DIO5	Ground for socket on Skywire	Defaults to Associated Indicator Output (Digital I/O 5) Since this pin must be grounded per Skywire, it has a 0 Ohm resistor to GND. Customs could remove the resistor and use the pad as a test point.
16	RTS#	RTS# (DIO6)	Cellular Modem UART Request to Send hardware flow control in. Pulled-down on board by default.	Same (Digital I/O 6)
17	Reserved, I^2C, or GPIO	AD3/DIO3/SPI_SS#	Most Skywire modems have this as a 1.8V GPIO, but the SVZM20 has it reserved and the QBG96 has is as an I^2C data signal. NOT CONNECTED	Analog Input 3 / Digital I/O 3 / SPI low enabled select line (defaults to disabled) NOT CONNECTED
18	Reserved, I^2C, or GPIO	AD2/DIO2/SPI_CLK	Most Skywire modems have this as a 1.8V GPIO, but the SVZM20 has it reserved and the QBG96 has is as an I^2C clock signal. NOT CONNECTED	Analog Input 2 / Digital I/O 2 / SPI clock line (defaults to disabled) NOT CONNECTED
19	RING or ADC1	AD1/DIO1/SPI_ATTN#	RING signal wakes up a host processor when there is incoming traffic on the network. ADC1 is an analog input (0 to 1.2V). NC if not used. Default is to pull-down (1k) this pin, but have stuff option to connect it to an i.MX6 GPIO for customs.	Analog Input 1 / Digital I/O 1 / SPI Attention low enabled line output (defaults to disabled)
20	ON_OFF or PWR_ON	AD0/DIO0	ON_OFF = Modem PWR_ON is active low internally pulled up to internal I/O rail with resistor. Do not use external pull ups. Note: If you want modem to turn on automatically when power is applied, permanently tie this signal to GND using stuff option.	Analog Input 0 / Digital I/O 0 (defaults to input)

Push Buttons

Table 19. Push Buttons and Designators

Reference Designator	Signal Name	Description
S1	PB_CTL_RST#	Push Button Control for Power-On Reset
S2	PB_CTL_PWR#	Push Button Control for PMIC Power Outputs

Notes:

1) A momentary push of S1 or a low pulse (~100ms or more) using an open-drain driver from the User I/O connector pin (J13 – pin 5) will force a reset of the board.

2) Holding the S2 power pushbutton in or driving the signal low (using open-drain driver) from the User I/O connector pin (J13 - pin 3) is the only way to turn off the power to the processor and I/O when the board input power is still being applied.

References 5

- Yocto Linux User Guide for the VL-EPC-2702
- i.MX6Dual/6Quad Applications Processors for Industrial Products Datasheet
- i.MX6Solo/6DualLite Applications Processors for Industrial Products Datasheet
- Hardware Development Guide for i.MX6 Families of Application Processors
- NXP Website Documentation for the Quad: https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-processors/i.mx-6quad-processors-high-performance-3d-graphics-hd-video-arm-cortex-a9-core:i.MX6Q?tab=Documentation_Tab
- NXP Website Documentation for the DualLite: https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-processors/i.mx-6duallite-processors-dual-core-3d-graphics-hd-video-arm-cortex-a9-core:i.MX6DL?tab=Documentation_Tab
- NimbeLink NL-SW-LTE-SVZM20: https://nimbelink.com/products/4g-lte-m-verizon-sequans/
- NimbeLink NL-SW-LTE-GELS3: https://nimbelink.com/products/4g-lte-cat-1-verizon-gemalto/
- Wi-Fi / Bluetooth Sterling-LWB Module Documentation: https://www.lairdconnect.com/wireless-modules/wi-fi-bt-modules/sterling-lwb
- Wi-Fi / Bluetooth Sterling-LWB Module Application Guide: https://connectivity-staging.s3.us-east-2.amazonaws.com/2019-03/330-0192.pdf
- FCC guidance for equipment authorization of transmitter module devices: https://apps.fcc.gov/oetcf/kdb/forms/FTSSearchResultPage.cfm?switch=P&id=44637
- CAN transceiver device datasheet: http://www.ti.com/lit/ds/symlink/sn65hvd230.pdf

KNOWN ISSUES

- The i.MX 6 SW controlled power-off is unsupported. In order to turn off the PMIC power output while the power input to the board is still supplied, you must either hold the S2 power pushbutton in or drive the PB_CTL_PWR# signal on the User IO connector (J13) low (with an open-drain driver) since the input is level sensitive by default.
- At high temperatures, the thermal sensor can sometimes not be read, resulting in the loss of thermal protection. The following command was found to allow completion of our verification testing.

  ```
  echo enabled > /sys/class/thermal/thermal_zone0/mode
  ```

- The Ethernet controller and UFD intermittently do not show up during power cycle test. This event is caused by systemd being used for initialization instead of the sysvinit method used in the previous Yocto versions. The released Yocto SD card image has systemd disabled. In order to disable systemd for a newly built image, edit a file in the NXP BSP (sources/meta-fsl-bsp-release/imx/meta-sdk/conf/distro/include/fsl-imxpreferred-env.inc) and comment out the following:

  ```
  #VIRTUAL-RUNTIME_init_manager = "systemd"

  #PREFERRED_PROVIDER_udev = "systemd"

  #PREFERRED_PROVIDER_udev-utils = "systemd"
  #DISTRO_FEATURES_BACKFILL_CONSIDERED = "sysvinit"

  #IMX_DEFAULT_DISTRO_FEATURES += " systemd"
  ```

- Ethernet system limitation per i.MX6 chip errata ERR004512 (for Solo/DualLite and Quad):

  The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx). The actual measured performance in an optimized environment is up to 400 Mbps.