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Going Faster and Further with Fieldbus

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Introduction

Industry experts, such as PROCENTEC, show steady growth in RS-485-based fieldbus technology adoption (PROFIBUS®) and rapid growth for Industrial Ethernet (PROFINET). In 2018, there were 61 million PROFIBUS fieldbus nodes installed worldwide, with PROFIBUS process automation (PA) growing 7% year on year. The PROFINET install base is at 26 million nodes, with 5.1 million devices installed in 2018 alone.[1]

With this steady growth in RS-485 fieldbus adoption and Industry 4.0 accelerating the deployment of smart connected factories, ensuring that fieldbus technologies are optimized helps to enable a smart system. Optimized fieldbus technologies must carefully balance EMC robustness and reliable data transmission.

Unreliable data transmission will reduce overall system performance. In motion control applications, fieldbus is typically used for closed-loop position control of single-axis or multiaxis motors. High data rates and long cables are common, as shown in Figure 1. If position control is unreliable, then performance degradation in practical terms means lower quality machine throughput and reduced factory productivity. In wireless infrastructure applications, fieldbus is typically used for tilt/position control of antenna, where accurate data transmission is critical. In both motion control and wireless infrastructure applications, varying levels of EMC protection are required, as shown in Figure 1. Motion control applications typically operate in electrically noisy environments, which may cause data errors. In comparison, wireless infrastructure must be protected against damaging indirect lightning strikes in an exposed environment.

For these demanding applications, a careful examination of RS-485 transceiver timing performance over cables is required to ensure a reliable system, as well as EMC characterization. This article introduces some key system timing and communication cable concepts; provides key performance indicators, including clock and data distribution and cable driving capability; and demonstrates benefits for industrial applications using the next-generation ADM3065E/ADM3066E RS-485 transceivers.

Timing Performance

When considering reliable data transmission at high data rates over long cable lengths, timing performance concepts, such as jitter and skew—often associated with low voltage differential signaling (LVDS)—become important for RS-485. Jitter and skew added by both the RS-485 transceiver and the system cable need to be examined.

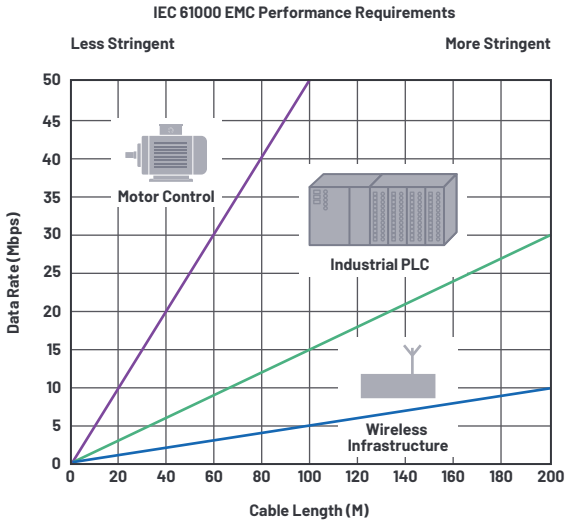

Figure 1. EMC, data rate, and cable length for RS-485.

Jitter and Skew

Jitter can be quantified as a time interval error; the difference between the expected arrival time of a signal transition and when that transition arrives in practice. Within a communication link, there are various contributors to jitter. Each contributor can be broadly described as either random or deterministic in nature. Random jitter can be identified from its Gaussian distribution and originates from thermal noise and broadband shot noise within a semiconductor. Deterministic jitter results from sources within the communication system; for example, duty cycle distortion, crosstalk, periodic external noise sources or intersymbol interference. In communications systems using the RS-485 standard, data rates are below 100 MHz, where these deterministic jitter effects dominate over random effects.

The peak-to-peak jitter value is a useful measure of the total system jitter resulting from deterministic sources. Peak-to-peak jitter can be examined in the time domain by superimposing a large number of signal transitions on the same display (commonly known as an eye diagram). This can be achieved on an oscilloscope display using infinite persistence, or with an oscilloscope's built-in jitter decomposition software, as shown in Figure 2.[2]

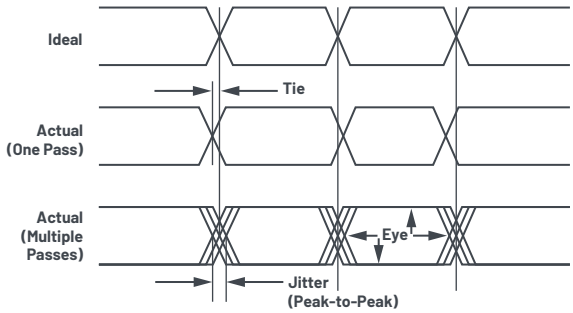

Figure 2. Time interval error, jitter, and eye.

The width of the overlaid transitions is the peak-to-peak jitter, with the open area in-between referred to as the eye. This eye is the area available for sampling by the receiving node at the far end of a long RS-485 cable. A greater eye width provides the receiving node a wider window for sampling and reduces the risk of incorrectly receiving a bit. The available eye is primarily affected by deterministic jitter contributions from both the RS-485 driver and receiver and the interconnecting cable.

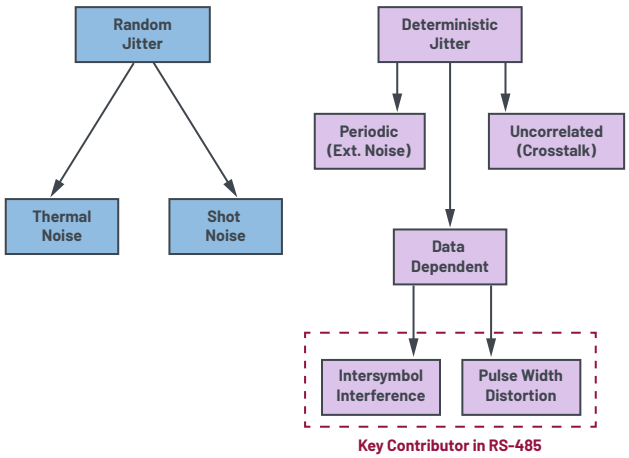

Figure 3. Key contributors to jitter in RS-485 communication networks.

Figure 3 shows the various sources of jitter in a communication network. In RS-485-based communication systems, two key contributors to timing performance are transceiver pulse skew and intersymbol interference. Pulse skew, otherwise known as pulse width distortion or duty cycle distortion, is a form of deterministic jitter introduced by the transceivers at the transmitting and receiving nodes. Pulse skew is defined as the difference in the propagation delay between the rising and falling edges of a signal. In differential communications, this skew creates an asymmetric crossover point and a mismatch between the duration of transmitted 0s and 1s. In a clock distribution system, excessive pulse skew manifests itself as a distortion in the duty cycle of the transmitted clock. In a data distribution system, this asymmetry increases the peak-to-peak jitter observed in the eye diagram. In both cases, excessive pulse skew negatively impacts the signals transmitted over RS-485 and reduces both the available sampling window and overall system performance.

Intersymbol interference (ISI) occurs when the arrival time of a signal edge is influenced by the data pattern which has proceeded that edge. Intersymbol interference effects become prominent in applications with longer cable interconnects, making ISI a key contributor in RS-485 networks. The longer interconnect creates an RC time constant where the cable capacitance has not been fully charged by the end of a single bit period. In applications where the transmitted data consists of a clock only, this form of intersymbol interference is not present. Intersymbol interference can also be caused by impedance mismatches on the cable transmission line, from line stubs or improper use of termination resistors. RS-485 transceivers with a high output drive strength generally help to minimize ISI effects as they require less time to charge the load capacitance of the RS-485 cable.

The percentage of peak-to-peak jitter tolerable is highly application dependent, and generally 10% jitter is used to benchmark the combination of RS-485 transceiver and cable performance. A combination of excessive jitter and skew affect the sampling capability of the receiving RS-485 transceiver, increasing the likelihood of communication errors. In properly terminated transmission networks, choosing a transceiver optimized to minimize transceiver pulse skew and intersymbol interference effects results in a more reliable, error-free communication link.

RS-485 Transceiver Design and Cable Effects

The TIA-485-A/EIA-485-A RS-485 standard[3] provides specifications for the design and operating range of RS-485 transmitters and receivers, including voltage output differential (VOD), short-circuit characteristics, common-mode loading, and input voltage thresholds and ranges. RS-485 timing performance, including skew and jitter, are not specified in the TIA-485-A/EIA-485-A standard, and are optimized by IC vendors with product data sheet specification.

Other standards, such as the TIA-568-B.2/EIA-568-B.2, telecommunications standard for twisted pair cabling[4] provide background for cable ac and dc effects on RS-485 signal quality. This standard provides considerations and test procedures for jitter, skew, and other timing measurements, with performance limits set; for example, the maximum allowable Category 5e cable skew is 45 ns per 100 m. Analog Devices application note AN-1399 discusses the TIA-568-B.2/EIA-568-B.2 standard in more detail and the consequences of using nonideal cabling on system performance.

While the available standards and product data sheets provide a good source of useful information, any meaningful characterization of system timing performance requires measurement of an RS-485 transceiver on a long cable.

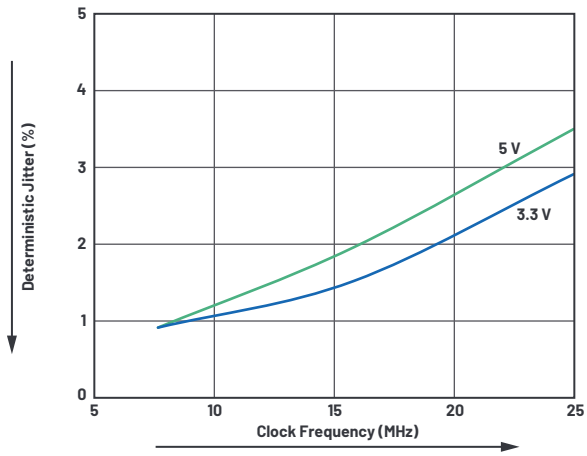

Figure 4. ADM3065E typical clock jitter performance.

Communicating Faster and Further with RS-485

The ADM3065E RS-485 transceiver features ultralow transmitter and receiver skew performance, which makes these devices ideal for transmission of a precision clock, which is often featured in motor encoding standards, such as EnDat 2.2.[5] The ADM3065E has been demonstrated to show less than 5%

deterministic jitter across typical cable lengths (Figure 4 and Figure 5) encountered in motor control applications. The wide supply range of the ADM3065E means this level of timing performance is available for applications that require either a 3.3 V or 5 V transceiver power supply.

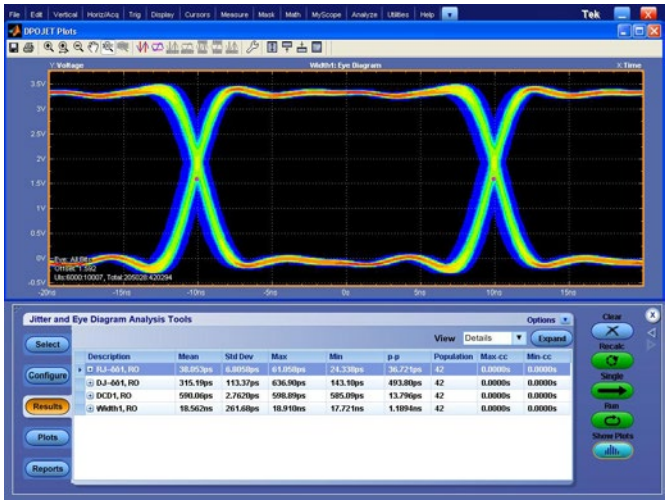

Figure 5. ADM3065E receiving eye diagram: 25 MHz clock distributed across 100 m cable.

In addition to superior clock distribution, the ADM3065E timing performance also enables reliable data distribution, with high speed outputs and minimal added jitter. Figure 6 shows that by using the ADM3065E, the timing limitations typically quoted for RS-485 data communication are greatly relaxed. Standard RS-485 transceivers are typically quoted for operation with 10% or less jitter. The ADM3065E can operate at greater than 20 Mbps on up to 100 m of cable, and still maintain just 10% jitter at the receiving node. This low level of jitter reduces the risk of incorrect sampling by the receiving data node, and results in reliability of transmission previously not possible using typical RS-485 transceivers. In applications where the receiving node can tolerate levels of jitter up to 20%, data rates of up to 35 Mbps across 100 m cable runs are achievable.

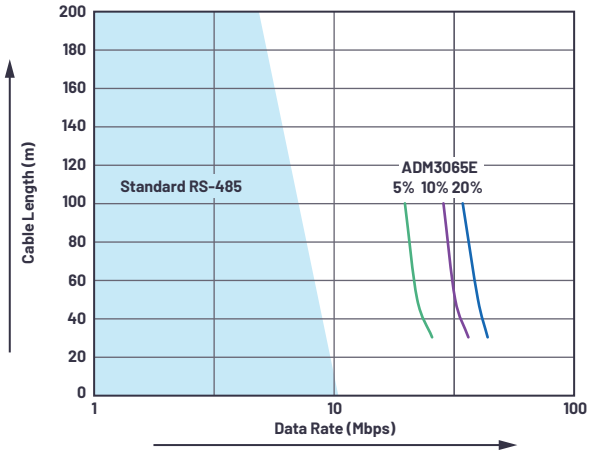

Figure 6. ADM3065E receiving data node superior jitter performance.

This timing performance makes the ADM3065E an ideal choice for the communication interface to motor control encoders. For every packet transferred using the EnDat 2.2 encoder protocol, the data is transmitted in synchronization with falling clock edges. Figure 7 illustrates that the start bit(s) begins the data transmission from the encoder back to the master controller, after the initial calculation of absolute position (T_{CAL}). The subsequent error bits (F1, F2) indicate

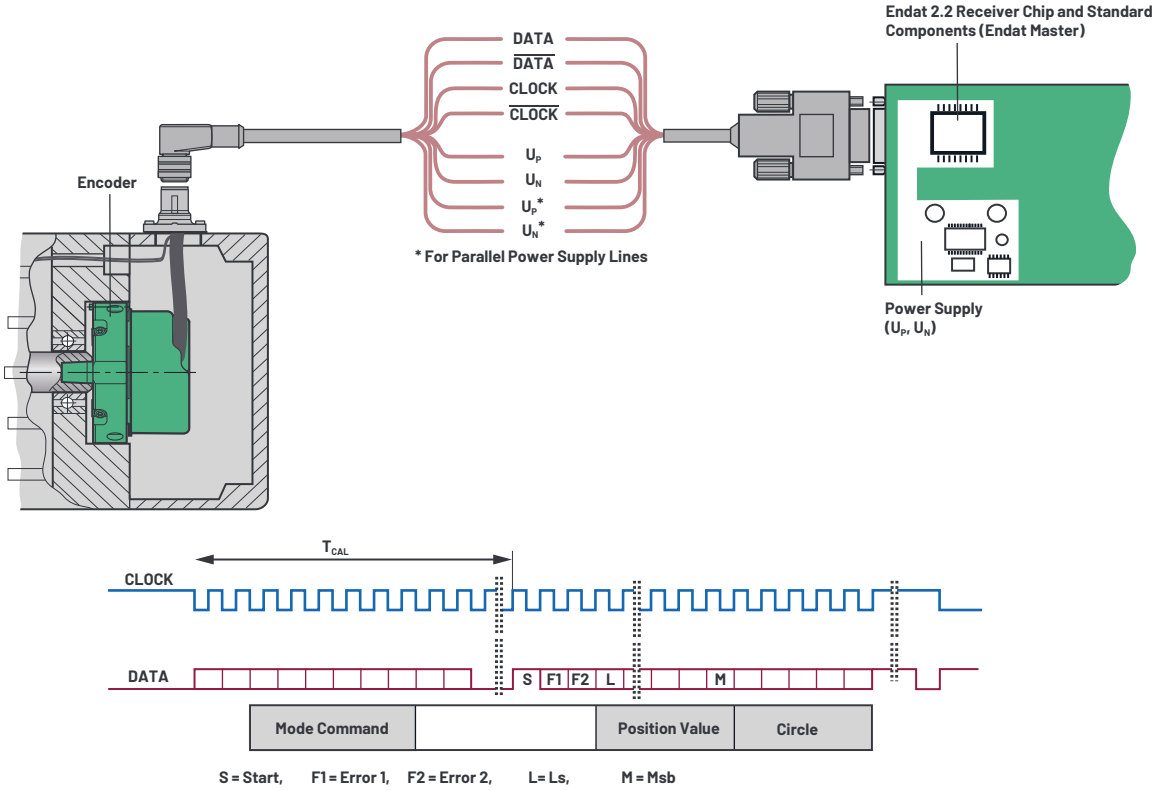

Figure 7. EnDat 2.2 physical layer and protocol with clock/data synchronization (adapted diagrams from EnDat 2.2).

when a malfunction of the encoder can result in incorrect position values. The encoder then transmits an absolute position value, starting with LS, with data following. Clock and data signal integrity is critical for successful position and error signaling over long cable runs, with EnDat 2.2 specifying a maximum 10% jitter. EnDat 2.2 specifies maximum operation at 16 MHz clock rate over 20 m of cabling. Figure 4 shows that the ADM3065E meets this requirement with only 5% clock jitter, and Figure 6 shows that the ADM3065E meets the jitter requirements for data transmission, while standard RS-485 transceivers do not.

Analog Devices' characterization of ADM3065E transceiver superior timing performance over cables ensures that system designers have the necessary information to enable a design that is successfully designed to meet the EnDat 2.2 specification.

Better Reliability over Longer Cables

The TIA-485-A/EIA-485-A RS-485 standard[3] requires compliant RS-485 drivers to generate a differential voltage amplitude, VOD, of at least 1.5 V into a fully loaded network. This 1.5 VOD allows 1.3 V of voltage dc attenuation over long cable lengths, with RS-485 receivers specified to operate with at least 200 mV of input differential voltage. The ADM3065E is designed to output a VOD of at least 2.1 V when powered at 5 V, exceeding the RS-485 specification requirements.

A fully loaded RS-485 network is equivalent to a 54 Ω differential load, which simulates a double terminated bus of two 120 Ω resistors with a further 750 Ω representing 32 connected devices of 1 unit load, or 12 kΩ. The ADM3065E features a proprietary output architecture to maximize the VOD while meeting the required common-mode voltage range, surpassing the requirements of TIA-485-A/EIA-485-A. Figure 8 illustrates that the ADM3065E exceeds the drive requirements of the RS-485 standard by >210% when powered from a 3.3 V supply rail, or by >300% when powered from a 5 V supply rail. This allows the ADM3065E family to communicate further, with more remote nodes and with more noise margin than regular RS-485 transceivers.

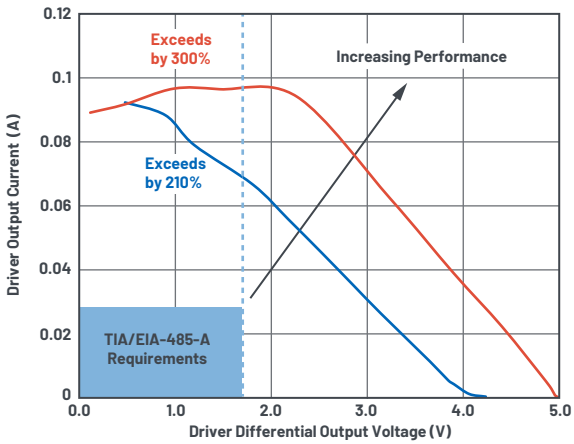

Figure 8. The ADM3065E exceeding the RS-485 drives requirements across a wide supply range.

Figure 9 further illustrates this point in a typical application over 1000 m of cable. When communicating over a standard AWG 24 cable, the ADM3065E is 30% better than a standard RS-485 transceiver—with 30% greater noise margin at the receiving node, or a 30% increase in the maximum cable length at low data rates. This performance is well suited to wireless infrastructure applications, where the RS-485 cable extends beyond several hundred meters.

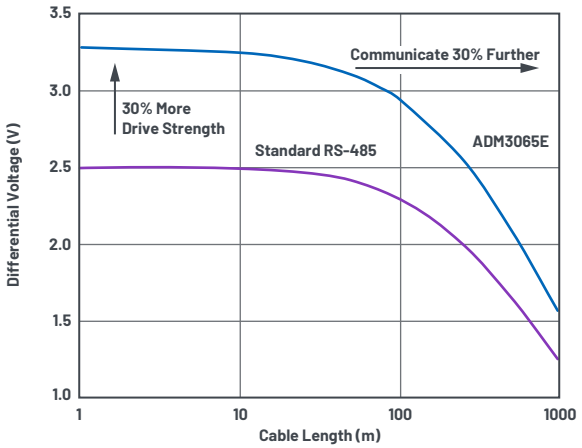

Figure 9. ADM3065E delivers a superior differential signal for ultralong distances.

EMC Protection and Noise Immunity

RS-485 signaling is balanced, differential, and inherently noise immune. System noise couples equally to each wire in an RS-485 twisted pair cable. Twisted pair cabling causes the induced noise currents to flow in opposite directions, and electromagnetic fields coupled onto the RS-485 bus cancel each other out. This reduces the electromagnetic susceptibility of the system. In addition, the enhanced ADM3065E 2.1 V drive strength allows greater signal-to-noise ratio (SNR) in communications. Over long cable runs, such as hundreds of meters between ground level and antenna on wireless base stations, having an enhanced SNR, as well as excellent signal integrity, ensures accurate and reliable tilt/position control of antennas.

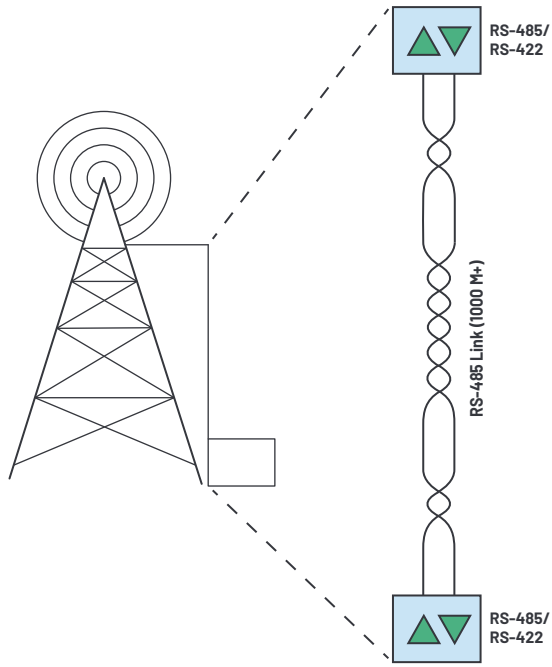

Figure 10. Wireless infrastructure cable lengths can extend over hundreds of meters.

As noted in Figure 1, EMC protection is required for RS-485 transceivers that interface directly to the outside world via adjacent connectors and cabling. For example, ESD on the exposed RS-485 connectors and cabling for the encoder to

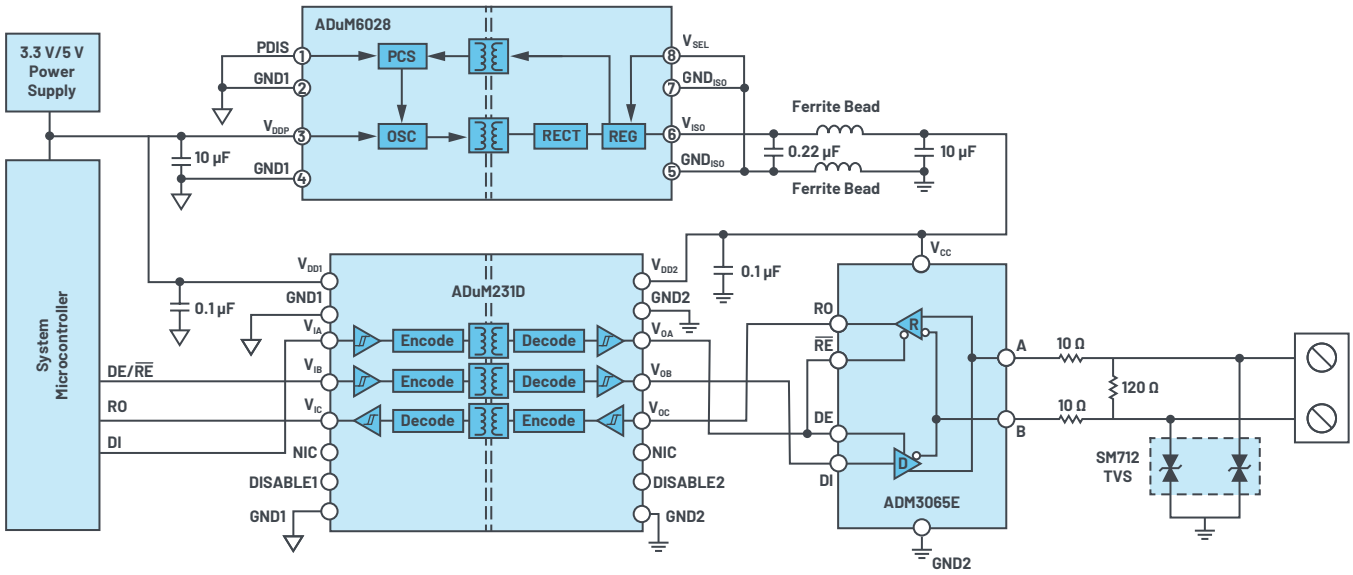

Figure 11. Complete 25 Mbps signal and power isolated RS-485 solution with ESD, EFT, and surge protection.

motor drive is a common system hazard. The system-level IEC 61800-3 standard relating to EMC immunity requirements for adjustable speed, electrical power drive systems requires a minimum ±4 kV contact/±8 kV air IEC 61000-4-2 ESD protection. The ADM3065E exceeds this requirement with ±12 kV contact/±12 kV air IEC 61000-4-2 ESD protection.

For wireless infrastructure applications, enhanced EMC protection is required to protect against damaging lightning surge events. Adding a SM712 TVS and two 10 Ω coordinating resistors to the ADM3065E inputs provides enhanced EMC protection—with up to ±30 kV 61000-4-2 ESD protection and ±1 kV IEC 61000-4-5 surge protection.

To increase noise immunity for electrically harsh motor control, process automation, and wireless infrastructure applications, one can add galvanic isolation. Galvanic isolation, with reinforced insulation and 5 kV rms transient withstand voltage, can be added to the ADM3065E using Analog Devices' *i*Coupler® and *iso*Power® technology. The ADuM231D provides the required three channels of 5 kV rms signal isolation, with precision timing performance allowing robust operation at rates up to 25 Mbps. The ADuM6028 isolated dc-to-dc converter provides the required isolated power with a withstand rating of 5 kV rms. Two ferrite beads are used to easily meet EMC compliance standards such as EN 55022 Class B/CISPR 22, resulting in a compact isolated dc-to-dc solution in 6 mm × 7.5 mm form factor.

Conclusion

Analog Device's ADM3065E RS-485 transceiver outperforms industry standards, with the possibility to communicate further and faster compared to standard RS-485 devices. At 10% jitter levels specified in EnDat 2.2[5], the ADM3065E allows the user to operate at 16 MHz clock rate over maximum 20 m of cabling, with standard RS-485 struggling to meet this requirement. The ADM3065E exceeds the RS-485 bus driving requirements by up to 300%, providing better reliability and more noise margin over longer cables. Noise immunity can be improved by adding *i*Coupler isolation, including the ADuM231D signal isolator, and the industry's smallest form factor isolated power solution, the ADuM6028.

References

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[3] "TIA/EIA-485-A, Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems." IHS Markit Inc., March 1998.

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