

C1812T474K2RAL TU

Aliases (C1812T474K2RAL7800)

SMD COTS X7R, Ceramic, 0.47 uF, 10%, 200 VDC, X7R, SMD, MLCC, COTS, Temperature Stable, Class II, 1812



Click [here](#) for the 3D model.

Dimensions

Chip Size	1812
L	4.5mm +/-0.3mm
W	3.2mm +/-0.3mm
T	1.7mm +/-0.15mm
B	0.6mm +/-0.35mm

Packaging Specifications

Packaging	T&R, 180mm, Plastic Tape
Packaging Quantity	1000

General Information

Series	SMD COTS X7R
Style	SMD Chip
Description	SMD, MLCC, COTS, Temperature Stable, Class II
Features	Temperature Stable, Class II
RoHS	No
Prop 65	⚠ WARNING: Cancer and reproductive harm - http://www.p65warnings.ca.gov .
Termination	Lead (SnPb)
Marking	No
Failure Rate	Testing per MIL-PRF-55681 PDA 8%
AEC-Q200	No
Component Weight	185 mg
Shelf Life	78 Weeks
MSL	1

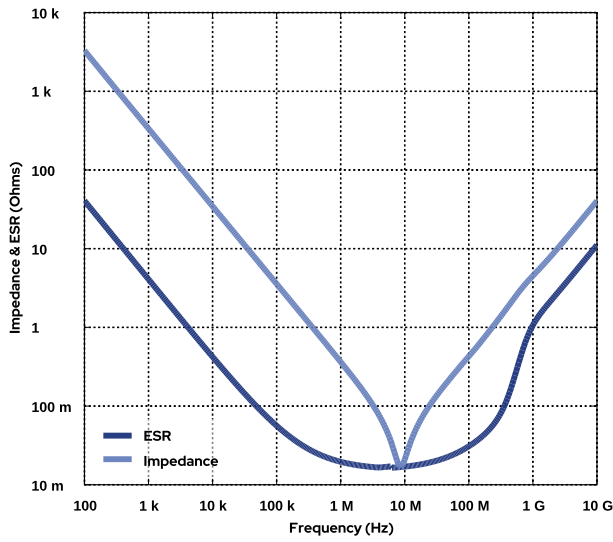
Specifications

Capacitance	0.47 uF
Measurement Condition	1 kHz 1.0Vrms
Capacitance Tolerance	10%
Voltage DC	200 VDC
Dielectric Withstanding Voltage	500 VDC
Temperature Range	-55/+125°C
Temperature Coefficient	X7R
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	15%, 1kHz 1.0Vrms
Dissipation Factor	2.5% 1kHz 1.0Vrms
Aging Rate	3% Loss/Decade Hour: Referee Time is 1000 Hours
Insulation Resistance	2.1277 GOhms

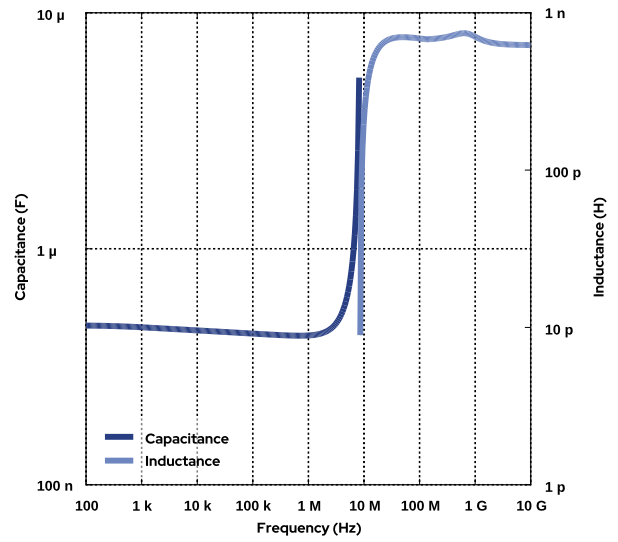
Simulations

For the complete simulation environment please visit [K-SIM](#).

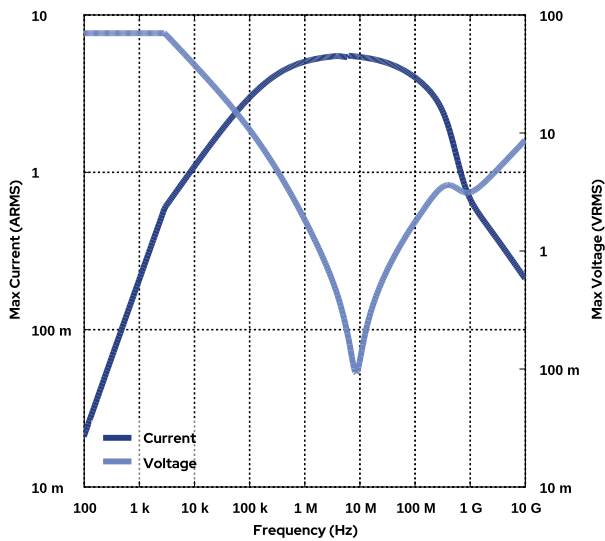
Impedance and ESR



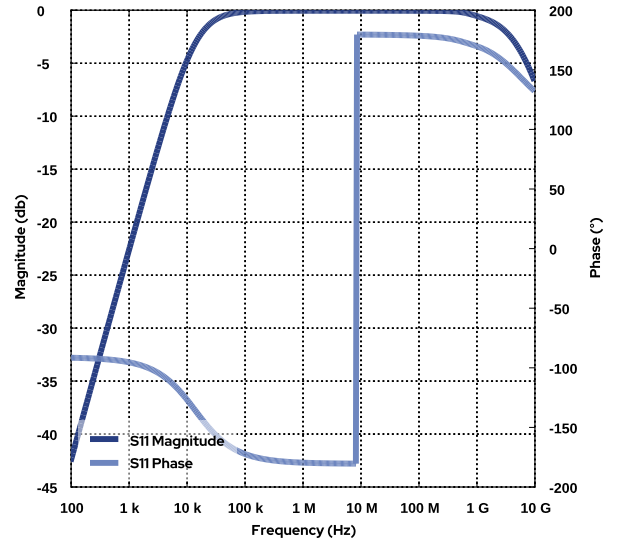
Capacitance and Inductance

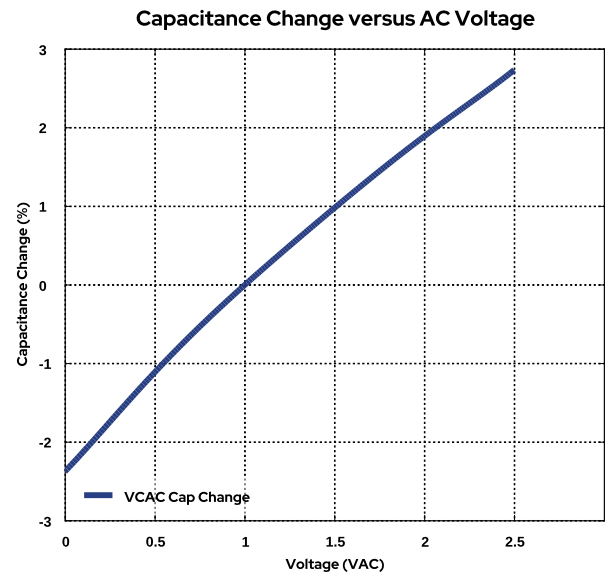
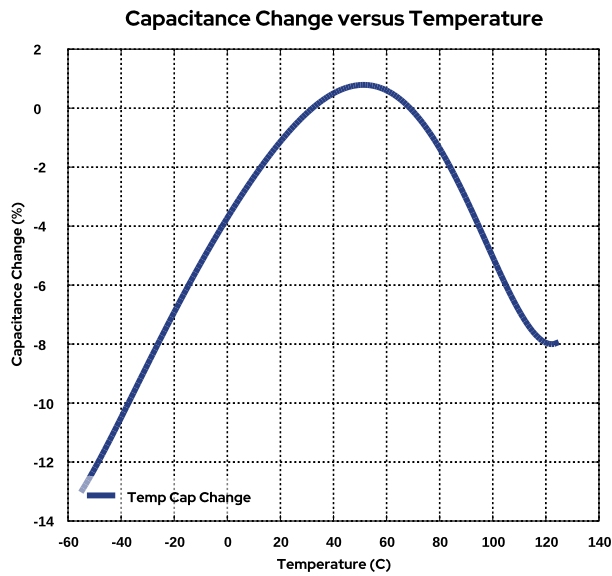
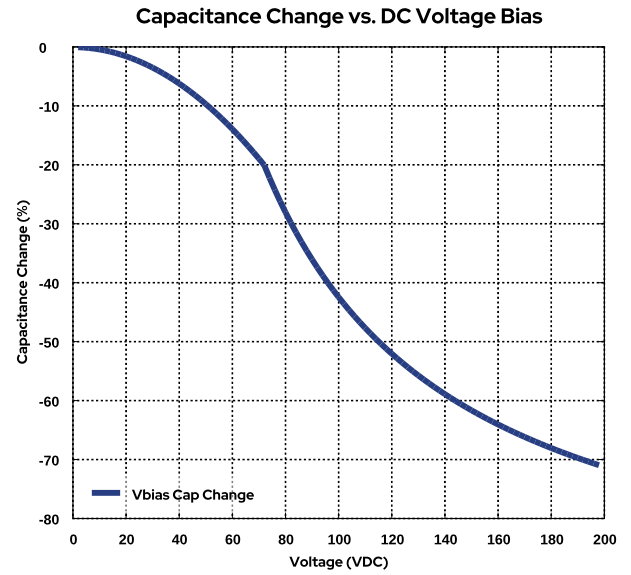
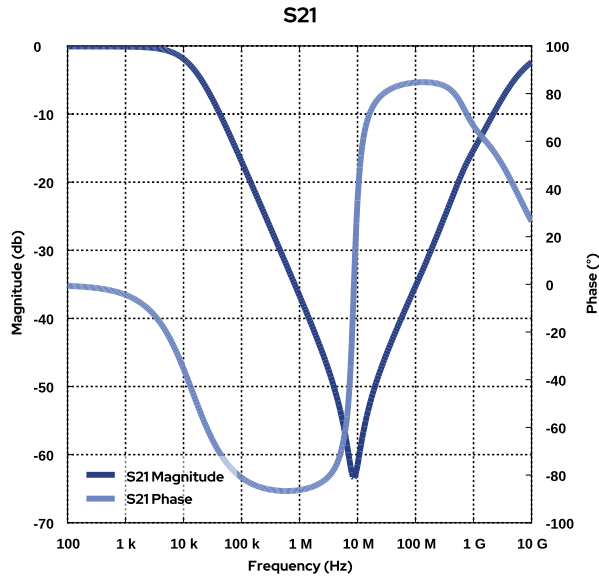


Current and Voltage



S11





These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.
- The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.