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PICOSTRAIN

Digital Amplifier for Strain Gages

PS021

Datasheet

02ND JUNE 2006

acam - solutions in time

Precision Time Interval Measurement

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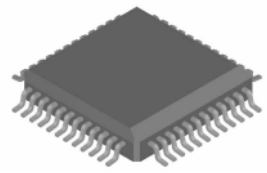
1. Introduction

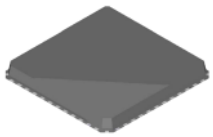
1.1 System Overview

PSØ21 is the newest front-end device out of the PICOSTRAIN® product family. PICOSTRAIN stands for a new digital concept to measure metal strain gages (SG). It is based on TDC technology (Time-to-Digital Converter). The digital measurement principle allows a high degree of flexibility. The current consumption of the total system, including the sensor, can be reduced down to less than 100 µA. The precision to be achieved is comparable to high-end 24-Bit A/D-converters and even surpasses them at high measurement rates. It has a serial interface, SPI® compatible, to communicate with a microcontroller or DSP.

The PSØ21 is downwardly compatible to the PSØ2. Hard-and software for PSØ2 can also be used with PSØ21.



TQFP 48
PSØ21



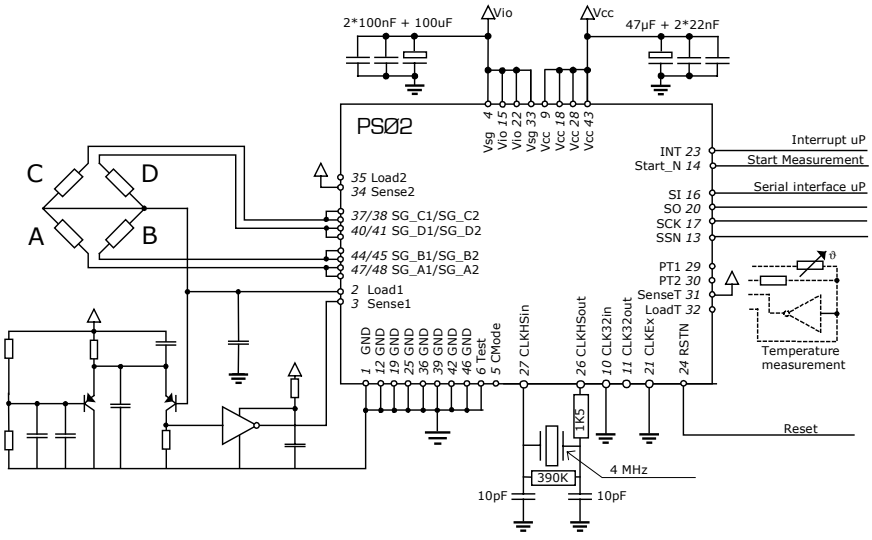
QFN7-48
PSØ21FN

Features

- Digital measuring principle in CMOS technology
- Up to 2 full- or 4 halfbridges
- Optional mode for Wheatstone bridges
- Compensated or non-compensated bridges
- Adaptation of compensation resistor's Tk by software
- Offset and span compensation internally separated (mathematically), therefore no need to trim the bridge offset
- Capable of driving only a halfbridge without any loss in precision
- Resistance strain gauge: 350 Ohm – 10 kOhm
- Programmable resolution:
  Up to 19 Bit (20nV rms or 500,000 scale div)
  @ 2 mV/V strain and 5 Hz update rate
- High Measurement rate:
  Up to 50 kHz with high resolution
  (12.4 ENOB @ 4 kHz and 2 mV/V max. strain)
- Extremely low current consumption possible: Down to 15 µA (incl. SG) at 1 Hz and 10 ENOB with 1 kOhm SG and 1000 µ strain
- High stability with temperature, low gain error (< 1 ppm/K)
- No need for a pre-amplifier
- No separate supply of SG
- No separate reference voltage
- Optional Single-conversion mode
- Separate temperature measurement
- Optional capacitor measurement
- Serial interface (SPI compatible)
- Supply voltage I/O and SG: 1.8 ... 5.5 V
- Separate Supply for interface I/Os
- Supply voltage PSØ21: 1.8 ... 3.6 V
- Op. temperature range –40°C ... +120°C
- QFN48 / QFP48 package (body size 7 x 7 mm²)

Applications

- Scales and load cells
- Force sensors
- Pressure sensors (also 4 – 20 mA)
- SG-amplifiers in general
- Solar cell driven devices
- Battery driven devices
- Wireless applications



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1.3 Structure of the datasheet

This functional description is made of several main sections for easy implementation of the PSØ21.

These main sections are:

2. Technical Characteristics

This main section is for reference with all the important technical data in a brief. Pinning, operating conditions and timings are shown. Several tables give an overview about the read and write register as well as a short description of the different bits. This section provides technical reference for the engineer actually working on the design-in of this product.

3. General Introduction

This main section is a general introduction into the field of measuring strain gauges. Some fundamental terms are introduced, which will be used frequently in this manual. We mainly explain the basics of the **PICO**STRAIN measuring principle and it's specialties.

4. Description of Basic Functions

Here the user finds everything to successfully start a first application with PSØ21. This section is important for anyone working with PSØ21 for the first time.

5. Details and Special Functions

In this section special functions and control bits are discussed. It provides information for those who want to optimize the maximum performance of the PSØ21. Things like temperature measurement and the calculation of the current consumption can be found here.

6. Special Modes

This section treats mainly measurement range 1 and capacity measurement.

7. How to get the best performance

This section gives hints what to do to get get the highest possible performance out of the PSØ21.

8. Applications

This section shows some typical application examples with schematics and configuration.

9. Background

This section gives some general background information about TDCs, strain gage measurement...

2 Characteristics and Specifications

2.1 Absolute Maximum Ratings

Supply voltage

Vcc vs. GND	-0.3 to 4	V
Vio, Vsg vs. GND	-0.3 to 7	V
Current into Output-Pin (Iout)	±30	mA
Storage temperature (Tstg)	-65 to 150	°C
Junction temperature (Tj) max.	125	°C

2.2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{cc}	Core supply voltage	$V_{io} > V_{cc}$	1.8		3.6	V
V_{io}	I/O supply voltage		1.8		5.5	V
V_{sg}	Strain gage supply voltage		1.8		5.5	V
t_{ri}	Normal Input Rising Time				50	ns
t_{fa}	Normal Input Falling Time				50	ns
t_{ri}	Schmitt Trigger Rising Time				5	ms
t_{fa}	Schmitt Trigger Falling Time				5	ms
T_a	Ambient Temperature		-40		120	°C

2.3 Electrical Characteristics

At Vcc=3.3 V ± 0.3 V, Ambient temperature –40 °C ... +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_q	Quiescent current 32 kHz	I_{cc} + I_{io}, only 32kHz oscillator running, V_{cc}=V_{io}=3V		5		µA
I_q	Quiescent current 4 Mhz	I_{cc} + I_{io}, only ClkHS running at 4MHz, V_{cc}=V_{io}=3V		150		µA
I_l	Input Leakage Current		-1		+1	µA
V_{oh}	High Level Output Voltage	I_{oh}= tbd mA V_{io}=Min.	Vio-0.4			V
V_{ol}	Low Level Output Voltage	I_{ol} = tbd mA, V_{io}=Min			0.4	V
V_{ih}	High Level Input Voltage	LVTTL Level, V_{io} = Max.	2.0			V
V_{il}	Low Level Input Voltage	LVTTL Level, V_{io} = Min.			0.8	V
V_{th}	High Level Schmitt Trigger Voltage		1.1		2.4	V
V_{tl}	Low Level Schmitt Trigger Voltage		0.6		1.8	V
V_h	Schmitt Trigger Hysteresis		0.1			V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{pu}	Pull Up Resistor	V_i=0V	20		200	kΩ
R_{pd}	Pull Down Resistor	V_i=Vcc	20		200	kΩ
C_i	Input Terminal Capacitance	f=1MHz, V_{cc}=0V			10	pF
C_o	Output Terminal Capacitance	f=1MHz, V_{cc}=0V			10	pF
C_{io}	Input/Output Terminal Cap.	f=1MHz, V_{cc}=0V			10	pF
t(POR)	Time delay Power-on Reset	From rising edge of WRN			360	ns

2.4 System Performance

At Vcc=3.3 V ± 0.3 V, Ambient temperature –40 °C ... +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INL	Integral Non-linearity strain			t.b.d.		% of FS
	Offset	Initial, uncalibrated		± 50		µV
	Offset drift	total system, 1kOhm DMS, 5V				
		Fullbridge		5		nV/K
		Halfbridge		80		nV/K
	Gain drift over -40°C ... 120°C	total system, 1kOhm DMS, 5V		1		ppm /K
PSRR1[1]	Power Supply Rejection Ratio Vio	Halfbridge[2] Vio 3 V or 5 V ±10%		120		dB
PSRR2[1]	Power Supply Rejection Ratio Vio	Fullbridge[2] Vio 3 V or 5 V ±10%		>140		dB
CMRR	Common Mode Rejection Ratio Vcc	Cannot be defined for PICOSTRAIN measuring principle		120		dB

[1] PSRR= -20*log(dVdd/dVout)

[2] Variation Vsg from 3 V to 5 V, Vcc from 2.5 V to 3.3 V

2.4.1 Measurement Capability

The following tables show the measurement capabilities for different supply voltages for the strain gage and the PSØ21 core.
All data shown include a SINC3 filter. For getting the data with fast-settle mode multiply the noise values by 1.73 or reduce the #LSB values by 0.8 Bit.
The data refer to the comparator circuit shown in Figure 21.

All measurements are done with a 1 kΩ fullbridge modified for **PICO**STRAIN.

Table 1: Measurement range 2, Vsg = 5.0 V, Vcc = 3.3 V

Measuring Rate in Hz	ENOB			No. of LSB's	Noise	
	SG Ratio	2 mV/V FS	3,3 mV/V FS	@ 2 mV/V	µV	ppm
*50.000	18,3	9,3	10,0	625	16.000	3,200
*35.000	18,4	9,4	10,1	695	14,400	2,880
*20.000	19,4	10,4	11,1	1.333	7,500	1,500
10.000	20,8	11,8	12,5	3.400	2.900	0,580
4.000	22,2	13,2	13,9	9.500	1,050	0,210
2.000	22,9	13,9	14,6	15.100	0,660	0,132
1.000	23,5	14,5	15,2	22700	0,440	0,088
500	24,0	15,0	15,7	32.700	0,305	0,061
250	24,5	15,5	16,2	47.600	0,210	0,042
100	25,3	16,3	17.0	83.000	0,120	0,024
50	25,8	16,8	17,5	117.000	0,085	0,017
20	26,5	17,5	18,2	192.000	0,055	0,010
10	27,1	18,1	18,8	277.000	0,036	0,007
5	27,5	18,5	19.2	384.000	0,028	0,005
2	28.1	19.1	19,8	555.000	0,018	0,004

SG Ratio: Resolution referred to resistance ratio of the SG
2mV/V: Resolution referred to 2mV/V maximum output (Full Scale)
3.3 mV/V: Resolution referred to 3.3mV/V maximum output (Full Scale)
***measured in measuring range 1**

Table 2: Measurement range 2, Vsg = 3.0 V, Vcc = 3.0 V

Measuring Rate in Hz	ENOB			No. of LSB's	Noise	
	SG Ratio	2 mV/V FS	3,3 mV/V FS	@ 2 mV/V	µV	ppm
*50.000						
*35.000						
*20.000						
10.000	20,5	11,5	12,2	2850	2,100	0,700
4.000	22.0	13.0	13.7	8.000	0,750	0,250
2.000	22.5	13.5	14.2	11.700	0,510	0,170
1.000	22.9	13.9	14.6	15.700	0,380	0,126
500	23.5	14.5	15,2	23.000	0,260	0,086
250	24,0	15,0	15.7	34.200	0,175	0,058
100	24.8	15.8	16.5	57.000	0,105	0,035
50	25.3	16.3	17.0	80.000	0,075	0,025
20	26.0	17.0	17.1	136.000	0,044	0,015
10	26.4	17.4	18.1	176.000	0,034	0,011
5	27.0	18.0	18.7	250.000	0,024	0,008
2	27.3	18.3	19.0	333.000	0,018	0,006

* measured in measuring range 1

Table 3: Measurement range 2, Vsg = 2.0 V, Vcc = 2.0 V

Measuring Rate in Hz	Eff. Bits			No. of LSB's	Noise	
	SG Ratio	2 mV/V FS	3,3 mV/V FS	@ 2 mV/V	µV	ppm
10.000	19,5	10,5	11,2	1.430	2,800	1,400
4.000	21,3	12,3	13,0	5.100	0,780	0,390
2.000	21.7	12.7	13.4	7.000	0,570	0,285
1.000	22.0	13.0	13.7	8.000	0,500	0,250
500	22,6	13,6	14.3	12.500	0,320	0,160
250	23.3	14.3	15.0	20.000	0,200	0,100
100	24.0	15.0	15.7	32.000	0,125	0,062
50	24.5	15.5	16.2	48.000	0,082	0,041
20	25.2	16.2	16,9	77.000	0,052	0,026
10	25.8	16.8	17.5	114.000	0,035	0,017
5	26.3	17.3	18.0	166.000	0,024	0,012
2	26.7	17.7	18.4	210.000	0,019	0,009

2.4.2 Offset and Gain Error

Figure 1: Offset drift of the complete electronics[1] in temperature range –20°C to 90°C
Vsg = Vcc = 3V, 1kOhm SG with 0 mV/V strain
Offset drift halfbridges: 55 nV/K; Offset drift fullbridge: < 2 nV/K

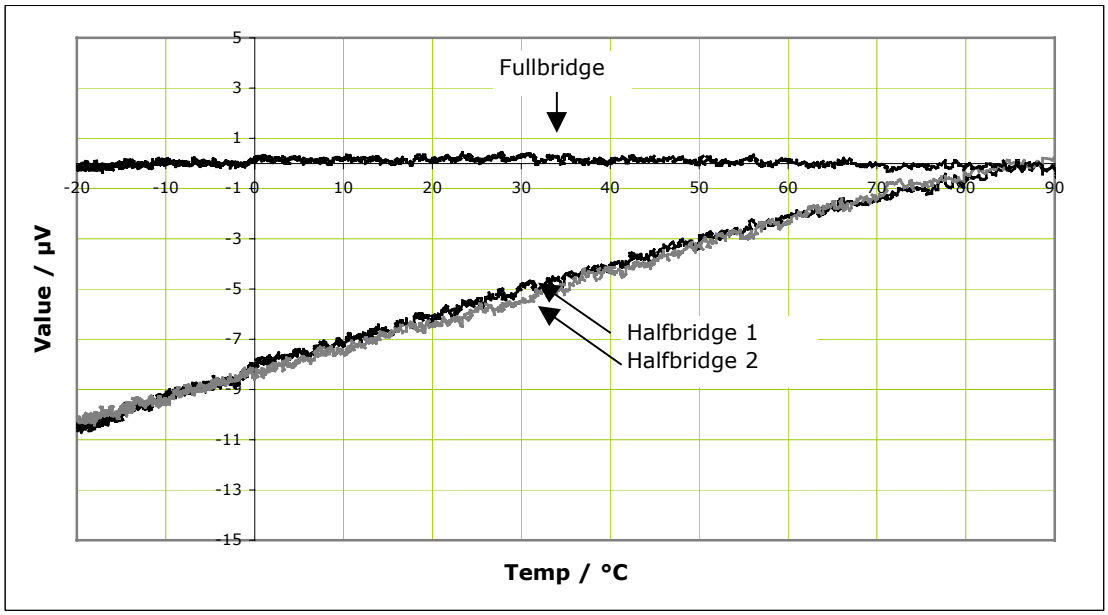
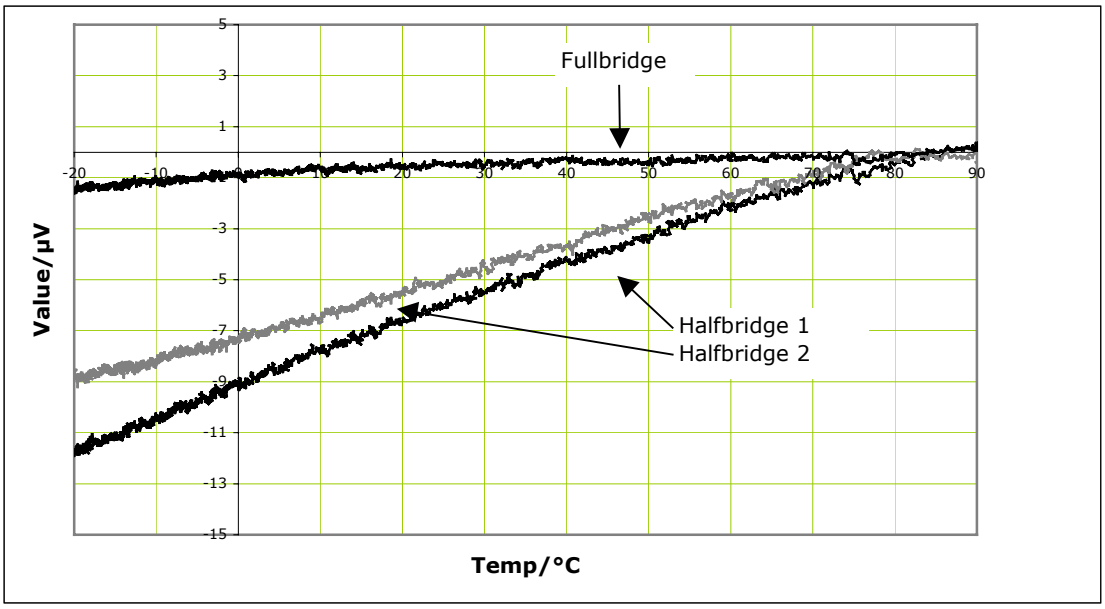


Figure 2: Gain+Offset drift complete electronics[1] in ppm of max. strain in temperature range –20°C to 90°C
Vsg = Vcc = 3V, 1kOhm SG with 2,5mV/V strain
Gain+Offset drift HB1: 1,02 ppm/K; HB2: 1,16 ppm/K; Fullbridge: < 2 nV/K



[1] measured with PSA2 evaluation board, SG temperature constant

2.4.3 Current consumption

The following graphs refer to the **total** current, which is the current into the strain gage and into PSØ21 incl. the comparator.

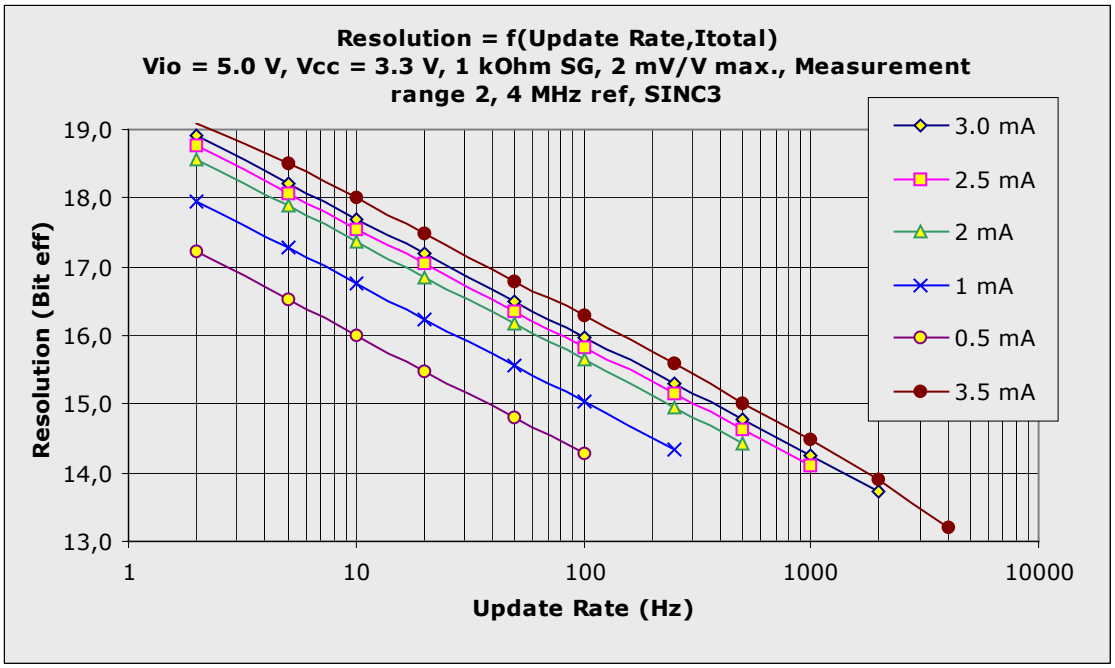


Figure 3: Vsg = 5 V (Strain gage), Vcc = 3.3V (PSØ21)

2.5 Timings

At Vcc=3.3V ± 0.3V, ambient temperature -40°C ... +85°C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
	Oscillator				
Clk32	32 kHz reference oscillator		32,768		kHz
t_{oszst}	Oscillator start-up time with ceramic resonator		150		µs
t_{oszst}	Oscillator start-up time with crystal oszillator		700		
ClkHS	High-speed reference oscillator	2	4	5	MHz
ClkEx	External high-speed reference clock input	2	4	5	MHz
	Serial interface	Max @ V_{io} =			
		1.8V	3.3V	5V Vio	
f_{clk}	Serial clock frequency	-	10	20	MHz
		Min @ V_{io} =[1]			
		1.8V	2.2V	3.0V	4.5V[2]
t_{pwh}	Serial clock, pulse width high	80	50	30	25	ns
t_{pwl}	Serial clock, pulse width low	80	50	30	25	ns
t_{sussn}	SSN enable to valid latch clock	20	10	8	7	ns
t_{pwssn}	SSN pulse width between write cycles	100	50	30	25	ns
t_{sud}	Data set-up time prior to SCLK falling	15	7	6	5	ns
t_{hd}	Data hold time before SCLK falling	10	5	4	3	ns
		Max @ V_{io} =			
		1.8V	2.5V	3.3V	5V	
t_{vd}	Data valid after SCLK rising	tbd.	40	26	18	ns

[1] Worst case at supply voltages 2.5V, 3.3V and 5V

[2] Core-Voltage Vcc=3.3V

Serial Interface (SPI compatible, Clock Phase Bit =1, Clock Polarity Bit =0)**:**

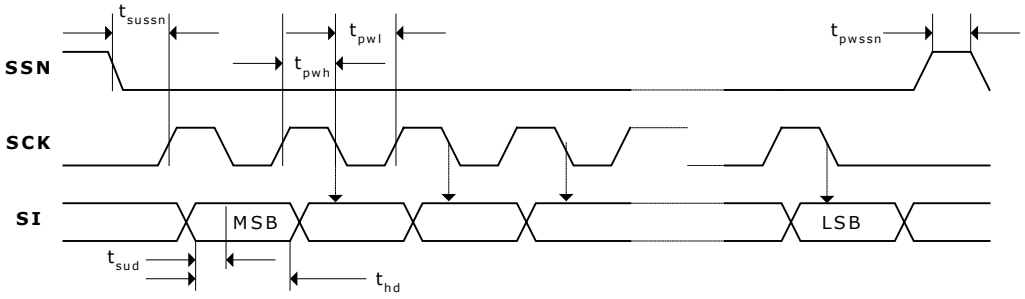


Figure 4: Write

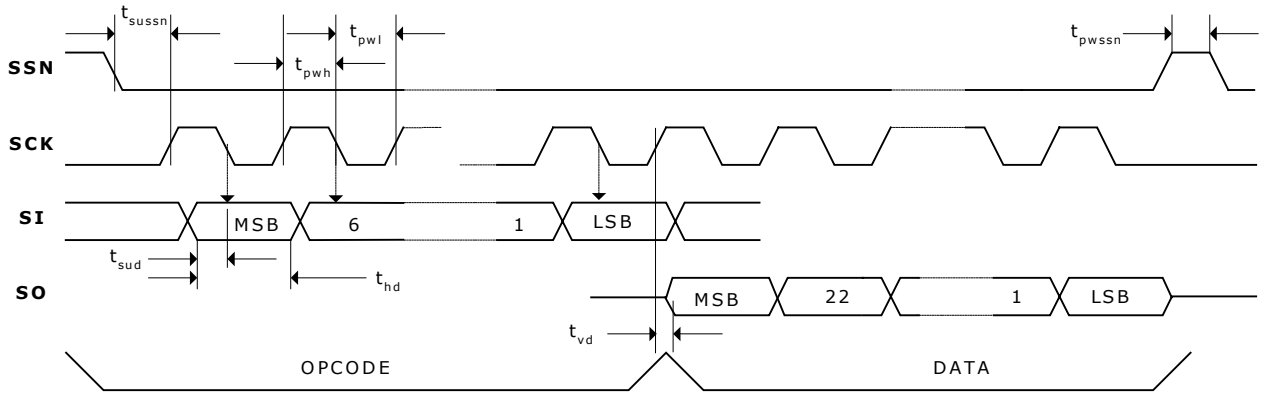


Figure 5: Read

Table 4: OP-Codes

8 Bit OP Code								
MSB							LSB	Description
1	0	0	0	ADR3	ADR2	ADR1	ADR0	Write into 24 Bit register at address
1	0	1	1	0	ADR2	ADR1	ADR0	Read 24 Bit register from address
1	0	1	1	1	ADR2	ADR1	ADR0	Read 24 Bit register from address, autoincrement address
1	1	0	0	0	0	0	0	Init
0	1	0	1	0	0	0	0	Power On Reset
0	0	0	0	0	0	0	1	Start measurement
0	0	0	0	1	0	0	0	Select Double Bridge 1
0	0	0	0	1	0	0	1	Select Double Bridge 2
0	1	1	ADR4	ADR2	ADR3	ADR1	ADR0	Write {Reg4, Reg5} to RAM address

2.6 Pin Configuration

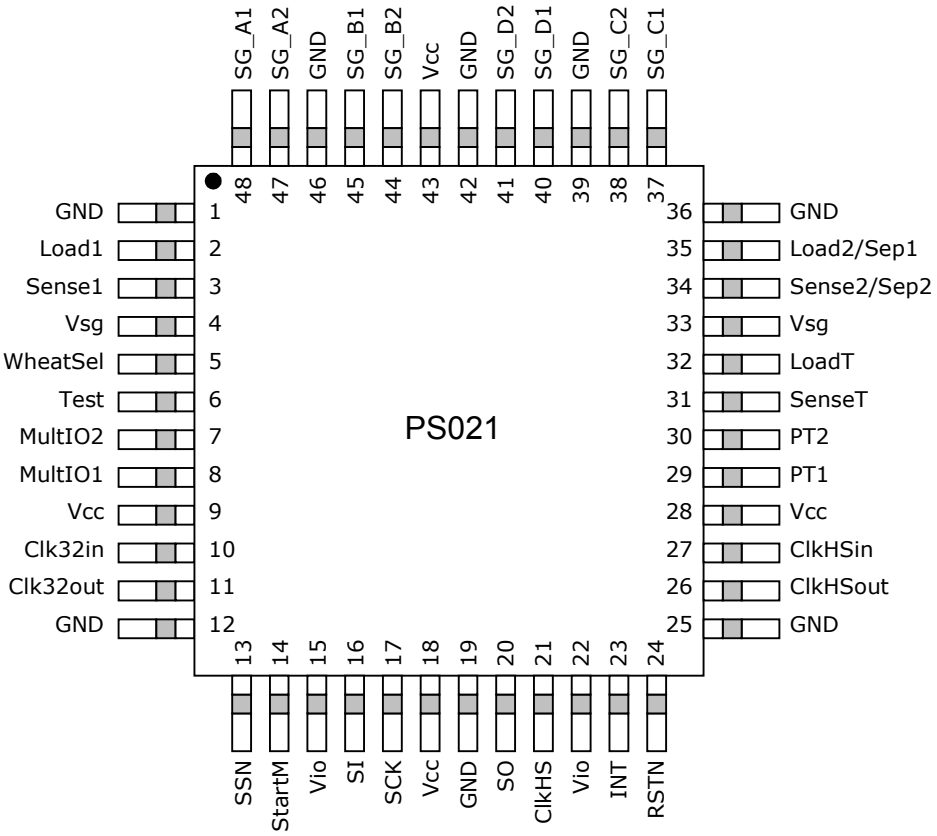


Figure 6: Pinning TQFP48 / QFN7-48

Table 5: Pin Descriptions

No.	Name	Description	Value	If not used
1	GND	Ground		
2	Load1	Load output 1		Pins 44, 48,47,48
3	Sense1	Sense input 1		GND
4	Vsg	Strain gage supply voltage		
5	WheatSel	Select for Wheatstone Mux in the comparator		n.c.
6	TestIn	Test-Pin, connect to GND		GND
7	MultIO2	Multifunctional IO		n.c.
8	MultIO1	Multi-funcional IO		n.c.
9	Vcc	Core supply voltage		
10	CLK32in	Input 32kHz clock generator		GND
11	CLK32out	Output 32kHz clock generator		n.c.
12	GND			
13	SSN	Slave Select	Low active	GND
14	StartM	Start new measurement	High active	GND
15	Vio	I/O supply voltage		
16	SI	Input serial interface		

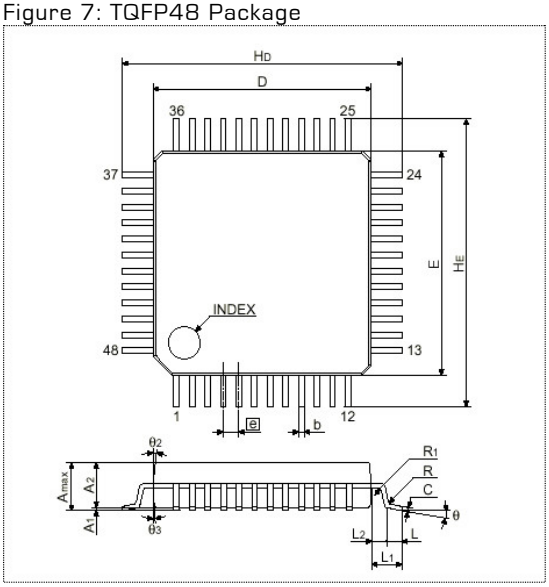
17	SCK	Clock serial interface		
18	Vcc	Core supply voltage		
19	GND			
20	SO	Output serial interface		
21	ClkEx	Input external high-speed reference clock		GND
22	Vio	I/O supply voltage		
23	INTN	Interrupt Flag	LOW active	n.c.
24	RSTN	Reset input	LOW active	Vio
25	GND			
26	ClkHSout	Output high-speed clock generator		n.c.
27	ClkHSin	Input high-speed clock generator		GND
28	Vcc	Core supply voltage		
29	PT1	Port 1 temperature measurement		Pin 32
30	PT2	Port 2 temperature measurement		Pin 32
31	SenseT	Sense input temperature measurement		GND
32	LoadT	Load output temperature measurement		Pins 29, 30
33	Vsg	Strain gage supply voltage		
34	Sense2 Sep1	Sense input 2 Separate compensation		Vsg
35	Load2 Sep2	Load output 2 Separate compensation	one-sense mode: halfbridge:	n.c. Pins 37, 38,40,41
36	GND			
37	SG_C1	Port 1 halfbridge C		Pin 35
38	SG_C2	Port 2 halfbridge C		Pin 35
39	GND			
40	SG_D1	Port 1 halfbridge D		Pin 35
41	SG_D2	Port 2 halfbridge D		Pin 35
42	GND			
43	Vcc	Core supply voltage		
44	SG_B2	Port 2 halfbridge B		Pin 2
45	SG_B1	Port 1 halfbridge B		Pin 2
46	GND			
47	SG_A2	Port 2 halfbridge A		Pin 2
48	SG_A1	Port 1 halfbridge A		Pin 2

2.7 Package Drawings

Table 6: Dimensions TQFP48 package

Symbol	Dimension in Millimeters			Dimension in Inches (*)		
	Min.	Nom.		Max.	Min.	Nom.
E	6,9	7		7,1	(0,272)	(0,276)
D	6,9	7		7,1	(0,272)	(0,276)
A				1,7		
A1		0,1				(0,004)
A2	1,3	1,4		1,5	(0,052)	(0,055)
e		0,5				(0,020)
b	0,13	0,18		0,28	(0,006)	(0,007)
C	0,1	0,125		0,175	(0,004)	(0,005)
θ	0°			10°	(0°)	
L	0,3	0,5		0,7	(0,012)	(0,020)
L1		1				(0,039)
L2		0,5				(0,020)
HE	8,6	9		9,4	(0,339)	(0,354)
HD	8,6	9		9,4	(0,339)	(0,354)
θ2		7°				(7°)
θ3		4°				(4°)
R		0,2				(0,008)
R1		0,2				(0,008)

Figure 7: TQFP48 Package

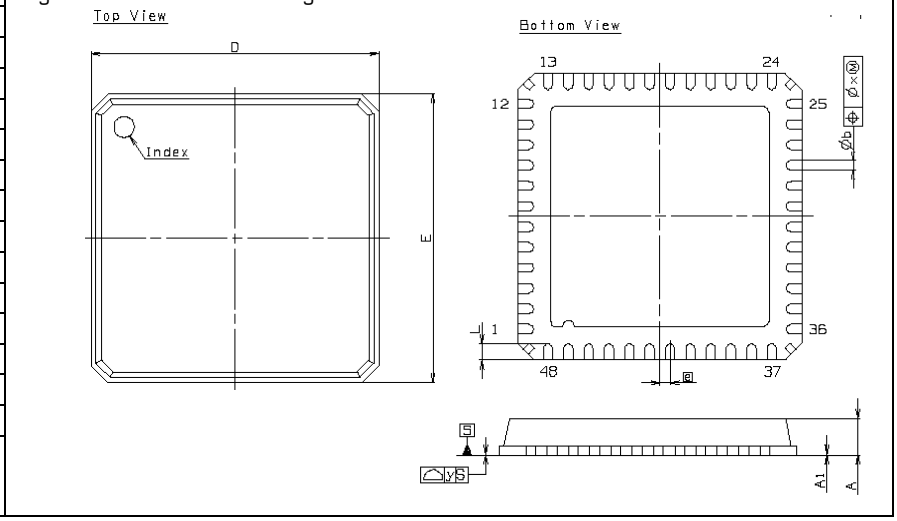


* for reference

Table 7: Dimensions QFN7-48 package

Symbol	Dimension in Millimeters		
	Min.	Nom.	
E		7	
D		7	
A			1.00
A1			0.05
e		0,5	
b	0.18		0.30
L	0.30		0.50
x			0.10
y			0.08

Figure 8: QFN7-48 Package

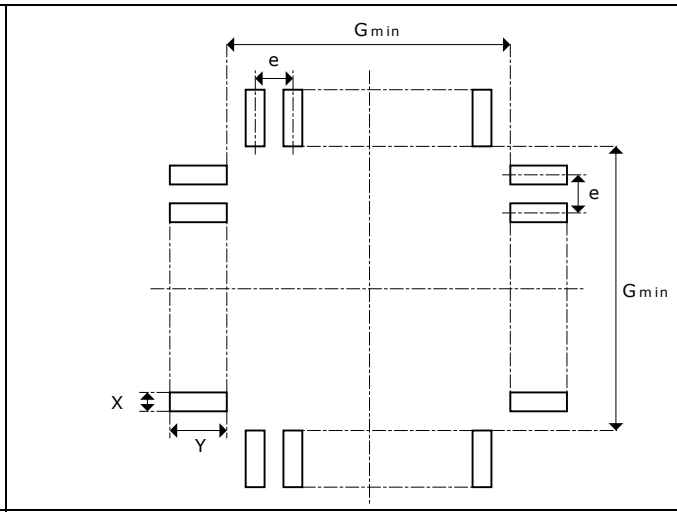


Recommended Foot Pattern

TQFP48

e = 0,5 mm
G_{min} = 7,4 mm
0,2 mm < X < 0,25 mm
Y ≥ 1 mm (2 mm recommended)

Recommended sockets for testing:
Yamaichi IC51-0484-806
Seiko IC51-806.KS11882



QFN7-48

e = 0,5 mm
G_{min} = 5,93 mm
Zmax = 7,31 mm
D2' < 5,63 mm
CPL = mm
CII = mm
Amax = 5,78 mm
X = 0,28 mm
Y = 0,69 mm

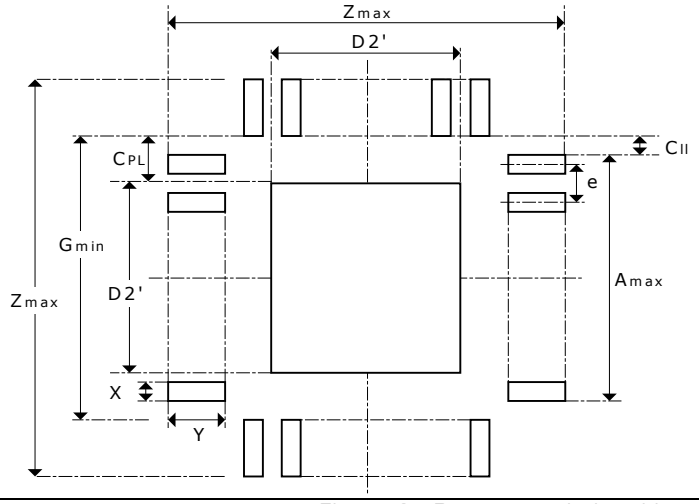


Figure 9: Recommended pad layout

2.8 Registers

2.8.1 Write Registers

Table 8 Write registers (Default values in second row)

Bit	Reg 0		Reg 1		Reg 2		Reg 3		Reg 4		Reg 5		Reg 6		Reg 7	
23	CalAvRate	1	CycleTime	0	RdsonModify	0	Mult1	x	RD1	1	RD2	1	s.c.	0	RunCont	0
22		0		0		1		x		0		0	s.c.	1	Rdson Filter	0
21	RdsonSimple	0		0		0		x		0		0	s.c.	0	s.c.	0
20	ClkHSDiv	0		0		0		x		0		0	s.c.	1	ClkHSring	0
19		0		0	RdsonAvRate	1		x		0		0	s.c.	0	ClkHSon	0
18	Cmeasure	0		0		0		x		0		0	s.c.	0		1
17	MultEN	0		0		0		x		0		0	s.c.	0	s.c.	0
16	SelClk32	1		0		0		x		0		0	Noise1	0	s.c.	0
15	SubFB	0		0	GainAvRate	0		x		0		0	CalDel	0	n.c.	
14	SumFB	0		0		1		x		0		0		1	s.c.	0
13	NegSense2	0		0		0		x		0		0		0	s.c.	0
12	NegSense1	0		1		0		x		0		0		0	s.c.	0
11	NegSenseT	1	AvRate	0	GainCorRate	0		x		0		0	s.c.	0	s.c.	0
10	TempRate	0		0		0		x		0		0	s.c.	1	s.c.	0
9		0		0		0		x		0		0	s.c.	0	s.c.	0
8	DoubleBr	0		0		1		x		0		0	s.c.	1	s.c.	0
7	SubOffset	0		0	PortFilter	0		x		0		0	n.c.		s.c.	0
6	Sinc3	0		0	OffsetAvRate	0		x		0		0	s.c.	0	s.c.	0
5	SingleCon	0		1		1		x		0		0	s.c.	0	s.c.	1
4	HighRes	1		0		0		x		0		0	WarmUp	1	s.c.	1
3	Mrange2	1		0	CalCycle	0		x		0		0		0	s.c.	0
2	HighSpeed	0		0		0		x		0		0		0	s.c.	1
1	Bridge	0		0		1		x		0		0	MFake	0	s.c.	0
0		0		0		0		x		0		0		0	s.c.	1

s.c. = Special acam configuration bits, n.c. = not in use

Bit	Reg 8		Reg 9		Reg 10		Reg 11		Reg 12		Reg 13		Reg 14		Reg 15	
23	SignTG2	0	s.c.	0	SignMult2	0		x		x		x		x		x
22	SignTG1	0	s.c.	0	SignMult1	0		x		x		x		x		x
21	CompSleep	0	s.c.	0	PSØ21_Adj1	0		x		x		x		x		x
20	CompConOn	0	s.c.	0	PSØ21_Adj1	1		x		x		x		x		x
19	CompCon	0	s.c.	0	PSØ21_Adj1	0		x		x		x		x		x
18		0	s.c.	1	PSØ21_Adj1	0		x		x		x		x		x
17		0	s.c.	1	PSØ21_Adj1	0		x		x		x		x		x
16		0	s.c.	0	PSØ21_Adj1	1		x		x		x		x		x
15	PortSw4	1	n.c.	0	Quarterbridge	0		x		x		x		x		x
14		1	n.c.	0	Cal_Adjust	0		x		x		x		x		x
13	PortSw3	1	Cmeas2	0	Cal_Adjust	0		x		x		x		x		x
12		0		0	Cal_Adjust	0	Mult2	x	TKOffs1	x	TKOffs2	x	TKGain1	x	TKGain2	x
11	PortSw2	0	AvRate2	0	Cal_Adjust	0		x		x		x		x		x
10		1		0	Cal_Adjust	0		x		x		x		x		x
9	PortSw1	0		0	Cal_Adjust	0		x		x		x		x		x
8		0		0	Cal_Adjust	0		x		x		x		x		x
7	SpreadRng	0		0	ModSpanByT	0		x		x		x		x		x
6		0		0	ModRSpan	0		x		x		x		x		x
5	SpreadSrc	0		0	LoadStartDel	0		x		x		x		x		x
4		0		0	LoadStart	0		x		x		x		x		x
3	SpreadEN	0		0	PSØ21_Adj2	0		x		x		x		x		x
2	WheatEN	0		0	PSØ21_Adj2	0		x		x		x		x		x
1	SepGain	0		0	PSØ21_Adj2	0		x		x		x		x		x
0	Mult2En	0		0	PSØ21_Adj2	0		x		x		x		x		x

Note:
Registers Mult1, Mult2, TKOffs1, TKOffs2, TKGain1 and TKGain2 are not initialized when a INIT or Power-on reset is done. It is mandatory to write the correct values into these registers before switching on multiplication.

Table 9: Short description of the Bits:

Name	Description	Values
Reg 0		
Bridge <1,0>:	Select bridge mode: One-sense or Alternating mode Halfbridge or fullbridge	[0,0] = Fullbridge, One-sense mode [1,1] = Fullbridge, alt. mode [0,1] = Bridge0 (Ports A, B) [1,0] = Bridge1 (Ports C, D)
HighSpeed:	Select frequency mode in measurement range 1	0 = 32 kHz Clock 1 = ClkHS
Mrange2	Switch PSØ21 to measurement range 2	0 = measurement range 1 1 = measurement range 2
HighRes	Select High-Resolution mode of the TDC time measuring unit	0 = without HighRes 1 = with HighRes
SingleCon	Single-conversion mode	1 = Single-conversion on

Sinc3	Switch-on SINC3 filter	0 = Fast settle 1 = SINC3-Filter on
SubOffset	Select Auto-offset calculation	1 = with Auto-offset
DoubleBr	Switch to doublebridge mode	
TempRate	Controls temperature measurement	0 = off 1 = each AVRate 2 = each 6th AVRate 3 = each 9th AVRate
NegSenseT	Negation SenseT input	0 = falling edge
NegSense1	Negation Sense1 input	0 = falling edge
NegSense2	Negation Sense2 input	0 = falling edge
SumFB	Select summation in fullbridge mode	HB1 + HB2
SubFB	Select difference in fullbridge mode	HB2 – HB1
SelClk32	Use 32 kHz clock as cycle clock	1 = on, MRange 1 only
MultEN	Switch-on multiplication	1 = on
Cmeasure	Switch-on capacity measurement	1 = on
ClkHSDiv	Sets predivider for CLKHS Mrange2: TDC range = max. discharge time = $Tref * 2^{ClkHSDiv} * 2^{8}$ ClkHSDiv = 1 is recommended	0 = divided by 1 1 = divided by 2 2 = divided by 4 3 = divided by 8
RdsonSimple	Enable simplified Rdson correction	1 =on
CalAvRate	Sets the averaging rate of the calibration value in measurement range 2	0 = 1 1 = 8 2 = 32 3 = 64

Reg 1		
AVRate	Averaging rate for a single measurement	1 ... 4095
CycleTime	Cycle time in multiples of the reference clock for the cycle time	1 ... 4095

Reg 2		
CalCycle	Sets the number of cycles before the TDC does a calibration measurement	1 = each cycle 2 = each 2nd ... 15 = each 15th
OffsetAVRate	Averaging rate of Auto-offset measurements	1 = 1 2 = 2 3 = 4 ... 7 = 128
PortFilter	Additional Filter	1 = on (is recommended)
GainCorRate	Sets the repetition rate of gain compensation measurements in multiples of AVRate	0 = off (no gain compensation) 1 = each AVRate 2 = each 2nd ... 15 = each 15th
GainAVRate	Averaging rate of gain compensation	1 = 1 2 = 2 3 = 4 ... 15 = 16284

RdsonAVRate	Averaging rate Rdson compensation	1=1 2=2 3=4 ... 15=16284
RdsonModify	Modification of Rdson calculation after an INIT	Use default value

Reg 3		
Mult1	Multiplication factor, fixed-point number with 8 integer and 16 fractional digits	Mult1 = Register3/2^{16} = 0 ... 255.9999

Reg 4		
RD1	Write-back register Rdson halfbridge1	Use default value 0x800000

Reg 5		
RD2	Write-back register Rdson halfbridge2	Use default value 0x800000

Reg 6		
Mfake	Number of dummy cycles at the beginning of an AVRate measurement	0 = 0 1 = 1 2 = 2 3 = 4
WarmUp	Number of dummy cycles after an INIT	0 = off 1 = 16 2 = 32 3 = 64 ... 7 = 1024
CalDel	Controls point in time of calibration in multiples of the ClkHS/ClkEx period after start of capacitor discharge	CalDel: 0, 1, 2, ..., 15 # of periods: don't use, 4, 5, ..., 18
Noise1	Modifies the internal noise generator	0 = on

Reg 7		
ClkHSon	Switch-on high-speed oscillator	0 = Oscillator off 1 = Oscillator on 2 = settling time = 640 µs 3 = settling time = 1280 µs
ClkHSring	Switch-on internal ring-oscillator	1 = ring oscillator on
RdsonFilter	Switch-on spike filter for Rdson compensation	1 = Filter on
RunCont	Runtime of internal ring-oscillator	0 = if required 1 = continuously

Reg 8		
Mult2EN	Enable 2nd multiplication factor for 2nd halfbridge or 2nd fullbridge	1 = on

SepGain	Switch to separate gain compensation resistors	1 = on, mandatory in Wheatstone mode
WheatEN	Switch to Wheatstone mode	1 = on
SpreadEN	Enable adding noise to the cycle time	1 = on
SpreadSrc	Select source of noise generator	0 = each cycle 1 = each 8th cycle 2 = each interrupt 2 = interrupt
SpreadRng	Sets the range of the cycle time noise	0 = 0 cycle 1 = add noise to 4 cycles 2 = add noise to 8 cycles 3 = add noise to 16 cycles
PortSw1	Free assignment ports to pins 48,47	00 = SG_A1,SG_A2 01 = SG_B1,SG_B2 10 = SG_C1,SG_C2 11 = SG_D1,SG_D2
PortSw2	Free assignment ports to pins 45,44	
PortSw3	Free assignment ports to pins 41,40	
PortSw4	Free assignment ports to pins 37,38	
CompCon	Comparator control bits	
CompConOn	Selects 'switched Comparator'	1 = on
CompSleep	Sets external comparator to sleep mode	1 = on
SignTG1, SignTG2	Sign of correction for span compensation resistors	

Reg 9		
AvRate2	Averaging rate for the 2nd bridge in doublebridge mode	0 = off, 2nd bridge uses AvRate
Cmeas2	Switch for capacity measurement with external multiplexer	0 = off 1 = on without compensation 2 = on with compensation, analog Mux with enable 3 = on with compensation, 2 single analog switches

Reg 10		
LoadStart	Start measurement through load pin (not the port pins)	1 = on (recommended)
LoadStartDel	Sets delay with LoadStart	0 = about 25 ns typ. 1 = about 140ns Typ.
ModRSpan	Software adaptation of the bridges Span resistor Rspan	1 = on, recommended for bridges with Rspan
ModSpanByT	Replace Rspan with temperature measurement value	1 = on
SignMult2, SignMult1	Signs for the multiplication factors	0 = positive 1 = negative

Reg 11		
Mult2	Multiplication factor, fixed-point number with 8 integer and 16 fractional digits	Mult1 = Register3/2^{16} = 0 ... 255.9999

Reg 12		
TkOffs1	Offset factor for 1st fullbridge in ppm	16 Bit integer, 8 Bit fractional

Reg 13		
TkOffs2	Offset factor for 2nd fullbridge in ppm	16 Bit integer, 8 Bit fractional

Reg 14		
TkGain1	Multiplication factor Rspan 1st fullbridge	8 Bit integer, 16 Bit fractional

Reg 15		
TkGain2	Multiplication factor Rspan 2nd fullbridge	8 Bit integer, 16 Bit fractional

2.8.2 Read Registers / Ouput Data Formats

Table 10: Read Registers

ADR	Symbol	Bits	Description								
0	HB1	24	Result halfbridge 1, fixed-point no. with 16 integer digits, 8 fractional digits								
1	HB2	24	Result halfbridge 2, fixed-point no. with 16 integer digits, 8 fractional digits								
2	STAT/ TMP	24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Bit 15...0
			Double Bridge	TMP	Error PLL1	Error PLL2	Error DSP	Timeout TMP	Timeout HB2	Timeout HB1	Temperature result
3	REG 0	24	Content of write register 0, to be used for testing the communication								
4	TDC1	24	TDC result								
5	TDC2	24	TDC CAL value in measuring range 2								
6	RD1	24	Rdson configuration value to be written into register 4								
7	RD2	24	Rdson configuration value to be written into register 5								

- **Result registers HB1 and HB2**
  The contents of registers HB1 and HB2 depend on the operating mode:

a. Without Doublebridge

Table 11:

Bridge[1:0]	SumFB	SubFB	Content HB1	Content HB2
0 or 3	0	0	HB1	HB2
1	0	0	HB1	-----
2	0	0	-----	HB2
0 or 3	1	0	-----	HB1 + HB2
0 or 3	0	1	-----	HB2 – HB1

b. With Doublebridge

Table 12:

Bridge[1:0]	SumFB	SubFB	DBStat	Content HB1	Content 2
0 or 3	0	0	0	HB1 of FB1	HB2 of FB1
1	0	0	X	HB1 of FB1	HB2 of FB1
2	0	0	X	HB1 of FB2	HB2 of FB2
0 or 3	1	0	0	-----	(HB1 + HB2) of FB1
0 or 3	0	1	0	-----	(HB2 - HB1) of FB1
0 or 3	0	0	1	-----	HB2 of FB2
0 or 3	1	0	1	-----	(HB1 + HB2) of FB2
0 or 3	0	1	1	-----	(HB2 - HB1) of FB2

The data have the format of a fixed-point number with 16 integer and 8 fractional digits:

Table 13: Data format

23 … 8	7 … 0	$HB1 = Mult \times \frac{\Delta R}{R} \times 10^6 = Register1 \div 256$
HB1 etc.		
16 Bit integer	8 Bit fractional	

- **Content Register STAT (Status register):**

DBStat	Shows in Double-bridge mode the no. of the bridge actually measured
TMP	Temperature value is valid
HB2	Value of 2nd halfbridge is valid
HB1	Value of first halfbridge is valid
Error DSP	TDC and DSP collided during RAM access. Increase MFake or use Single conversion
TimoHB1	There was a time-out during the last measurement of halfbridge 1
TimoHB2	There was a time-out during the last measurement of halfbridge 2
TimoTMP	There was a time-out during the last measurement of temperature

- **Register Reg 0**

This register is the mirror image of write register 0. It can be used for testing the communication by the SPI interface.

- **Register TDC1**

This register represent the result of the time measurement and therefore of the discharge time.

Measurement range 2:
The time interval is given in multiples of the reference clock.

Table 14: Data format

23 … 0		τ = TDC1 x Tref x 2^ClkHSDiv = register4/65536 x Tref x 2^ClkHSDiv
TDC1		
8 Bit integer	16 Bit fractional	

The TDC1 value is given as fixed-point number with 8 integer and 16 fractional digits, therefore the 24 Bit integer register content must be divided by 2^{16}.

Measurement range 1:
The time interval is given in multiples of the TDC resolution (LSB).

Table 15: Data format

23 … 0	$\tau \approx$ TDC1 * 30 ps (Normal resolution) $\tau \approx$ TDC1 * 15 ps (High resolution)
TDC1	

The resolution of the TDC depends on temperature and supply voltage. The values given are only typical ones at 5 V and 25°C Tamb.

- **Register TDC2**

In measurement range 2 this register gives the period of the calibration clock in 8-fold multiples of the resolution. As the period is known, e.g. 250 ns with a 4 MHz clock, the resolution of the internal TDC can be calculated:

$$\text{resolution} = \frac{T_{ref} * 2^{ClkHSDiv}}{TDC2 * 8}$$

Table 16: Data format

23 … 0	τ ≈ TDC2 * 8 * 30 ps (Normal resolution)
TDC2	τ ≈ TDC2 * 8 * 15 ps (High resolution)

- **Register RD1 and RD2**
  These registers can be used to optimize the settling behavior of the Rdson compensation. It is possible to read these data after a measurement and to write them back into registers RD1 and RD2 with the next configuration of the PSØ21.

2.9 Recommended Modifications to the Default Values

It is possible to have good measuring results already with the default settings. We recommend the following modifications to the default settings to get the best possible measurement quality.

Register Name	Bits	Default	Recommended value
PSØ21_Adjust1	Reg10, Bits 16-21	'dec17	'dec17; 'dec29; 'dec45 ***
Cal_Adjust	Reg10, Bits 8-14	'dec0	'dec63

*** 'dec 17 (default) is generally recommended and shows good results in all operating modes. In the two following exceptional cases modifications might improve the results:

a. At high AVRate (>20) 'dec45 might give better results. At AVRAten < 20 'dec45 should not be used.
b. At high AVRate (>20) and low Vcc-Core (<2.5V) it is better to use 'dec29 instead of 'dec45.

3. General Introduction

3.1 Measuring Task

Metal strain gauges (SG) change their value with mechanical deformation, especially a variation in length. The strain ε designates the relative variation in length of the strain gauge:

$$\text{Strain}(\varepsilon) = \frac{\Delta L}{L} \qquad (1).$$

Common strain gauges have a maximum strain of typical

$$\varepsilon_{max} = 1000\ \mu\ (1000 \times 10^{-6} \text{ or } 0.1\ \%).$$

The ratio of the resistance variation to the length variation is designated K-factor or strain gain.

$$\frac{\Delta R}{R} = K \times \frac{\Delta L}{L} \qquad (2).$$

For metal strain gauges the K-factor is typically of value 2. The maxim variation of the SG resistance is then given as:

$$\Delta R_{max}/R = \varepsilon_{max} \times K \approx 2000\text{ppm} \qquad (3)$$

If the SG is connected in the manner of a Wheatstone bridge, this corresponds to a maximum signal output voltage of 2 mV/V. The resistance of common metal strain gauges is typically 350 Ω or 1000 Ω. The maximum variation in resistance and therefore the effective measurement range is within 0,7 Ω to 2 Ω. This small variation must be resolved according to the measurement task. The range of the resolution needed is very wide. It is between 10 ENOB (e.g. for pressure sensors) and 18 ENOB (e.g. calibrated scales).
In the upper range the precision of the measurement has to be:

Resolution: 2000ppm/2^{18} = 0,008 ppm eff.
or 26.9 ENOB referenced to the full resistance

The typical measurement rates are in between
2 - 8 Hz (e.g. scales) and
4 - 10 kHz (e.g. fast pressure sensors).

3.2 Measuring Principle

PSØ21 is based on the **PICO**STRAIN measuring principle showing a new approach to strain gauge measurement. Contrary to the Wheatstone bridge where the variation of resistance is transformed into a variation of voltage, **PICO**STRAIN transfers it into a time interval. For this purpose the SG resistors are connected to a capacitor, forming a low-pass filter.

The capacitor is charged to the supply voltage and then discharged through one of the SG resistors. The discharge time down to an arbitrary trigger level is measured with ultra-high precision using a TDC (Time-to-Digital Converter).

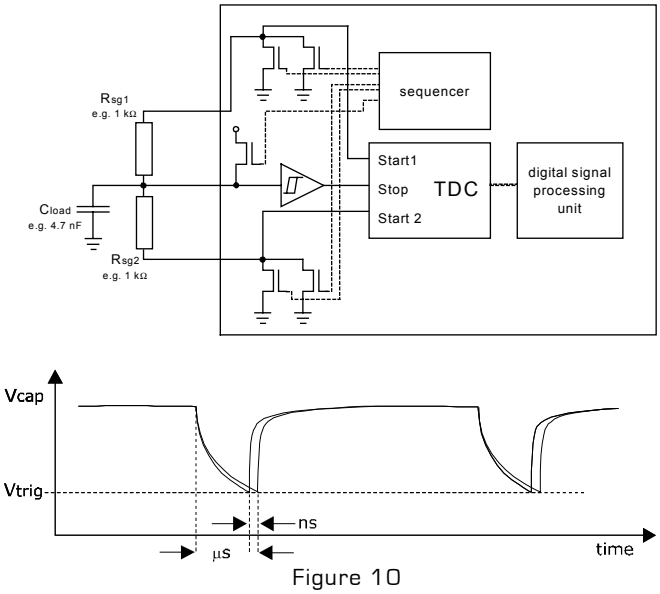


Figure 10

The discharge time is in the range of 2 to 100 µs. The TDC unit used in the PSØ21 has a single-shot resolution of typ. 15 ps.

This measuring process is repeated in time-multiplex with both resistors of a halfbridge, using the same capacitor and the same comparator. Calculating the ratio of the results will turn out the absolute values and temperature dependencies of the capacitor and the comparator.

Additional patented circuits and algorithms inside the PSØ21 compensate for further error sources like the switch-on resistance of the output drivers (R_{dson}) and the propagation delay of the comparator. The result is very precise, nearly free of gain errors and very stable with temperature. In total each single measurement is made of 8 discharge/charge cycles.

Due to the measuring principle, PSØ21 does not need a fullbridge but a halfbridge is sufficient. In total PSØ21

is capable of measuring up to 4 halfbridges. The supply of the halfbridge is provided directly by the PSØ21. There is no need for a separate supply of the SG. Also the reference voltage is not required.
Thanks to the pulsed driving the PSØ21 easily controls the current through the whole system and, even more important, reduces the current consumption to remarkably lower values than comparable ADC systems.

In a standard circuit for a fullbridge the common + and – connections of the two halfbridges are disconnected. The halfbridges then are connected directly to the PSØ21 (Figure 11).

The PSØ21 can handle also the classical Wheatstone bridge. Therefore it is necessary to use a slightly modified comparator circuit. In general it is not possible to get the same high resolution as with the standard circuit. For Wheatstone bridges it will be 0.6 Bit less. We recommend to use the Wheatstone mode only in applications with long cables (> 0.5 m) between sensor and electronics. In Wheatstone mode it is possible to work with up to 10m cable length (Figure 12).

3.3 High Precision

Depending on the configuration, the PSØ21 is capable of doing up to 50.000 single measurements per second. Each of these single measurements has a precision of 18 to 22 Bits referring to the initial resistance value. Referring to the measurement range this is about 10 to 13 effective Bits (ENOB).

If higher resolution is needed, internal chip averaging can do this. The resolution will be improved approximately by the square root of the number of samples. The maximum averaging rate of PSØ21 is 4095. Therefore the resolution can be improved by a factor $\sqrt{4095} = 64$, which corresponds to additional 6 ENOB. Of course, it is possible to select any interim value. There is a wide variety in setting resolution/update rate and it is possible to find the optimum setup for a dedicated measurement task.

It is also remarkable that the resolution is very insensitive to low supply voltage. When using a 2.0 supply voltage for the strain gauge and the PSØ21 the loss in resolution compared to 5 V supply voltage is only 1.1 Bit. Another effect is that the rms noise also decreases with lower supply voltage, e.g. at 4 kHz update rate from 1.05 µV at 5 V to 0.78 µV at 2.0 V. This convenient behavior is unknown from A/D converters.

In section 2 of this datasheet there are tables with data for resolution vs. average rate at different values of supply voltage.

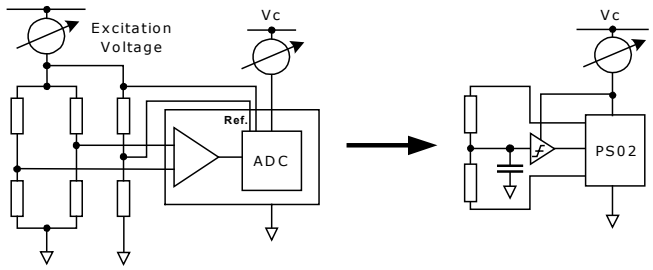


Figure 11

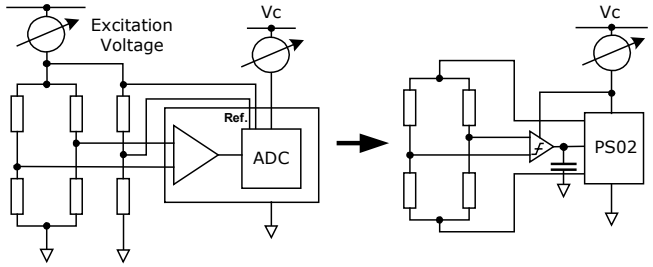


Figure 12

3.4 Low Current Consumption

Up to now we discussed the maximum performance of the PSØ21. It is a main feature of PSØ21 that unused performance (resolution / update rate) can be re-invested into lower power consumption. According to the application it is possible to decrease the total current of the system by decimal power.

Example 1:

If the requirements are 2 Hz update rate and 10 ENOB resolution, the total current consumption, including current into PSØ21 and strain gauge, is less than <10µA. Thereby it is hardly affected by the resistance value, whether it is 350 Ohm or 1000 Ohm.
Such an application can easily be driven from a solar cell.

Looking for a total current of the circuit less than 200 µA it is necessary to be aware of the comparator as the main consumer. The quiescent current of the recommended comparator circuit is about 180 µA @ 3V. PSØ21 there offers the possibility to switch off the comparator between the measurements automatically.

By this method the current into the comparator can be reduced to a few µA at low measuring rates.

As a further advantage the current into the strain gauge and therefore the power dissipation is reduced (Power dissipation being proportional to the square of the current). Self-heating is a difficult problem in high precision applications and may be reduced or even eliminated by the **PICO**STRAIN measuring principle.

Example 2:

Taking a calibrated scale with 3.000 scale divisions and 5 Hz update rate, the minimum noise of PSØ21 is already too low by a factor of 4. This surplus in noise can be re-invested in saving current. By setting exactly the necessary resolution the current will be reduced by a factor of 16 and the power dissipation by a factor of 256. Compared to the standard method of measuring a strain gauge, using a fullbridge and an ADC, the power dissipation in the strain gage is reduced by about 99%.

3.5 High Update Rate

The **PICO**STRAIN measuring principle is very well suited for high update rates. There is no sudden drop in resolution above a dedicated frequency, as it is known from Sigma-Delta ADCs. With PSØ21 it is possible to achieve 50 kHz at 18.3 ENOB resolution referred to resistance or 9.3 ENOB referred to full scale at 2mV/V.
Even at full speed a PSØ21 based system needs less current than traditional systems. Taking a 1 kOhm SG, the total current of the system at full speed in measuring range 2 (approx. 4 kHz) is about 3.5 mA. This is still less than the usual current only into the SG.

For higher frequencies (> 10 kHz) measuring range 1 is recommended. For frequencies > 10 kHz measuring range 1 must be used. It is possible to measure with up to 50 kHz. The operating current of PSØ21 increases in measuring range 1 up to 10 mA. At update rates > 10 kHz the resistance values of the comparator must be changed (please refer 4.3 for details).

4. Basic Functionality

The following description of PSØ21 is based on the measurement range 2 configuration that shows the best results in most applications.

The other operating modes will be described in section 6. Sections 4.1 to 4.4 describe the external circuitry needed for PSØ21. After that the basic operation and the various options to control the measurement will be described.

4.1 Connecting the SG

4.1.1 Halfbridge

PICOSTRAIN based systems do not need a fullbridge. Two resistors, below called halfbridge, are sufficient. Together with a capacitor these two resistors form a low-pass filter. The capacitor is loaded to Vio and then alternately discharged through the resistors.
PSØ21 offers two sets of ports, one for each halfbridge. Each block is made of 6 pins, where each SG element is connected via 2 pins to PSØ21.

The pins for halfbridge 1 are:

Pin	# Pin	SG
SG_A1, SG_A2	48, 47	R + ΔR
SG_B1, SG_B2	45, 44	R – ΔR
Load1	2	
Sense1	3	

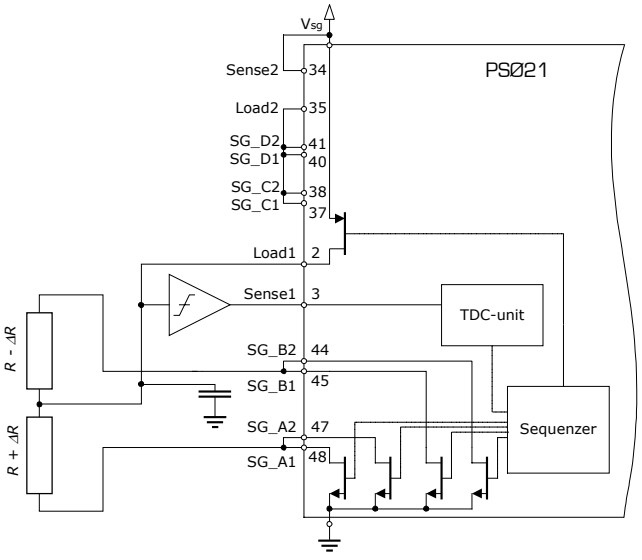


Figure 13: Halfbridge

Equivalent for halfbridge 2:

Pin	# Pin	SG
SG_C1, SG_C2	37, 38	R + ΔR
SG_D1, SG_D2	40, 41	R – ΔR
Load1	35	
Sense1	34	

The connection has to be made according to Figure 13. Attention must be paid to the external connecting of neighboring SG pins (e.g. SG_A1 and SG_A2). The power of the output driver is doubled that way.
The pins of unused SG elements must be connected to the corresponding Load1/2 pin. The unused Sense1/2 input must be connected to Vsg.

The halfbridge itself is selected by Bridge[1:0] in Register 0:
Bridge = 1: Halfbridge 1 (Ports A & B)
Bridge = 2: Halfbridge 2 (Ports C & D)

4.1.2 Fullbridge

In order to achieve the highest resolution with a fullbridge this fullbridge must be split into two halfbridges:

Both halfbridges will be measured in an interleaved manner. The circuit is shown in Figure 14. This mode is called ‚Alternating mode'. An advantage of the Alternating mode is the redundancy or tolerance against failures. If one halfbridge fails, the other halfbridge is still fully operating. Further it is possible to measure two halfbridges with different resistance values.

By the measuring principle only one comparator is necessary. For those applications that do not need 2 comparators we recommend the use of only one. This mode is called „One-Sense" mode.

The fullbridge mode is selected in Bits:
Bridge[1:0] in Register 0:
Bridge = 0: One-Sense
Bridge = 3: Alternating

The fullbridge mode is the one with intrinsically the lowest temperature drift of the electronics. Connecting the 2 halfbridges in a way that the results will be subtracted drastically reduces the temperature drift down to the range of 5nV/K. This value is up to 10 – 20 times lower than the one of a good strain gage. In the temperature drift mentioned the comparator circuit is already included.

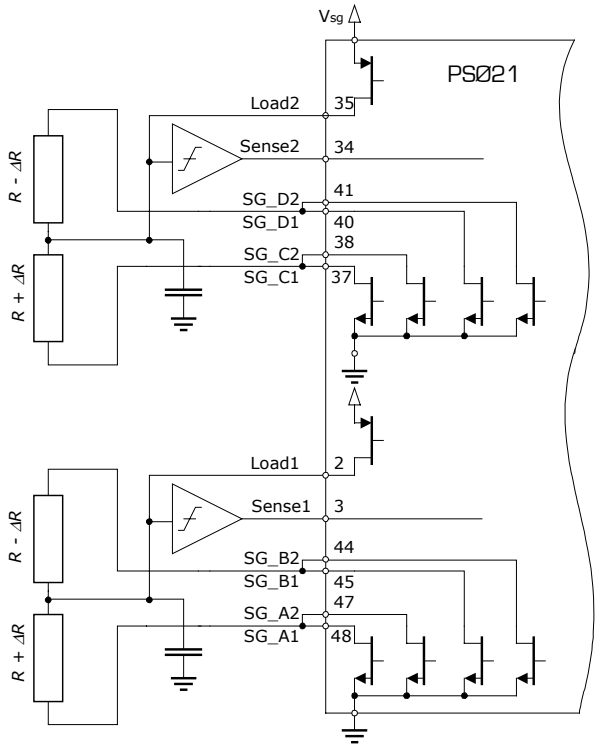


Figure 14: Fullbridge, Alternating mode

The calculation of the difference of the 2 halfbridges is set in register 0: [SubFB]=[1]). With this setting the halfbridge on A/B is connected inverse, means R – ΔR to port A and R + ΔR to ports B.

4.1.3 Doublebridge Mode

PSØ21 allows to measure up to 4 halfbridges or 2 fullbridges:

Doublebridge mode is selected by Bit DoubleBr in Register 0:
DoubleBr = 0: 1 Fullbridge
DoubleBr = 1: 2 Fullbridges

Following table lists the setting for the different Doublebridge modes:

Table 17
DoubleBridge=1

Bridge[1:0]	
0	Both fullbridges, One-Sense
1	Fullbridge 1
2	Fullbridge 2
3	Both fullbridges, Alternating

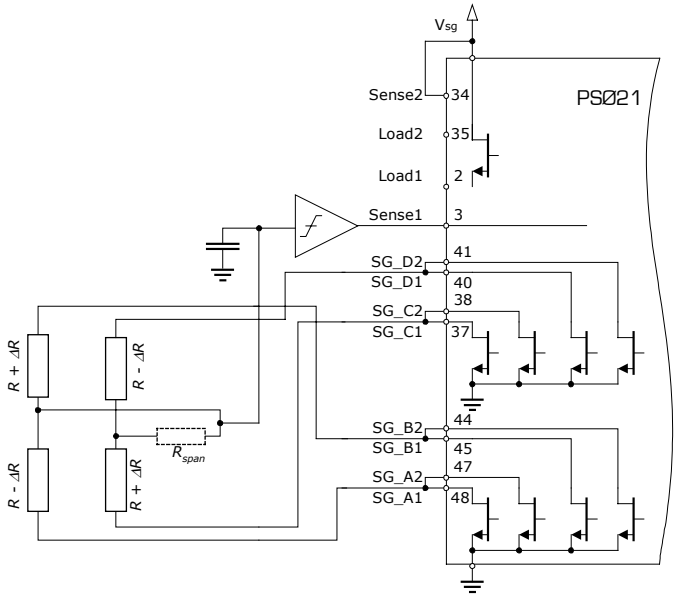


Figure 15: Fullbridge, One-sense mode

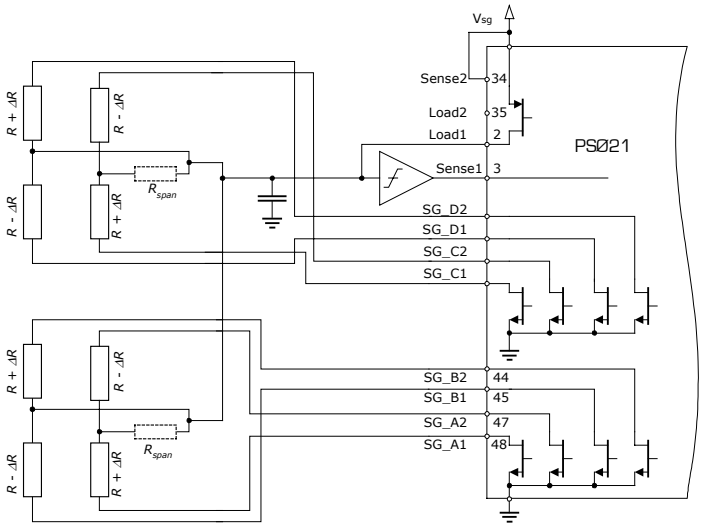


Figure 16: 2 Fullbridges

When working with Double-Bridge mode, the increase of driver output power by using pairs of pins is not available. This doubles the number of ports available

for SG elements. When working with 350 Ω strain gauges the reduction of driver output power will give additional failures. We therefore recommend using higher values of strain gage resistance when working in Doublebridge mode.
The PSØ21 offers two different modes. The selection is done by setting the AvRate2 in register 9. A "0" (def.) stands for mode 1, any higher value for mode 2.

Mode 1:
In mode 1 the fullbridges are measured separately and alternately (A/B and C/D) on the basis of the averaging rate specified in the AVRate register. After one fullbridge is measured the interrupt flag is set and data can be read out. The MSB of the status register indicates which fullbridge was measured. The measurement for the other fullbridge is started automatically. Both fullbridge measurements are based on one and the same register setup.

A further option is to select whether one or two comparators will be used. Figure 16 shows a configuration with only one comparator. This makes sense for bridges locally neighbored to each other. If the bridges are locally separated, it is better to work with two separated comparators.
Theoretically it is also possible to measure only one fullbridge in Doublebridge mode, but this option is implemented for testing only and should not be used in real applications.

Mode 2:
In mode 2 the two fullbridges are not automatically and alternately measured but the separate fullbridges are selected by an OPCode:

OPCode 0x08 Select fullbridge 1
OPCode 0x09 Select fullbridge 2

Each fullbridge is measured with its own averaging rate, AvRate for fullbridge 1 and AvRate2 for fullbridge 2. During the measurement of one bridge the user can send an OPCode for measuring the other bridge. After the interrupt from the first measurement the PSØ21 then automatically starts the measurement of the second bridge. The measurement continues with that bridge until the user switches back to the other bridge. Both bridges use the same Cycle time.

This mode increases the flexibility of the Doublebridge mode:

- Using different averaging rates allows giving each bridge its own resolution and measurement time.
- It is possible to have different update rates for the two fullbridges

4.1.4 Wheatstone Mode

The Wheatstone mode allows connecting a classical Wheatstone bridge configuration to the PSØ21. It is activated by setting register 8, WheatEN = "1".
It is also possible combine this mode with doublebridge mode for two fullbridges. The configuration options are the same as for the normal modes.

The following figures show how to connect the Wheatstone bridge:

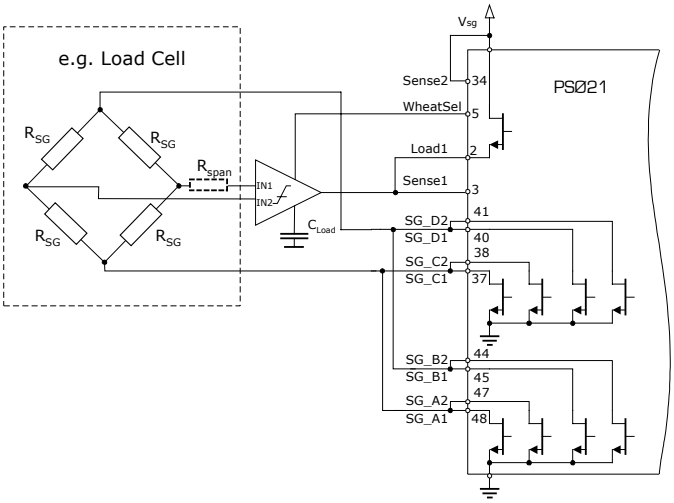


Figure 17

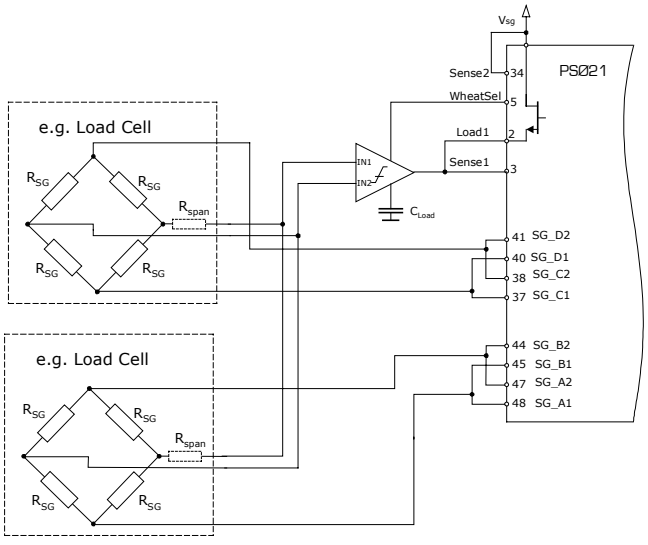


Figure 18

Notes:

- The comparator circuit has to be modified. For details see 4.3.4 Wheastone Comparator.
- The gain compensation can be used only in combination with separate gain compensation resistors (reg 8: SepGain = 1). For details see 4.7.2 Separate Compensation.
- When calculating the discharge capacitor it has to be considered that the strain gage resistance is reduced by 25%. The discharge capacitor's values are increased (e.g. 220 nF instead of 180 nF for a 350Ω SG).

Advantages of the Wheatstone mode
This mode shows technical advantages when the applications needs long cables between sensor and electronics. In this mode the cable capacities are self-compensated. So it is possible to work up to 10 m cable length. For such applications it is necessary to use LoadStart = 1 and LoadStartDel = 1 to suppress reflections of the pulses during Start.

Another advantage is that current Wheatstone bridges can be connected to PSØ21 without any modification.

Disadvantages of the Wheatstone mode
In this mode only 66 % of the standard performance can be achieved. The resolution is reduced by 0.6 Bit. The characteristic valuefor the strain is reduced from 2 mV/V to 1.3333mV/V. Because of this the Wheatstone mode is not suited to current saving applications. At the same resolution the current increases especially due to the necessarily increased averaging rate by a factor of about 2.5. Because of the reduced resolution /higher current consumption the Wheastone mode should be used only in applications where its advantages get dominant.

4.1.5 Long Wires (6-wires)

When working with long wires it is possible to compensate also the wire resistance (not in Doublebridge mode). This is comparable to the 6-wire technology. This is achieved by joining the two connections per resistor at the sensor's site, not at the PSØ21 site.

In case of long wires without Wheatstone mode it is very important to fix the wires mechanically. This will avoid distortions from the wire's parasitic capacity. Principally for cables longer than 1 m we recommend to use the Wheatstone mode. With Wheatstone mode the 6-wire compensation is possible in the same way.

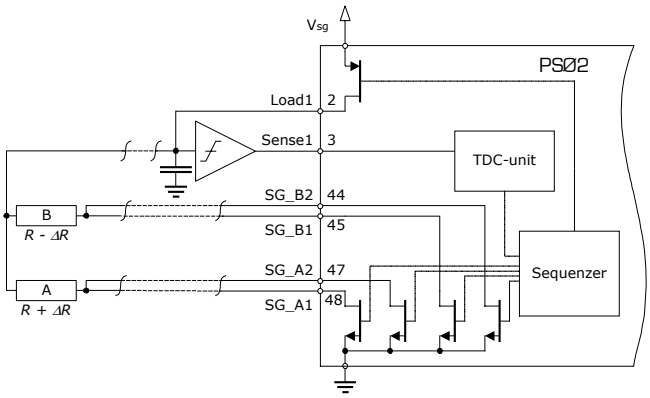


Figure 19

4.2 The Capacitor

For correct operation it is necessary to select the right capacitor value and the right capacitor material.

Following the recommendation for the comparator circuit given in Figure 20, the discharge time is about

$$\tau = 0,7 * R_{SG} * C_{Load}.$$

In measurement range 2 the time interval measurement uses not only the high-speed unit of the TDC but also the reference clock (pre-divider). Doing this the measurement range of the TDC is extended to 2^8 periods of the reference clock. For best resolution the discharge time should be in the range of 50 to 60 µs. This allows update rates up to 2 kHz. For higher update rates the discharge time must be reduced. At update rates higher than 7 kHz measurement range 1 is recommended (see section 6).

The following values are recommended for measurement range 2:

R_{SG}	C_{Load}
1 kOhm	68 nF
350 Ohm	220 nF

For checking purposes the measured and calibrated time interval measurement of the TDC can be read. It is given as value TDC1 (read register 4) in multiples of the high-speed reference clock (divided by ClkHSDiv). It is necessary to set [GainRate] = 0 before.
Generally the size of the discharging capacitor is not very critical. There is a wide range (± 30%) of capacitance without system malfunction.

4.2.1 Capacitor Material

The discharging capacitor is an important part of the circuit and has direct influence on the quality of the measurement and the stability with temperature.

We recommend the following materials (group 1):
- CFCAP® (Multilayer ceramic Taiyo Yuden)
- COG or NPO ceramics
- Polystyrene
- Polyvenylsulfid

Also these materials may be used but with some small losses in temperature stability (group 2).
- X7R
- Polyester

The following materials must **not** be used (group 3):
- ZOG

When working with capacitors out of group 2 the following register settings are mandatory:

Name	Value
GainCorRate	0 or 1
TempRate	0 or 1

These settings are also preferred when working with capacitors from group 1. The reason is that capacitors are mechanical devices, too. With the above-mentioned settings the PSØ21 driving sequence guarantees the lowest possible mechanical stress. This has a positive effect on the measurement quality, especially at high measuring rates.

4.3 The Comparator

The comparator significantly influences the quality of the measurement. It is not integrated in the PSØ21. It is possible to get results of outstanding quality using a very simple bipolar comparator circuit as shown in Figure 20, much better than with an integrated CMOS comparator. Further the circuit is very insensitive to low supply voltage. When driving the chip with Vcc and Vsg at the lower limit of 1.8 V, the absolute noise is still less than with 5 V – a proof of the power and robustness of this simple and low-cost measuring principle.

Note:
All components for the comparator circuit are standard components. There are no special demands. For the resistors we recommend metal film types. The capacitor at the collector resistor should be of COG/NPO type. All other capacitors are standard. For the PNP transistors we recommend low noise devices like 2N5082 or BC859. There is no need to use matched transistors.

4.3.1 Standard Comparator

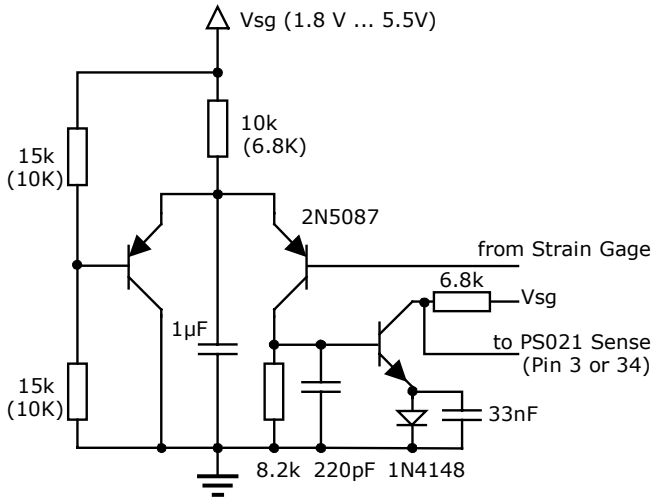


Figure 20

This is the most simple comparator circuit that might fit to most of the applications. It offers good noise data and a high supply voltage rejection (PSRR), which is 120 dB with fullbridges. The gain error over temperature (1.5 ppm) and voltage (0.015 %/V) is fully sufficient. It is e.g. good enough for OIML class III approved scales up to 6000 scale divisions.
.
The comparator in Figure 20 has a quiescent current of about 180 µA at 3 V supply voltage. As the comparators circuit shown is non-inverting, it is necessary to set the Sense-inputs be non-inverting, too.

The resistor values in brackets should be used at 2.2 V supply voltage.

Reducing the 220 pF by 50 pF will further improve the PSRR and gain error, but on the cost of additional noise.

4.3.2 Low Noise Comparator

Using this comparator will show the best performance with respect to noise showing a high PSRR and a low gain error at the same time. The improvement can be seen when setting up to 5 transistors in parallel (interim values are possible, too). The noise will be lowest with C1 = 220 pF. The noise data will be about 30 to 40 % better than with the standard comparator.

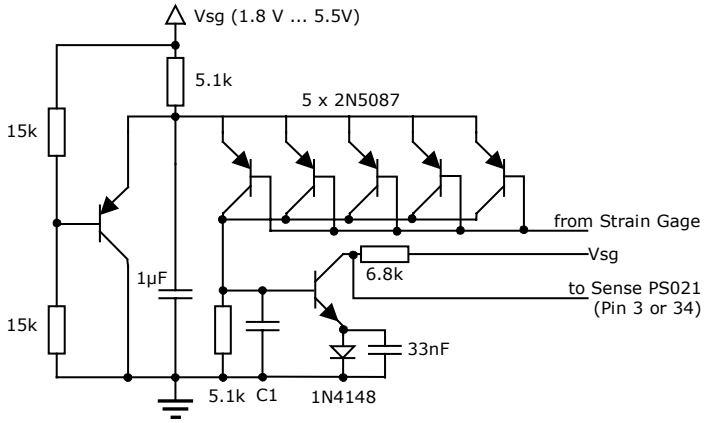


Figure 21

Reducing C1 to 56 pF improves the PSRR to > 140 dB, the gain error over voltage to 0.001 %/V and the gain error over temperature below < 1ppm/K. The noise is increased but still less than with the standard comparator. These very good data are based on a wide supply voltage range; they are based on a Vsg variation from 3 V to 5 V and a Vcc variation from 2.5 V to 3.3V. Especially the high PSRR is 10 times better than the one of best A/D converters. It allows the operation directly from a floating supply voltage under the limits of OIML-R76 class III approved scales for 6000 scale divisions.

4.3.3 Switched Comparator

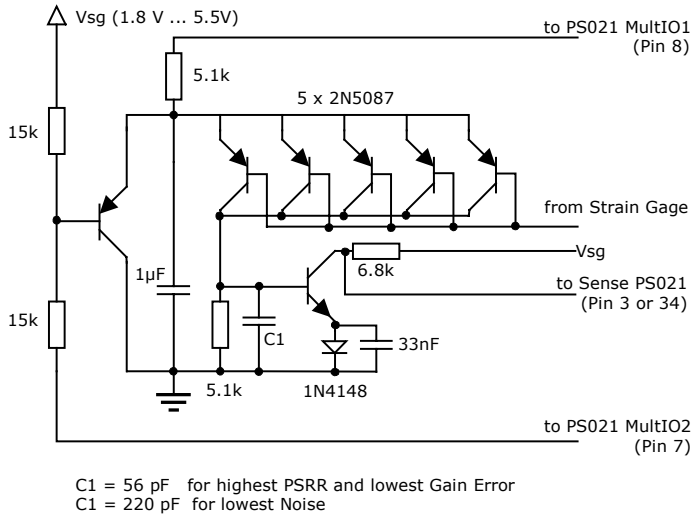


Figure 22

The PSØ21 offers the possibility to switch off the comparator for applications with a very low current target of 100µA and less. Otherwise the comparator would be the main current drain. The comparator is disabled between single conversions and also during the recharge cycle of the discharge capacitor. The current is practically reduced to 0.

For this comparator type the PSØ21's 32 kHz clock has to be used. This clock controls the timers for the comparator disable.

This option is configured in Bits 16 to 21 in register 8.

CompConOn
Switches on the comparator control option. Configures the pins 7 and 8, MultIO1 and MultIO2 for the comparator disable.

CompSleep
Special bit that can be used in case of very long brakes between measurements (e.g. > 2 sec.). With CompSleep = 1 the port MultIO1 is set to high-Z and port MultIO2 is set to "1". The middle capacitor (1 µF) is charged to Vio through the emitter resistance. The comparator is now in a currentless sleep mode but can be waked up very fast.

To use this option it is necessary to set Mfake to 3 (4 fake measurements). This is the time the comparator needs to get back to the active state.

CompCon
The 4 comparator control bits are split into:

CompCon<1..0>
Controlling the switch-on behavior
0: Comparator is always on
1: Comparator is off during the capacitor charging cycle (Load = 1)
2: Comparator is active only together with the oscillator, presumed that this one is pulsed by single conversion mode
3: Comparator is active only together with the oscillator, presumed that this one is pulsed by single conversion mode. Additionally it is off during the capacitor charging cycle (Load = 1)

CompCon<3..2>
It is recommended to not change the default values.

4.3.4 Wheastone Comparator

The comparator circuit has to be modified a little bit when working with Wheatstone bridges.

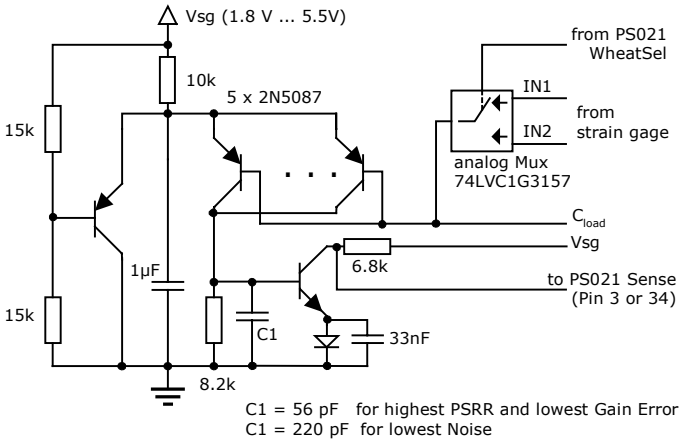


Figure 23

An analog multiplexer is added to the comparator circuit. It switches the halfbridges alternately to the comparator. The switching signal is coming from pin 5 of PSØ21, WheatSel (only in Wheatstone mode). No further modifications are necessary. The comparator can be set up as standard type, low noise type or switched type.
The multiplexer 74LVC1G3157 shows very good results, has a wide operating voltage range and is of low cost.

4.3.5 Comparator for Highest Rates

The component's values mentioned up to now have been dedicated to applications below 5 kHz. They have to be modified for higher update rates.

For measuring rates up to 50 kHz we recommend:

Voltage divider:	15 K → 6.8 K
Emitter resistor:	10 K → 3.3 K
Collector resistor:	8.2 K → 3.3 K
Collector capacitor:	56 pF

The low-noise setup makes no sense at high measuring rates because of the dominance of other noise sources.

4.4 The Oscillator

PSØ21 needs up to two reference clocks when operating in measurement range 2, depending on the mode:

- High-speed clock as predivider for the TDC measuring unit
- High-speed clock or 32 kHz clock for setting the cycle time

4.4.1 High-speed Oscillator

This one is always needed with measurement range 2. There are two sources for the high-speed oscillator:

- Connecting a resonator or quartz to the PSØ21's clock generator pins ClkHSin, ClkHSout
- External reference clock at ClkEx (Pin 21)

Principally we recommend using the clock generator of the PSØ21. The clock is used as predivider for the TDC measuring unit. Its quality has direct influence on the quality of the measurement result. Low jitter and short-time stability are the important properties. When using the microcontroller's clock additional noise will make the measurement quality worse.
The quality needed for the resonant circuit is about 500 – 1000. From there it is sufficient to use a ceramic resonator. A quartz oscillator is not necessary; it produces no better results and has a longer settling time.

The high-speed oscillator of the PSØ21 is activated by setting [ClkHSon] in register 7. The following options are available:

ClkHSon =
- 0 = Oscillator off.
- 1 = Oscillator on immediately, continuously running. The measurement starts immediately after opcode ‚Start Measurement' or external trigger.
- 2 = Start oscillator after opcode ‚Start Measurement' or external trigger, The measurement starts with 640 µs delay. At the end of the measurement the oscillator is switched off.
- 3 = as ‚2', but with 1280 µs delay.

Options 2 and 3 can be used only in combination with the 32 kHz oscillator. They make sense only in Single-conversion mode [SingleCon = "1"]. The programmable delay guarantees that the oscillator has settled before the measurement starts. For ceramic resonators 640 µs will be sufficient. quartz resonators need 1280 µs.

Whenever an external reference clock will be used the pin ClkHSin must be connected to GND. Whenever the internal oscillator is used, ClkEx must be connected to GND.

Figure 24 shows the external circuit for the oscillator.

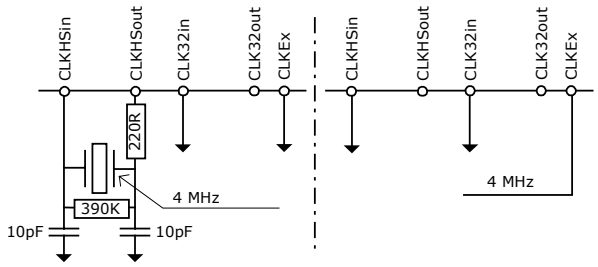


Figure 24

There is an internal divider dedicated to the high-speed clock, regardless of which one is used:

ClkHSDiv	Divided by
0	1
1	2
2	4
3	8

It must be seen that behind the divider the internal frequency is in the range of 2 - 5 MHz. Therefore the external high-speed clock is limited to the range of frequencies between 2 and 40 MHz. For reasons of noise reduction it is recommended to use frequencies below 5 MHz. We recommend a frequency of 4 MHz. In this case the divider should be set to 1.

Attention:
At low core voltages (Vcc < 2.2 V) the series resitor has to be changed from 1K5 to 560Ohm for correct operation.

4.4.2 The 32kHz Oscillator

It is possible to use a 32kHz clock as a time base for the cycle time. The external circuit is shown in the following figure. Here, too, a ceramic resonator is sufficient. There is no need for a quartz. The current consumption is in the range of about 3 µA @ 3 V.

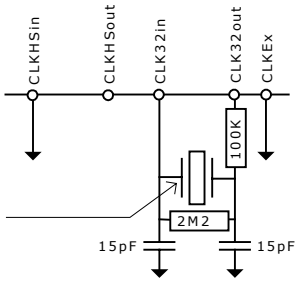


Figure 25

The additional 32kHz oscillator should be used in applications with strong need for current saving. In these cases Single-conversion mode should be selected together with ClkHSon > 1. The high-speed oscillator is running the only during the measurement. The high-speed clock is still necessary for the TDC unit in measurement range 2.

The external circuit is necessary only if the 32 kHz oscillator is used. Otherwise Clk32in has to be connected to GND.

The following sections describe the measurement itself:

4.5 Cycle Time

Cycle time is described as the sum of discharge time and recharge time. The user defines it in multiples of the reference clock. The setting for the cycle time defines the number of single measurements per second and in consequence the precision / update rate. It is therefore a very important value and requires some planning.

Reg	1	Description
Bits	12 ... 23	
	0 ... 4095	CycleTime x Tref = Cycle time

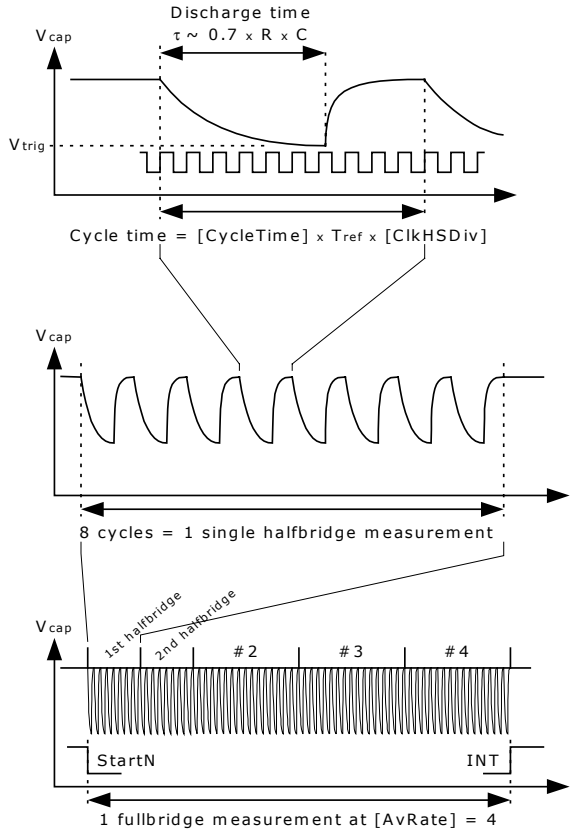


Figure 26

Measurement sequence during a cycle:

A new cycle starts with the intrinsic measurement, means the measurement of the discharge time of the capacitor. The capacitor is discharged from Vio through the SG resistors down to the threshold of the comparator. The remaining time is used to re-charge the capacitor back to Vio. Hence it is important to make a good choice for the cycle time, depending on the SG resistance, the capacity and the comparator's threshold.

For a correct operation it is mandatory that the cycle time is not too short.

Errors if cycle time is too short:

If the cycle time is shorter than the discharge time, the measurement is not finished, and the device will give a time –out.

If the time remaining after discharging is too short, the capacitor won't be recharged in a sufficient manner, leading to additional errors of the data.

The recommendation for the minimum charging time is:

$$T_{lade\text{-}min} = 2\ \mu s + C_{load}/nF * 120\ ns$$

Example 3:

R_{SG} = 1 kOhm
C_{load} = 68 nF

$T_{lade\text{-}min}$ = 2 µs +68 * 120 ns = 10.2 µs

This selection guarantees a minimum charging time of 15 to 20 τ, which will be sufficient for the capacitor.

On the other hand, the maximum cycle time is limited only by the size of the value CycleTime in register 1.

Usually the high-speed clock ClkHS is used as the reference for the cycle time. In measurement range it is also possible to select the 32 kHz clock. In measurement range 2 it is necessary to select the ClkHS.

Selection of reference in measuring range 2:

Sel_clk32k = 0 → CLKHS for reference
Sel_clk32k = 1 → 32 kHz for reference

Example 4: Choice of the cycle time

Measurement range 2
R_{SG} = 1 kOhm
C_{load} = 68 nF

Goal: valid data at maximum update rate

Tmeas = 0.7*R_{SG}*C_{load} = 47.6 µs
Tload-min= 2 µs +68 *120 ns= 10.2 µs

Tcycle-min = 47.6 µs + 10,2 µs = 57.8 µs

Taking CLKHS = 4 MHz as a reference for the cycle time we have the following settings
:
Sel_clk32k = 0 (select CLKHS)
CycleTime = 232 (232*250 ns=58 µs)
In this case the cycle time is 58 µs.

The maximum update rate is about 2,15 kHz in halfbridge mode, about 1.08 kHz in fullbridge mode and about 539 Hz in doublebridge mode. Additionally it depends on the settings for GainCorRate and TempRate (see section 5),

4.6 Averaging / Resolution

4.6.1 Precision of a Single Measurement

The precision of a single measurement (AVRate = 1) depends on 2 parameters:

- The measurement range
- The discharge time

As long as the update rate is not higher than 5 kHz we recommend working with measurement range 2. Setting the discharge time to 50 µs, PSØ21 has the performance shown in the following table. The precision of a single measurement depends on whether SINC3 filter is active or not (Fast-settle).

Measurement range 2:

Vsg	**SINC3**	**Fast-settle**
5.0 V:	0.60 µV	1.15 µV
3.0 V:	0.55 µV	0.88 µV
2.0 V:	0.57 µV	0.98 µV

Values in µV RMS noise.

At the same the data show the performance of PSØ21 at 2 kHz update rate in measurement range 2.

There is no reduction of resolution when working with a halfbridge only!
This is an important key feature of the **PICO**STRAIN measurement principle.

Standard circuits based on A/D-converters need a Wheatstone bridge in any case. If only 2 SG resistors are available, a pair of fixed resistors must simulate the missing 2. In consequence the differential output voltage of the bridge is halved, e.g. 1mV/V instead of 2mV/V. This is equivalent to a loss of 1 Bit in resolution. In case a halfbridge shall be measured by an A/D-converter and the target resolution should be as good as with PSØ21, the A/D-converter must have twice as good noise data.

PICOSTRAIN devices typically work with halfbridges. Measuring fullbridges is nothing else than measuring two halfbridges alternately. Halfbridges and fullbridges are equal to the PSØ21. Both give the same resolution at the same update rate.

Note:
Taking the proposal given in Example 4 it is possible to measure a fullbridge with a maximum update rate of 690 Hz, The resolution is better by factor √2 compared to a halfbridge at 1.38 kHz. To get 1.38 kHz update rate with a fullbridge, it is necessary to reduce the charging capacitor and the charging time by a factor of 2. The final resolution will be slightly reduce compared to a halfbridge.

4.6.2 Increasing Resolution by Averaging

PSØ21 internally improves the precision of the measurement results by averaging. The measuring principle guarantees that no significant systematic errors affect the result. The standard deviation is improved by the square root of the averaging rate.

Reg	1	Description
Bits	0 ... 11	
	0 ... 4095	AVRate

Example 5:

Halfbridge as given in example 4. 5V SG supply voltage. SINC3 Filter enabled.

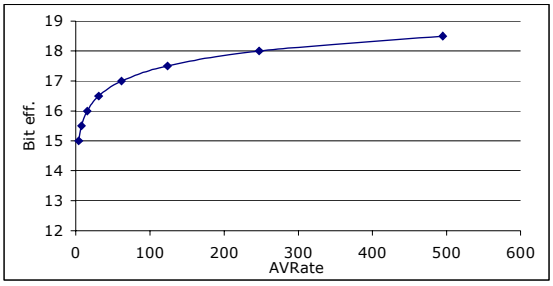
Averaging rate:
AVRate = 430

Update rate:
2,150 Hz/430 = 5 Hz

Precision:
V_{noise}=0.6 µV/√430 = 29 nV rms

With 1000µ (2mV/V) maximum strain the resolution can be calculated as:

Resolution = 10mV/29nV
= 344,000 LSB or 18.4 ENOB



Note: An ADC based solution working on a halfbridge requires an ADC with about 15nV rms noise at 5 Hz update rate.

4.7 Gain Compensation

The comparator itself shows a significant propagation delay, which is added to the result. It introduces an additional, temperature dependent gain error. The absolute maximum of this error is in the range of 1 % of the maximum measured value. PSØ21 is capable of measuring the comparator's propagation delay and therefore can compensate for the gain error.
This compensation takes 1 measurement (= 1 cycle time) per halfbridge. The measurement is done at the end of a normal measurement. For noise reduction the correction data can be averaged (GainAVRate).

The registers GainCorRate[3:0] and GainAVRate[3:0] control the gain compensation:

GainCorRate	Frequency
0	Off
1	Each measurement
2	Each 2nd measurement
3	Each 3rd measurement
.....	
15	Each 15th measurement

GainAVRate	Averaging
0	No averaging
1	Averaging factor 2
2	Averaging factor 4
.....	
15	Averaging factor 16,384

For the most applications we recommend to set GainCorRate to 1 and GainAVRate to 3 (8-fold).

Using these settings the gain drift over temperature is only about 1 ppm/K (0.0001 %/K) of full scale. It is further decreased by the use of the PSRR optimized low-noise comparator. The gain error of a good, temperature compensated strain gage is in the range of 10 - 15 ppm/K, which is much worse than the PSØ21 value. This error can be neglected.

The remaining temperature drift is not random but systematic and always negative.

4.7.1 Standard Compensation

For a standard compensation no additional circuitry is necessary. The PSØ21 by itself generates the necessary measurement data for calculating the comparator delay. Besides the strain gage measurements only 1 or 2 additional measurements are needed.

Halfbridge	1 additional cycle
Fullbridge alternating	2 additional cycles
Fullbridge one-sense	1 additional cycle

The standard compensation can be used in combination with all PICOSTRAIN typical setups. It can not be used with Wheatstone mode.

4.7.2 Separate Compensation

This compensation method uses two additional resistors. The resistors are connected between the discharging capacitor (Wheatstone mode: IN2) and the Sep1/Sep2 inputs.

Writing register 8: SepGain = "1" activates the separate gain compensation.

Applications:
- Separate gain compensation is mandatory in Wheatstone mode
- Optional in HB1 and one-sense fullbridge measurements
- Not possible in alternating fullbridge measurements

The following figure shows the schematics for use of separate gain compensation:

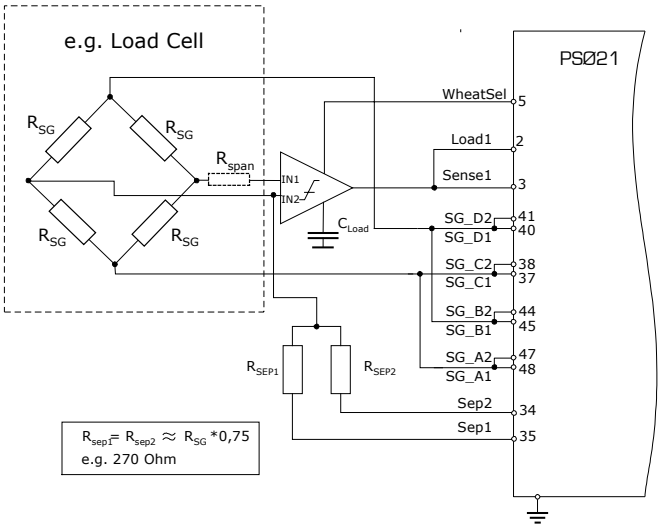


Figure 27

In this mode the Sense2 and Load2 inputs are reconfigured to Sep1 and Sep2 inputs. The resistors are connect between those inputs and the discharging capacitor or, in Wheatstone mode, the IN2 comparator input.
The value of resistors Rsep1 and Rsep2 should be in the range of the strain gage resistance. It is not necessary to trim them to the exact values. The results are not better. It is sufficient to select the nearest E12 series value where the next highest one is preferred. Attention must be payed that the increased discharge time due to the higher resistance does not collide with the cycle time and the maximum range of the TDC unit. There is no possibility to read the time values Sep1 and Sep2.

A separate gain compensation always needs 3 additional cycles after the basic measurement (Avrate * 8 * #HB).

Note:
When working with Wheatstone bridges the effective resistance of the bridge is reduced to 75 % of the single resistors. They are e.g. effective 262.5 Ω instead of 350 Ω. Therefore the choice for Rsep would be 270 Ω.

4.8 Update Rate

The update rate results from the cycle time and the averaging rate. Attention should be paid to the fact that a single measurement takes 8 cycles of discharging/recharging.

Depending on the settings, further measurements due to gain compensation, temperature measurement and fake measurements (s.5.5.1 MFake) must be added. The gain compensation measurement is done maximum once per SG measurement and takes normally 1 cycle, with separate compensation resistors (SepGain = "1") 3 cycles per halfbridge. The temperature measurement is done at a maximum of once per SG measurement and takes 2 cycles. Fake measurements are done once per SG measurement.

The rate of gain-, temperature- and fake measurements is configurable. For details see the dedicated sections.

The total time for a measurement is calculated as:

t_{meas} = (AVRate x 8 x #HBs + 1+2+0) x Tcycle

(@ GainCorRate = TempRate = 1, Mfake=0)

Example 6:

Tcycle:	65 µs
AVRate: 100	
GainCorRate:	1 (each measurement)
SepGain:	1 on
TempRate:	1 (each measurement)
Mfake:	1
Strain gage:	Fullbridge

t_{mess} = (100 x 8 x 2 + 3 + 2 + 1) x 65 µs
= 104.39 ms

The update rate therefore is 9.6 Hz at a noise value of 40 nV rms or about 18 Bit resolution referred to 2mV/V max. strain.

4.9 Serial Interface (SPI)

The SPI interface is a serial one with total 4 lines:

SSN - Slave Select
SCK - SPI Clock
SI - SPI Data In
SO - SPI Data Out

Additionally there is an interrupt line:

INT - LOW ACTIVE

PSØ21 can only be used in one out the four possible SPI modes, to be specified as:

Clock Phase Bit =1
Clock Polarity Bit =0

The timings are shown in Figure 4: Write and Figure 5: Read.

Incremental Access - SSN as Reset

The SerialSelectNot (SSN) line is the HIGH-active reset for the serial interface. After SSN is set to LOW different operations can be addressed, not depending on the status of the interface before the reset. After SSN was set to HIGH the address for incremental access is reset to 0. After an incremental access it is necessary to give a reset (SSN = HIGH) to the interface before sending a new opcode.

3-wire Interface without SSN

As a limited option the serial interface can be operated without the SSN line at all. In this case SSN must be connected to GND. Any read or write command is made of 32 Bit (opcode + data). After the access has finished the interface is ready for a new opcode. This is true also for Reset or Start-New-Cycle commands, although their length is only 1 Byte.

Note:
All pulses on the SCK wire - also spikes - are counted. In case of a miscount the communication is lost. This requires a power-on reset by a LOW at pin 24, RSTN.

There is only a limited possibility to use incremental access with a 3-wire interface, because the read access cannot be stopped. In this case it is necessary to give an external reset stopping the complete measurement.

4.9.1 Separate Supply Vio

The SPI interface and all other µP control pins have their own supply (Vio). This one is of free choice within the specification and does not depend on the other supply voltages, especially not on Vsg. They are fully separated. This offers a wide range of supply options in multi-power systems.

4.9.2 Write into the Chip

Table 18

MSB			LSB					Description
1	0	0	0	ADR 3	ADR 2	ADR 1	ADR 0	Write 24 Bit to address
1	1	0	0	0	0	0	0	INIT-Reset
0	1	0	1	0	0	0	0	Power-On Reset
0	0	0	0	0	0	0	1	Start Measurement

The first 5 command Bits specify the command. In the first case the following 3 ones give the target address for the write command. The transfer starts with the MSB and is finished sending the LSB. After sending the last Bit PSØ21 transfers the data into the target register or executes the command. It is not possible to do incremental writing. Each register must be addressed separately.

4.9.3 Read from the Chip

Table 19

MSB							LSB	Description
1	0	1	1	0	ADR 2	ADR 1	ADR 0	Read 24 Bit from ADR
1	0	1	1	1	ADR 2	ADR 1	ADR 0	Read 24 Bit from ADR, Auto-increment

When reading from the chip it is necessary to send the opcode first, too. The opcode is built of the command bits and the address bits. With the first positive edge of the clock following the opcode, PSØ21 sends the MSB of the addressed register to SO output. Each positive edge transfers the next lower Bit to the output.

An auto-increment function is implemented. If the clock continues after the LSB has been sent, and if SSN is still kept at GND, then with the next positive edge of the clock PSØ21 will transfer the MSB of the next higher register to the SO output pin. By this it is possible to read out the total register content of the PSØ21 with a single command.

An Interrupt resets the auto-increment unit. New data starting from address 0 can be read out without sending a new opcode. A read sequence can be stopped any time giving HIGH to the SSN line.

4.10 Controlling PSØ21

Before doing any measurements it is necessary to setup the measuring mode of the PSØ21.

4.10.1 Configuration

PSØ21 configuration is done in the following way:

1. Power-on Reset

After the power supply was applied, it is necessary to reset the device. One possibility to do this is to give a LOW pulse of minimum 250 ns length to pin RSTN. An alternate way is to write opcode 0x50 into the device. After the reset the PSØ21 is in wait state, no measurement is going on. All write registers have been set to the default values.

2. Write to registers

Writing into the registers starts with sending opcode 0x80 & ADR. The following 24 Bit are written into the register with address ADR.

Example 7:

0x83 is the opcode for writing into register 3, which specifies the multiplication factor.

It is necessary only to write into registers where the default settings shall be or must be changed.

Note: It may be necessary to write into registers that include chip-internal configuration bits. Also in this case it is necessary to write the complete register content and especially to write the default bits.

3. Init

Sending opcode 0xC0 starts an initialization (INIT) of the PSØ21. An INIT is comparable to a Power-on Reset but without changing the write registers. An INIT guarantees that the PSØ21 is in its initial, well-defined state.

The configuration is finished.

4.10.2 Measurement Start/Control

Sending opcode 0x01 makes the PSØ21 start measuring. According to the register settings PSØ21 carries out a complete measurement sequence. At the end of the sequence pin INT (Pin 23) is set to GND, indicating that data are available for reading now. Pin INT is reset to HIGH with the first access to the serial SPI interface. The measurement can alternately be started also by a positive edge at the StartM pin even if single conversion is not active.

Auto Mode

If the PSØ21 is configured to automatic measurement (SingleCon = 0), the next measurement starts while data is read out through the SPI interface. It absolutely necessary to ensure that the data is read complete before the next measurement sequence has finished. Otherwise the data will be overwritten. When reading from the interface while data are overwritten the data might have any wrong value.

Single-Conversion

If the PSØ21 is configured to Single-Conversion (SingleCon = 1), it goes into wait state after setting pin INT. A new measurement can be started in two ways:
a. Send opcode 0x01 through SPI interface
b. Positive edge at pin StartM (Pin 14)

Especially option b. opens the chance to synchronize the PSØ21 update rate to an external device. Of course it is necessary to ensure that the external frequency is lower than the maximum possible update rate of the PSØ21 with its current setup.

4.10.3 Reading Data

As soon as the INT flag is set it is possible or necessary to read out the data from PSØ21.

The values HB1 and HB2 are formatted as fixed-point numbers with 16 integer and 8 fractional digits:

Table 20: Data format

HB1 or HB2 ...	
23 ... 8	7 ... 0
16 Bit integer	8 Bit fractional

Reading the integer content of the register, this must be divided by 256:

$$\text{result} = HB \div 256 = Mult \times \frac{\Delta R}{R} \times 10^6$$

Der Wert wird im 2-er Komplement ausgegeben. Er geht damit von -32768 ... +32767.99

Mult1/2 are the multiplication factors defined in register 3 and 11. They have the format of a fixed-point number with 8 integer and 16 fractional digits. 65535 therefore must divide the integer content of register 3 or 11.

$$Mult = Reg3/2^{16} = 0 \ldots 255{,}9999847$$

In case the value of MULT1/2 is 1 the result represents directly the relative change of the resistance, shown in parts per million (ppm). If MULT1/2 is set to the inverse of the K-factor, the result represents the strain in microstrain (µ).

Result's unit:

ppm	for Mult = 1
µ	for Mult = 1/K-factor

Example: 1000µ strain with k = 2 gives 2000 ppm variation of resistance. The data output at full strain and Mult = 1 would be 2000.0.

The multiplication factors additionally have sign bits, to be set in register 10, bits SignMult1 and SignMult2.

SignMultX = 0	positive factor
SignMultX = 1	negative factor

By default the PSØ21 is set to only one multiplication factor (compatibility to PSØ2). The second multiplication factor is activated by setting register 8, bit Mult2EN = 1. In this case the 2nd multiplication factor will be used for the second halfbridge (2nd fullbridge in doublebridge mode).

4.10.4 Stop Measurement

A running measurement can be stopped in two manners:

1. Setting SingleCon Bit

Setting this bit to 1 enables a single measurement only. The PSØ21 is in Single-Conversion Mode. It sets the INT flag after the measurement and then waits for the next command.

For a correct operation it is necessary to leave the other bits of Reg0 at the former values, so that only Bit AutoDis is changing. Internal data like R_{dson} correction values and gain correction values are saved. But switching again to Automatic measurement, it may occur that these internal correction values drift at the beginning and that it takes some measurements to get again the right correction values.

2. INIT

While a measurement is going on, it is possible at any time to send opcode 0xC0 (INIT), which will stop the measurement immediatedly. Without setting the INT flag, PSØ21 is in a wait state. All internal correction values will be deleted (e.g. Rdson correction value). Only the values of the write register are not changed.

5. Details and Special Functions

5.1 Calibration in Measurement Range 2

In measurement range 2 the TDC unit uses a predivider for time interval measurement. It is necessary to calibrate the high-speed unit of the TDC. This is done by the PSØ21 itself and can be controlled through several parameters:

5.1.1 CalDel

Controls the point in time of the calibration in measuring range 2. The calibration measurement is done during the discharge phase. CalDel gives the number of periods of ClkHS between start of discharging and start of calibration measurement:

CalDel	# of ClkHS periods
0	don't use this
1	4
2	5
3	6
4	7 (default)
...	...
15	18

A calibration takes 4 clock cycles. So the calibration has finished 8 to 22 clock periods after the discharging has started. Working with a 4 MHz clock this would be 1 µs to 5.5 µs (default: 2 µs).

It might be necessary to reduce this time in case the measured time interval is shorter than the time needed for calibration. This might happen only at very short measuring times. We recommend to change the default values only in these cases.

5.1.2 CalcCycle

Gives the number of cycles in between calibration measurements. This number has strong influence on the current consumption. The number is set in Bits CalCycle[3:0] of register 2:

CalCycle[3:0]	# of cycles between calibrations
0	1
1	2
2	3 (default)
...	...
15	15

Using high values of CalCycle may reduce the current consumption of the PSØ21 core by 15-20%.

5.1.3 CalcAvRate

Averaging can reduce the noise of the calibration values themselves. The averaging factor is set by Bits CalAvRate (23:22] in register 0:

CalAvRate[1:0]	Averaging factor
0	off
1	8
2	32 (default)
3	64

It is recommended to use the default value.

5.2 Rdson-Compensation

During the discharge of the capacitor the single resistors of the strain gage lie in series with the switching transistors of the PSØ21. The switch-on resistance (= Rdson) of these transistors as well as their temperature dependence and supply voltage dependence are added as a failure to the measurement result. The Rdson itself is in the range of 3 – 5 Ω. The variation over temperature and voltage is in the range of 1 Ω. It can be easily seen that this is bigger than the initial measurement signal of a 350 Ω SG! The **PICO**STRAIN measurement principle is enhanced only with the patented compensation method for the Rdson.

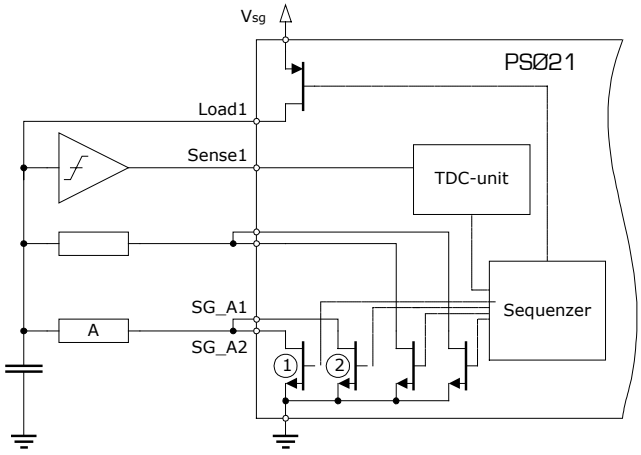


Figure 28: Rdson compensation

For compensation the switch is split into two transistors. For each SG resistor the capacitor is discharged 3 times, through transistor 1, through transistor 2 and

finally through both transistors in parallel. The PSØ21 intrinsic DSP calculates the correction R_{dson} correction value from these three data.

5.2.1 RdsonAVRate

The Rdson compensation can be further settled by averaging. Bits RdsonAVRate set the averaging rate in potentials of 2:

RdsonAVRate	Averaging factor
0	1
1	2
2	4
...	...
15	32,768

The higher the averaging rate the less noisy is the correction value, but the slower is the adaptation to changes. It is recommended to use the default values. At high update rates also higher values for the AVRate can be used.

5.2.2 RdsonModify

This value speeds up the adaptation of the R_{dson} after an INIT. We recommend using the default value ‚4'.

5.2.3 RD1, RD2

RD1 and RD2 offer the possibility to write R_{dson} correction data from earlier measurements back into the chip. The measurement starts with the data from this earlier measurement. The correction values themselves are given in read registers 6 and 7.

5.2.4 RdsonSimple

Setting Bit 21 in register 0, RdsonSimple, reduces the R_{dson} compensation to a simplified mode with reduced calculation effort. This will reduce the precision of the result. Nonetheless the temperature compensation is not too bad and may be sufficient for several applications. With RdsonSimple the noise is slightly improved. With regard to high temperature stability we recommend to use the full R_{dson} compensation.

5.3 Temperature Measurement

The K-factor of strain gages depends on temperature and decreases with higher temperature. If the temperature of the strain gage is known, it is easy to correct for the main failure (active temperature compensation).

PSØ21 offers the option of temperature measurement with an external temperature sensitive resistor. The accordant pins are:

Name	**# Pin**
PT1	29
PT2	30
SenseT	31
LoadT	32

The external circuit is shown in Figure 29.

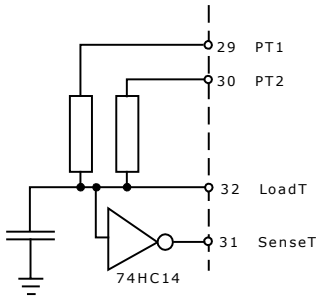


Figure 29

Basically the temperature measurement is nothing more than a simplified SG measurement at separate ports. A measurement takes 2 discharge/recharge cycles and is done once per measurement sequence.

In the first cycle the capacitor is discharged through the resistor connected to pin PT1. This pin should be connected to the temperature sensitive resistor. The nominal value of the resistance should be minimum 500 Ω.
In the second cycle the capacitor is discharged through the resistor connected to pin PT2. This should be the temperature stable reference resistor.

The result is given in register 2, Bits 0 ... 15 as ratio R_{PT1}/R_{PT2}.

The format of the result is a fixed-point number with 2 integer and 14 fractional digits.

Table 21: Data format temperature measurement

Temp	
15 ... 14	13 ... 0
2 Bit integer	14 Bit fractional

Therefore the integer content of the register must be divided by 2^{14} = 16348.

$$\frac{R_\vartheta}{R_{ref}} = Temp = \frac{Reg2}{16348}$$

5.3.1 Precision of Temperature Measurement

The same measuring unit is used for both, the temperature measurement and the strain gage measurement. Thanks to the high quality of this measurement there are no relevant errors introduced to the temperature measurement. The precision is limited by the quantization of the result.

The quantization error of the temperature measurement is $1/2^{14}$ = 61 ppm. A temperature dependent platinum resistor shows a sensitivity of about 3920 ppm/K. In this case the resolution of the temperature measurement would be about 0.015 °C, which is absolutely sufficient for the purpose of SG measurement.
Of course other types of temperature can be used, too, for example KTY... . They typically show even higher sensitivity, which will further improve the resolution.

Some care is necessary with NTCs. They drastically change their resistance with temperature. At high temperatures the discharge time might fall short of the minimum time interval for the TDC unit (about 1.5 µs in measurement range 2). This will produce a timeout of the PSØ21. When using NTCs this must be checked in advance.

5.3.2 Dimensioning

Maximum one cycle time is available for temperature measurement. Further the temperature-depending resistor significantly changes its value, e.g. 80 % at 100 °C increase of temperature with KTY ... and 40% at 100 °C with platinum resistors. At nominal resistance (25 °C) the measurement time should be at maximum half of the cycle time. The reference resistor should be of the same value as the nominal resistance of the sensor.

Example 8:

Temp. resistor:	KTY82 with 2kOhm
Reference resistor:	2 kOhm metal film 50 ppm/K
Cycle time:	30.5µs

Selected discharge time: ≈ 10 µs
From that the value for the charging capacitor is:
C = Tmeas/(0.7*Rnom) = 7.1 nF

The choice is 6.8 nF.

The frequency of the temperature measurement is set in Bits TempRate[1:0]:

TempRate	Frequency
0	Of
1	Each measurement
2	Each 6th measurement
3	Each 9th measurement

Typically TempRate should be TempRate=1.

5.4 Auto-Offset

With PSØ21 it is possible to do an automatic offset calculation after the initialization. The offset is then subtracted from the following measurement results.

The control of this Auto-Offset function is done in registers

- SubOffset (REG0, Bit7)
- OffsetAvRate (REG2, Bit4-6)

SubOffset = 1 enables automatic offset subtraction.

OffsetAVRate gives the number of measurements to be used for offset calculation. For applications operating in double bridge mode avaraging is not recommended and OffetAVRate has to be set to zero.

OffsetAvRate	# of measurements
0	1
1	2
2	4
3	8
...	...
7	128

When working in Single-Conversion Mode together with SubOffset =1 the PS021 doesn't generate an interrupt after a single offset measurement. For this reason each offset Measurement has to be started by calling opcode StartM, followed by a sleep for the duration of the measurement (recommended 16*AVRate*Tcycle).

Example 9:

That means that if the OffsetAvRate is set to 3 then the opcode StartM has to be sent 8 times to finish the measurements for offset compensation and once more to start the real measurement.

5.4.1 Warm-Up

Warm-Up introduces dummy measurement which are executed only after an INIT or Power-on reset. Depending on the measuring mode and, more important, de-

pending on the kind of capacitor selected, it might happen that there is an additional offset in the range of several ppm at the start of the measurement. With AutoOffset this might give a slightly wrong offset value. To avoid this effect warm-up measurements are required to preload the capacitor.

Warm_Up	# of dummy cycles
0	0
1	16
2	32
3	64
...	...
7	1024

5.5 Computing time ALU

PSØ21 has two internal arithmetic units. With respect to the total computing time it might be necessary to introduce fake measurements. The total computing time depends on

- Halfbridge or fullbridge
- Speed settings ALU

Speed settings:
By default both ALUs are set to speed option 1. We recommend not changing these settings. The values 2 and 3 for the speed are for security only and without any influence on functionality. The computing times of the ALUs will be increased. Speed option 0 speeds up the ALUs by about 30 %, but it is not recommended to use this, a malfunction will result.

Taking the default values the total computing time of TALU +BALU is:

Computing time @ 3.3V

	typ. (3.3 V, 25 °C typical process)	worst (3.0 V, 85 °C worst case process)
Halfbridge:	t.b.d. µs	t.b.d. µs
Fullbridge:	t.b.d.µs	t.b.d. µs

Computing time @ 2.5V

	typ. (2.5 V, 25 °C typial process)	worst (2.25V, 85 °C worst case process)
Halfbridge:	t.b.d. µs	t.b.d. µs
Fullbridge:	t.b.d. µs	t.b.d. µs

5.5.1 MFake

By the MFake register it is possible to introduce fake measurements, carried out after a reset, without a data post-processing.

Reason for MFake measurements:
PSØ21 has 2 independently working ALUs. Both of them have access to one and the same RAM. At the end of a complete measurement sequence and before the interrupt is set, it may happen that both ALUs try to access the same RAM. This conflict may cause an error in the calculation and will lead to wrong results.

In any case of such a conflict this will be indicated in the status register Bit ERROR-DSP (Bit19, REG2).

To avoid such a conflict it is possible to introduce fake measurements to avoid access to RAM of both ALUs simultaneously. Whether fake measurements are necessary or not depends on the configuration of the PSØ21 (half- or fullbridge) and the supply voltage.
Fake measurements will be necessary (MFake 0) if the total computing time TALU BALU is longer than the cycle time.

Especially when working with short cycle times it may be necessary to introduce more than one fake measurement. At maximum 4 fake measurements (4 cycles, MFake = 3) can be introduced.

Mfake	# of inserted fake measurements
0	0
1	1
2	2
3	4

5.6 Current Consumption

The current consumption of the total system is split into 2 main elements:

- Current through SG
- Current through core of the chip

Both elements together are the biggest consumers. Their current consumption can be varied in a wide range.

There are further current drains with low but nearly constant current like

- Comparator
- Oscillators etc.

For most current calculations they are not relevant.

5.6.1 Current into Strain Gage

This depends on

- Charging capacitor
- No. of charging cycles per second (cycle time)
- Supply voltage

The current into the strain gauge doesn't depend on the measuring mode.

The current is calculated as

$$I_{strain} = N_{cycles} \times C_{load} \times (k_{SG} \times V_{io} + k_{IO} \times R_{SG})$$

$$I_{strain} = \frac{f_{Cycle}}{CycleTime} \times C_{load} \times (k_{SG} \times V_{io} + k_{IO} \times R_{SG})$$

Putting the frequency and the CycleTime register value into the formula gives the current into the strain gage.

Factor k_{SG} includes the current into the strain gage.

Factor k_{io} includes the current into the I/O section of the PSØ21 and the AC current into the comparator. k_{io} depends on the voltage and the operating mode. Looking at the mode there is a difference between half- and fullbridge mode alternating on one side and fullbridge mode one-sense on the other side.

The following data refer to the recommended comparator circuit.

Factor k_{sg} for the strain gauge:

$$k_{SG} = 0.55$$

The I/O current is dominated by the current through the comparator. The following data are based on the recommended circuit for a switched comparator.

Factor k_{IO} for the I/O current:

Table 22: k_{IO}

IO-Voltage/V	Estimated
5	210 µA
3,3	140 µA
3,0	120 µA
2,5	70 µA

Example 10

R_{SG}	= 1 kOhm
f_{cycle}	= 4 MHz
CycleTime	= 2000
V_{IO}	= 3.3 V
Halfbridge mode	

$$I_{strain} = \frac{4MHz}{2000} \times 68nF \times (0{,}55 \times 3{,}3V + 140\mu A \times 1000\Omega)$$

$$I_{strain} = 265\mu A$$

As part of the 265 µA I_{strain}, about 246 µA flow into the strain gage and 19 µA into the I/O section of the chip and into the comparator. The current into the SG doesn't depend on the supply voltage.

The result is a very good approximation for a circuit based on the recommended comparator.

5.6.2 Current into PSØ21

The current into PSØ21 itself depends strongly on the mode in use, measurement range 2 or measurement range 1. In general the current depends on the core supply voltage.

Measurement range 2:

$$I_{PS021} = I_{PS021}(0) \times \frac{f_{cycle}}{CycleTime}$$

In measurement range 2 the current into the high-speed unit of the TDC is drastically reduced. Thanks to the predivider the high-speed unit is not active over the total measurement time.
$I_{PSØ21}(0)$ is the reference current of this measurement range (Be aware of the engineering units used !!!) . The reference current strongly depends on the divided clock (ClkHS/ClkHSDiv), because this one controls the TDC calibration as main consumer.

For different voltages the current in measurement range 2 is:

ClkHS / ClkHSDivn = 4 MHz:

$I_{PSØ21}(0)$ @ 3.3 V: 33.6 nAs
$I_{PSØ21}(0)$ @ 3.0 V: 28.3 nAs
$I_{PSØ21}(0)$ @ 2.5 V: 19.8 nAs

ClkHS / ClkHSDiv 2 MHz:

$I_{PSØ21}(0)$ @ 3.3 V: 50.7 nAs
$I_{PSØ21}(0)$ @ 3.0 V: 42.1 nAs
$I_{PSØ21}(0)$ @ 2.5 V: 28.7 nAs

With higher clock frequencies the time for calibration is shorter and therefore the current into PSØ21 is lower.

Save current by controlling the number of calibrations

In Measuring range 2 the current consumption of the PSØ21 doesn't depend on the discharge time but on the cycle time. About 40 % of the current is needed for calibrating the TDC. The above-mentioned values are based on calibration after each measurement. If at all this is necessary only for very long cycle times in the range of milliseconds. Mostly the calibration rate might be reduced. The setting is done in Bits CalCycle[3:0] of register 2.

CalCycle[3:0]	# of cycles between calib.
0	1
1	2
2	3
...	...
15	15

Taking a cycle time of 30.5 µs it is in general sufficient to calibrate every tenth measurement. With this setting the current into PSØ21 can be reduced by 35 %. For example, at 2.5V and 4 kHz update rate the current into PSØ21 would be about 430 µA.

5.6.3 Other Current Drains

These are

- Oscillators
- Comparator quiescent current (without switch-off)

Oscillators:
The 32 kHz oscillator, if in use, needs about 3 µA @ 3 V (about 4 µA @ 3.3 V).

The high-speed oscillator needs about
180 µA @ 4 MHz / 3.3 V,
150 µA @ 4 MHz / 3.0 V,
100 µA @ 4 MHz / 2.5 V,

based on the recommended circuit.

The average oscillator current can drastically be reduced by switching-off option in single-conversion mode.

Comparator:
The comparator needs about 180 µA quiescent current at 3.3 Vsg. This can be reduced to approximately 0 by the switched comparator option. Without using the switch-off option the current is constant and proportional to the voltage. It is about 1.4 times more than the Kio value. The Kio term in example 9 is replaced by this current. In any case it will be higher than with the swith-off option.

5.7 Port Switch

PSØ21 allows a free configuration of the driver ports. This allows a fine-tuning of the temperature dependency by referring pairs of nice matched driver ports to e.g. one halfbridge.
Another option is to use all 4 ports in applications with one halfbridge only, driving each SG resistor by two ports. So it is possible to connect SG resistors with less than 350 Ohm.

The settings are done in register 8:

PortSw1<1,0>	Pins 48, 47
PortSw2<1,0>	Pins 45, 44
PortSw3<1,0>	Pins 41, 40
PortSw4<1,0>	Pins 38, 37

The reference port is set by:

PortSwX	Port#
00	SG_A1, SG_A2
01	SG_B1, SG_B2
10	SG_C1, SG_C2
11	SG_D1, SG_D2

The default setting sets the port to the standard pin assignment.

Note:
There are many possible reconfigurations that make no sense (e.g. the same value in all four registers). But it is not possible to destroy the chip by a wrong configuration.

5.8 Quarterbridge

The mathematical formula behind the output data (ppm) in a halfbridge measurement of the PSØ21 output data is:

$$Res = 10^6 * \frac{R_{SG1} - R_{SG2}}{R_{SG1} + R_{SG2}}$$

Using halfbridges or fullbridges where the resistance variation has the same amount but opposite sign shows a linear function of the strain:

$$\frac{R_{SG1} - R_{SG2}}{R_{SG1} + R_{SG2}} = \frac{(R + \delta R) - (R - \delta R)}{(R + \delta R) + (R - \delta R)} = \frac{\delta R}{R}$$

This is the optimum.

In quarterbridges only one resistor is variable. The mathematical calculation introduces a non-linear term (As it happens to A/D converters on a Wheatstone bridge with only one variable resistor).

PSØ21 allows changing the mathematical operation for quarterbridges. By setting register 10, Quarterbridge = "1" the new calculation is:

$$Res = 10^6 * \frac{R_{SG} - R_{ref}}{2 * R_{ref}}$$

This gives a linear function of Rsg. The strain gage resistors have to be connected to ports SG_A or SG_C. The reference resistors are connected to ports SG_B or SG_C.

5.9 Anti Aliasing

In some applications like force sensors it cannot be avoided that there are frequencies in the sensor above the nyquist frequency (= half of measuring rate). These frequencies may introduce aliasing frequencies that falsify the result. With A/D converters this may be suppressed by the introduction of input low-pass filters. This cannot be directly transferred to **PICO**STRAIN principle.

Indeed with **PICO**STRAIN we already have a low-pass filter made of the SG resistors and the discharge capacitor. Limited by the system its 3dB cut-off frequency is in the range 1 to 5 kHz. It cannot be drastically reduced. If this is not sufficient further action is necessary.

One method is to introduce additional noise to the cycle time. This increases the bandwidth of the sampling frequency and suppresses possible sinusoidal interferences. This method is well known from spread spectrum systems and can also be used with **PICO**STRAIN.

Note:
For a successful suppression it is necessary that the clock noise is correlated to the Measurement! Never use an external noisy reference. This would not be correlated to the measurement and would give bad results.

There are two options for adding noise to the cycle time:

1. Single-conversion Mode
In this mode the PSØ21 waits after a measurement for the next external start trigger. Adding noise to the trigger time and so being not straightly periodical shows the above mentioned effect.

2. SpreadEN
PSØ21 has an internal pseudo-random generator for adding noise to the cycle time. It is activated by writing register 8, SpreadEN = "1".

Two further registers control the noise:

SpreadSrc selects the source clock for the random generator.

SpreadSrc	Source clock
0	Each cycle
1	Each 8th cycle
2	Each interrupt
3	Each interrupt

SpreadRng defines the noise range of the cycle time. This value will be added to the initial CycleTime value.

SpreadRng	# of noisy cycles
0	0
1	4
2	8
3	16

5.10 Temp.-compensated Bridges

5.10.1 General comment

The output signal of a SG under load depends on the temperature. For uncompensated bridges it typically increases with higher temperature. The reason is that the temperature dependency of the bridges gain factor (K-factor) cannot be neglected. The same is true for the load cells ε. In the following we call this "span error".

A further failure source is the unavoidable tolerance of the SG resistors. Without any matching or trimming this gives a non-zero output signal with no load. In the following we call this "offset error".

A common method to reduce the span error is to introduce one or two series resistors into the power supply line of the bridge. These series resistors have a temperature drift that is opposite to the span error. E.g. with increasing temperature these resistors increase by value and reduce the efficient bridge supply voltage, keeping the output signal constant. This method shows good results for a limited temperature range (e.g. -10°C to 40 °C). Therefore it is necessary to adjust the compensation resistors precisely to the SG and load cell.

The bridge output voltage has to be trimmed precisely to o without load. Otherwise the span correction will introduce an additional temperature-dependent offset

error because the reduction of the effective bridge voltage would also reduce the offset voltage. A purely mathematical corrected (µC) offset voltage would vary with temperature. It easily happens that this drift is not acceptable.

5.10.2 PSØ21 – New facilities

The PSØ21 offers a very elegant method to correct for the span and offset compensation. This is based on the fact that the PSØ21 separates span and offset compensation and can measure directly the span compensation resistor.

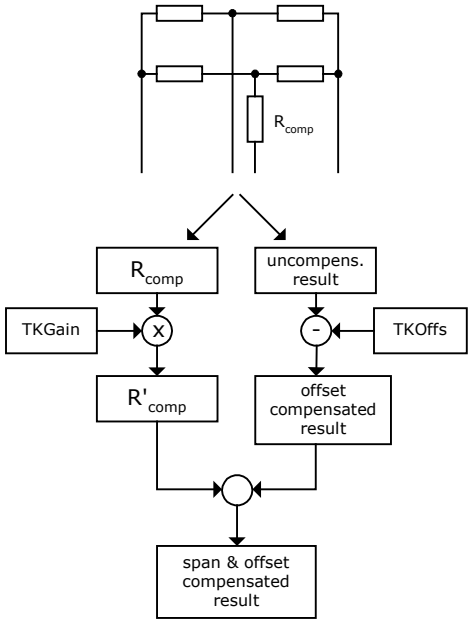


Figure 30

Span resistor

The PSØ21 measures the value of the span resistor and allows modifying the value and the direction of this value by multiplication with register values. So it is very easy to fit adjust this resistor by software to the sensors behaviour. This feature opens up a lot of possibilities for correction and simplified production of the sensor/load cell. Higher quality and lower production costs will be the consequence,

New facilities are:

- Make a good compensated load cell from a bad compensated one without modifying the load cell.
- Simplify production by waiving of the fine tuning of the span resistors, doing this later by software
- Increase the yield of your production

Offset compensation

The PSØ21 is able to separate the offset error from the span error. It has a register for the offset error of the non-loaded sensor. This value is not used in the span compensation and keeps constant even when the span resistor changes. In consequence it is not necessary to make zero adjust for the bridge at all. The only thing to be done is to measure the offset with no load.

This feature, too, simplifies the sensor production, increases the quality and lowers the costs.

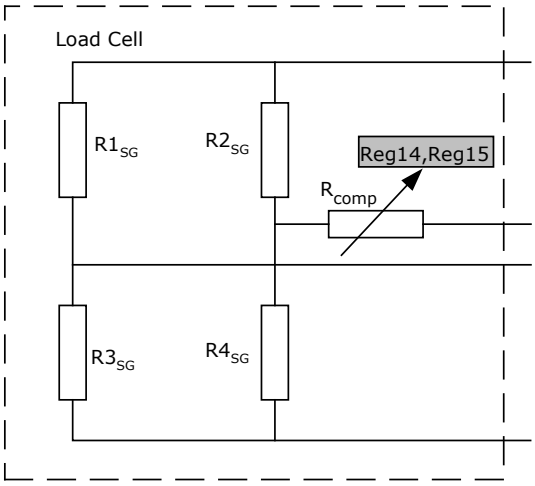


Figure 31

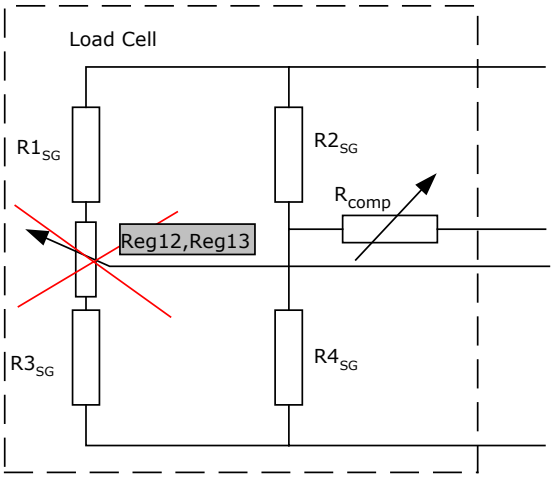


Figure 32

Span and offset compensation are possible in all full-bridge modes. In doublebridge mode each fullbridge

has its own factors for span and offset. Those features are not available in halfbridge modes.

Note:
This method can be used only when just one compensation resistor is used on the load cell. It does not work with two compensation resistors, one in each supply line.

5.10.3 Configuration of Span Compensation

Option 1:
Register 10:
ModRspan = 1
ModSpanByT = 0

This is the standard option. The PSØ21 measures the span compensation resistors and multiplies them with the factors TKGain1 (register 14) and TKGain2 (register 15). TKGain1 is used for the fullbridge mode. In doublebridge mode TKGain1 is used for the first fullbridge, TKGain2 for the second one.

TKGainX are 24 Bit fixed point numbers with 8 integer and 16 fractional digits. The range for the multiplication factors is therefore 0 to 255.9999. Of course reasonable values will be in the range of 1. On the other hand it is possible to bypass the span compensation resistor by setting TKGain = 0.

Option 2:
Register 10:
ModRspan = 1
ModSpanByT = 1

Now the PSØ21 uses the result from the separate temperature measurement instead of the compensation resistors. The initial span compensation resistor which is typically mounted on the load cell is no longer effective. While in option #1 the measured compensation resistor is corrected by multiplication this is different under option #2. The mathematical operation is modified. The measured and uncalibrated strain is multiplied with the factor:

$$K = 1 \pm TKGain \times \frac{R_{temp}}{R_{ref}},$$

The sign (±) is defined by SignMultX.

The compensated result is calculated as:

$$res_{comp} = \left(1 \pm TKGain \times \frac{R_{temp}}{R_{ref}}\right) \times res_{non-comp}$$

In case there is a compensation resistor on the bridge, this one will be eliminated by the internal mathematical calculation and has no compensation effect.

SignMult1, SignMult2
These two bits in register 10 define the sign of the compensation. A negative one will convert e.g. the compensation resistor into a negative resistor with the inverse temperature behaviour. The negative might be a reasonable option when working with a separate temperature measurement.

(Rcomp + Rsg)/Rsg
In case the compensation resistor on the load cell is used and no separate temperature measurement is done, the PSØ21 stores the value (Rcomp + Rsg)/Rsg in the temperature register. Practically this is the temperature value of the load cell. This temperature information can be used in an external µC for an additional temperature compensation calculation e.g. outside the allowed temperature range.

Wheatstone Bridges
When working with existing Wheatstone bridges it is necessary to transform the temperature behaviour of the span compensation from A/D converters to **PICO**STRAIN. This is done by setting the multiplication factors TKGain1 and TKGain2 – the " fine tuning" - to ≈ 0.75 instead of ≈ 1.

5.10.4 Offset Compensation

First it is necessary to measure the offset of an unloaded bridge. To do this set TKGain = 0 and Mult1 = Mult2 = 0.5 (fullbridge and Wheatstone mode). Further set in register 1 SubOffset = 0. Make a separate measurement with a high averaging rate. The result is the bridge offset given in ppm. Write this value into the offset register.

TKOffs are fixed point numbers with 16 integer and 8 fractional digits. The range is

-32,767.000 ppm to +32,767.999.

This corresponds to an offset range of ±163 mV at 5 V supply.

5.11 Multiplication

The PSØ21 has two 24-Bit multiplication registers. This is a comfortable option to bring the measurement

data into the wanted range. It is possible to select multiplication factors so that the result is equal to the value to be displayed in e.g. kg or bar. It is also possible to correct for the varying k-factors of different bridges.

The multiplication factors are 24-Bit fixed point numbers with 8 integer digits and 16 fractional digits. The range is from 0 to 255.9999. The multiplication can be switched on by setting Reg 0, Bit 17: MultEn = 1 and for teh second multiplication factor Reg8, Bit 0: Mult2En = 1.

Working with two multiplication factors:

1. Single Bridge Mode
Mult1 multiplicates halfbridge 1 result
Mult2 multiplicates halfbridge 2 result

This is done also when the PSØ21 puts together the two halfbridhe result to one by means of SumFB or SubFB. The multiplication is done before.

2. Double bridge Mode
Mult1 multiplicates fullbridge 1 result
Mult2 multiplicates fullbridge 2 result

In case the two halfbridge results of one fullbridge are not put together by SumFB or SubFB both halfbridges will be multiplied by the same factor.

5.12 Supply by Lithium Coin Cells

Lithium coin cell batteries are an elegant medium to supply power, possible thanks to the low current consumption of **PICO**STRAIN.

When connecting a **PICO**STRAIN system directly to the lithium coin cell two special register setting are recommended to get the best results:

CalAvRate = 0 (Reg0, Bit 22 to 23)
CalcCycle = 1 (Reg2, Bit 0 to 3)

These settings are necessary because of the relatively high and non-liner inner resistance of a lithium battery. It is important that the PSØ21 gets rapidly adopted to supply voltage variations, especially in single-conversion mode (pulsed load to the battery).

Those settings are not necessary when working with carbon-zinc or alcaline batteries.

6 Special Modes

6.1 Measurement Range 1 for High Update Rates

In measurement range 1 the TDC doesn't work with a predivider, the time interval is measured directly with the TDC's high-speed unit. This one has a measurement range of 2^{20} LSB. The right choice for the charging capacitor should give a discharge time interval of about 140,000 LSB – 350,000 LSB in normal resolution and about 280,000 LSB to 700,000 LSB in high-resolution mode. This is equivalent to 4 – 10 µs. Longer discharge times are not effective. In contrary to measurement range 2 the quality of the measurement result is not limited by the comparator but by the thermal noise of the TDC measuring unit. The resolution in measurement range 1 therefore is not as good as in measurement range 2. It is about 1.5 Bit lower.

The advantage of measurement range 1 is that the user can work with the 32 kHz oscillator only and turn down the high-speed oscillator. The external circuitry is very compact.

Also with respect to current consumption the measurement range 1 shows disadvantages compared to measurement range 2. The current consumption of the TDC is 6 to 8 times higher. Nonetheless, at low update rates and low precision the current can be reduced drastically. Under such conditions the current into the TDC is negligible compared to other current drains (comparator, strain gage).

Measurement range 1 is the first choice in applications with update rates higher than 10 kHz. Taking ClkHS as reference for the cycle time, the maximum possible update rates are in the range of 50 kHz.

6.1.1 Capacitor in Range1

In measurement range 1 the discharge time should be in the range of 4 – 10 µs. According to the recommended comparator circuit the discharge time is given as:

$$\tau = 0.7 * R_{SG} * C_{Load}$$

We recommend the following choices for capacitance:

R_{SG}	C_{Load}
1 kOhm	10 nF
350 Ohm	33 nF

Cycle time:
In measurement range 1 the reference for setting the cycle time can be selected:

HighSpeed = 0 → select 32kHz as reference
HighSpeed = 1 → select ClkHS as reference

6.1.2 Averaging / Resolution

The precision of the result depends on whether the SINC3 filter is in use or not:

The following data are available with AVRate = 1:

Measurement range 1:

Vio	SINC3	Fast Settle
5 V:	5.0 µV	8.7 µV
3 V:	4.6 µV	8.0 µV
2.5 V:	5.2 µV	9.0 µV

Values are given in µV rms noise.

6.1.3 Current Consumption Range 1

The calculation of the current consumption in measurement range 1 differs only with regard to current into PSØ21 from the calculation in range 2. The current into the strain gage is calculated as shown in 5.6.2 Current into PSØ21.

In measurement range 1 the current into the PSØ21 depends linearly on the discharge time of the SG. It is calculated as:

$$I_{PSØ21} = I_{PSØ21}(0) \times 0{,}65 \times R \times C \times f_{cycle}/\text{CycleTime}$$

Here the current depends on the core supply voltage:

$I_{PSØ21}(0)$ @ 3.3 V:	17 mA
$I_{PSØ21}(0)$ @ 3.0 V:	14 mA
$I_{PSØ21}(0)$ @ 2.5 V:	10 mA

The values are remarkably higher than in measurement range 2. The reason is found in the measuring principle of range 1. In this mode, the current draining high-speed unit of the TDC is running for the complete discharge time interval.

6.3 Capacity measurement

PSØ21 offers three ways to measure capacities. They differ in external effort and possible applications.

6.3.1 General Note

It is common to all modes that RdsonAvRate has to be set to „1“ (simplified Rdson compensation) and GainCorRate has to be set to “0” (off, no gain compensation). There is no real need for an Rdson compensation because in capacity measurements the resistor values are much higher. In the third mode there is an additional compensation algorithm that compensates the comparator delay.
It is further common to all modes that a simple 74HC14 comparator is sufficient. There is no need for the bipolar comparator circuit used for strain gage measurements.
For further noise suppresion it is recommended to set in register 10:

LoadStart = 1
LoadSTartDel = 1

Attainable resolution
Due to the manifold variants of circuitry and component data it is not possible to make a generalized statement about precision, as it is possible for strain gage measurements. Generally **PICO**STRAIN shows a performance comparable to high-end electronics. The following data are verified by experiment and shall show the performance of the PSØ21:

Sensor capacity: 50 pF
Signal span: 10 pF

Attainable frequency: 50 kHz
Resolution: 13 ENOB of FS @10 kHz (= 1fF)
20 ENOB of Fs @ 5 Hz (= 10 aF)

The effective resolution goes down from Femtofarad to Attofarad.

Quarterbridge mode
It is reasonable to use the quarterbridge mode (register 10, Quarterbridge = “1”) because a variable capacitor is compared to a fixed reference capacitor. When connecting the measurement capacitor to Port A and the reference capacitor to port B the output function of the PSØ21 will depend linearly on the capacity of the measuring capacitor.

For a linearization it is sufficient to correct the sensor’s non-linearity.

6.3.2 Floating Capacitors

Both capacitors are connected to Vcc and are discharged through one and the same resistor. This mode is used in all applications where the measuring capacitors need not be connected to ground. For this mode set register 1, Cmeasure = “1”. In doublebridge mode all four ports of the PSØ21 are available. It is possible to measure the ratio Csense/Cref of up to 4 sensors.

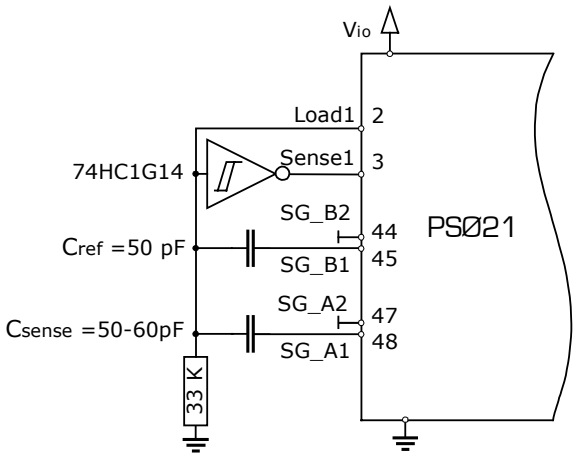


Figure 33

6.3.3 Grounded Capacitors

For grounded capacitors the following circuit should be used:

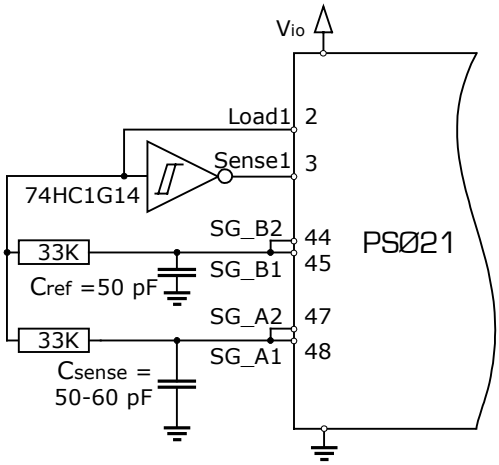


Figure 34

The advantages of this circuit are the simplicity, the fact that the capacitors are connected to ground and the availability of all four ports. The resolution is about 1 Bit less than for the other modes. Also the temperature drift might be higher.
Disadvantage: The capacitors are connected to GND and are discharged through different resistors. It is recommended to use resistors from a voltage divider mounted in one and the same package. The difference in temperature drift of the resistors will affect the total temperature drift.

This mode runs like the usual strain gage measurement. There are no special Bits to be set besides RdsonAvRat = 1, GainCorRate = 0 and StartByLoad = 1. Measurements are possible in measurement range 1 and range 2.

6.3.4 Compensated Capacity Measurement

This third option offers the solution for highest resolution applications with low offset and gain drift.

Here, too, the capacitors are connected to ground. But now they are switched alternately to the resistor by an analog switch. The analog switch is controlled by the PSØ21. Besides SG_A1 the port pins are no longer used and can be connected to ground.

In this mode the PSØ21 has additional compensation algorithms that correct for parasitic capacities and the comparator propagation delay. Parasitic capacities might have a negative influence especially on the temperature drift of the circuit. For a correct compensation measurement it is necessary to use an analog switch with disable function. This circuit minimizes the gain and offset drift.

This mode allows only one pair Csense/Cref. PSØ21 is to be set to halfbridge mode. The resistor R could also be connected to GND, but connecting it to pin 48 as shown reduces the current consumption. The mode is activated by setting register 9, Cmeas2 in the following sub-modes:

Cmeas2 = 0: off
Cmeas2 = 1: on, no compensation, analog multiplexer with disable (e.g. 74LVC2G53)
Cmeas2 = 2: on, with compensation, analog multiplexer with disable (e.g. 74LVC2G53)
Cmeas2 = 3: on, with compensation, using two separate single analog switches (n.o. = normally open)

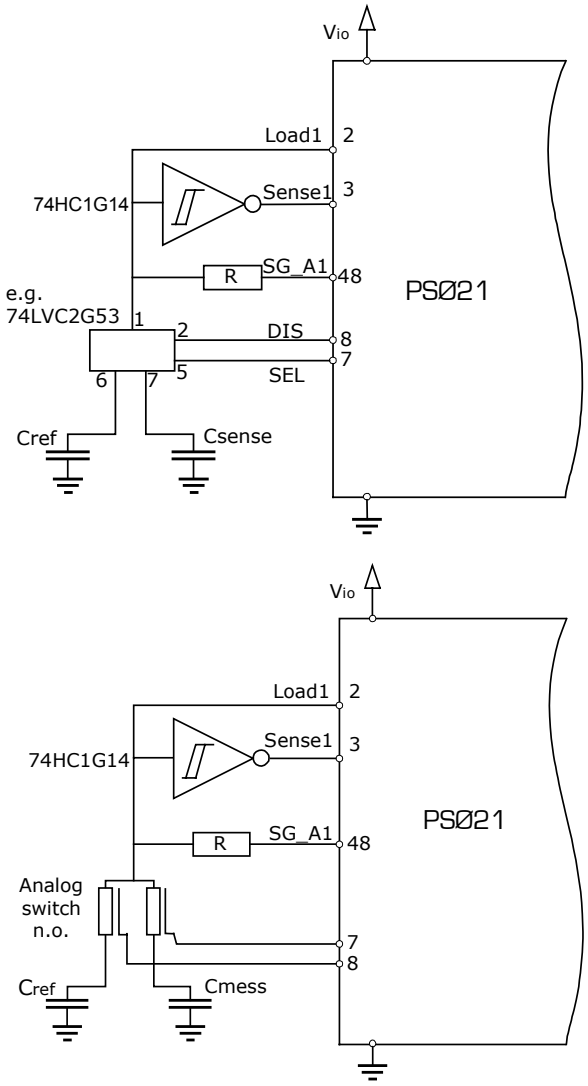


Figure 35

7. How to Get the Best out of PSØ21

PSØ21 is a high-end converter for strain gages and capacitive sensors. One one hand it is possible to make measurements up to 50 kHz; on the other hand it is possible to get a resolution down in the nanovolt range. In this section we summarize some measures the user has to regard when looking at the best performance. It is dedicated to those users that look after the full performance of the PSØ21 and like to profit by acam's experience.

All the precision and drift data in this manual are evaluated with real boards. The measurements have been done with the PSA21 and a 1 kOhm fullbridge modified for **PICO**STRAIN. No idealizations have been done. The measurement results include the noise and drift of the full measurement chain.

7.1 Default settings of adjustment registers

The PSØ21 has some internal registers for slight fine adjustments. After a power-on reset all registers have reasonable settings that already provide very good measuring results. Experiments showed that the results can be further improved by some finetuning as it is described in section 2.9. It is rcommended to use those settings in register 10. Attention should be paid to the fact that there are three different settings for PSØ21_adj1 depending on the update rate and supply voltage. The difference is not very big but can be seen in the data.

7.2 Cycle Time / Measuring Time

The results will be best with a measuring time (discharge time of the capacitor) of 50 µs. Therefore the cycle time should be in the range of 60 to 70 µs, depending on the strain gage resistance. Possible update rates are then:

- 2 kHz in halfbridge mode
- 1 kHz in fullbridge mode
- 500 Hz in doublebridge mode

If the target update rate is not higher than those data we recommend to use this 50 µs discharge time. At higher rates it has of course to be decreased.

7.3 Supply Voltage

Like any other converter for analog signals the PSØ21 has a better resolution at a higher supply voltage. The highest precision will be available with Vsg = 5 V and Vcc = 3.3 V. Nonetheless the circuit can be oprated down to Vsg = Vcc = 2 V. In this case the PSØ21 shows a very convenient behaviour. The absolute noise in nV is constant or even slightly lower at low voltages (see also the tables in 2.4.1 **Measurement Capability**). With decreasing voltage the resolution decreases linearily only in the full specified supply voltage range. This is unique for high-precision converters and is very helpful in bettery operated systems.

If possible, do not use switching regulators, especially no step-up converters. Depending on the device in use this might drastically reduce the precision of the system.

Tip: At devices with low battery voltage (e.g. 2 V with two nearly empty AA cells) connect the PSØ21 directly to the battery. This is much simplier, shows lower cost and shows the better measurement results. The extremly good power supply rejection (PSRR) of the PSØ21 allows even measurements for legal use at this kind of slow but strong variations of the power supply.
The microprocessor can be driven at e.g. 3.3 V supplied by a step-up converter. The PSØ21 SPI interface and all pins related to µC communication have their own power supply Vio. Vio can be set to any supply voltage within the 1.8 V to 5.5 V range independently from the other voltages. Internal level shifters provide a correct operation.

7.4 Reading Data

Reading data in any case is a distortion of the analog-to-digital conversion. This is mainly due to coupling capacities on the printed circuit board. When measuring strain gages these distortions are obvious and reduce the measurement quality especially at high update rates. Nonetheless they are limited as **PICO**STRAIN works with low resistances and high capacities.

When measuring capacities the distortions are much higher because the capacities in use are much lower

and the resolution often is in the atofarrad range. In such application regard the following hints:

There are three ways to avoid a reading during an active measurement:

1. Insert MFake measurements
Sometimes the time interval between the interrupt and the beginning of the next measurement might be not nough to read out the data. Adding up to 4 MFake measurements will prolonges the read time by up to 4 measuring cycles (typ. 65 µs per cycle).

2. Fast read out
It is possible to increase the SPI clock at 3.3 V to 20 MHz. By this measure it is possible to read a 24-Bit data within 1.2µs. In many cases this will be fast enough to not disturb the next measurement. Usually such a fast readout demands a specific hardware. So this is a reasonable solution for high measuring frequencies where the loss in frequency due to the MFake measurements is not acceptable.

3. Single-conversion mode
An intrisically safe method avoiding reading during a measurement is the single-conversion mode. In this mode the PSØ21 stops measuring with an interrupt. The µC can now read the data. After it has accomplished it starts the next measurement by sending a command or by port.

7.5 Board Layout

A good board layout is the basis for a good measurement. Here some hints :

Use a 4-layer pcb with a full ground layer. It is not necessary to separate analog and digital ground. The SPI-bus side of the PSØ21 has its own ground. We recommend to separate this ground from the rest of the ic.

Wire the analog signal lines on different layer than the digital ones. Make sure that the ground layer is between the analog and the digital layer. Don't feed digital lines through the analog part.

Place the high speed-oscillator as close to the PSØ21 as possible. Use the analog layer.

For reference look at the module layouts of the PSA21 evaluation system (see PSA21 datasheet).

7.6 High-speed Oscillator

The high-speed oscillator is part of the measuring chain and the user should have a close look on it. The quality of the oscillation, especially the shorttime jitter effect the measurement. Here some recommendations:

Preferrably use the internal oscillator driver of the PSØ21 and connect it to a ceramic oscillator or quartz. Never use the clock of the microcontroller. His jitter will typically be very bad because of distortions by the µC.

Use frequencies in the range of 4 MHz. By experience they show the best behaviour. Further it is possible to set the optimum measuring time of 50 µs without using the internal clock divider. This has a possitive effect on the measuring quality, too.

It is not necessary to use a quartz. The results won't be better. On the other hand the settling time of a ceramic oscittlator is much less than a quartz' one. An advantage in swichted oscillator applications.

7.7 Noise1 (Reg6, Bit 16)

A "0" in this bit adds some additional time noise for longtime stability of the measurement results. It reduces slow variations in the range 50 to 100 nV. As a disadvantage the noise is increased by about 30%. It depends on the application which feature is the more important one.

8. Applications

8.1 Calibrated Scale

This example describes how to use the PSØ21 so that it provides the resolution that is needed for a calibrated scale.
The scales resolution shall be 3,000 scale divisions (sd) at an update rate of 5 Hz. The load cell has 350Ω resistance and a maximum strain of 500 µ (K = 2). The supply voltage is 5 V for the strain gage (Vsg) and 3.3 V for the PSØ21 (Vcc).

Precision needed:
Looking at the scale's precision, it is claimed that the measurement's noise peak to peak is less than 0.2 scale divisions. Interpreting peak-to-peak as 6 sigma (standard deviation), the standard deviation needed for the measurement is

3,000 sd/0.2 *6 = 90,000 sd eff. at 500 µ or
= 180,000 sd eff. at 1000 µ.

Attainable precision:
Looking at Table 1: Measurement range 2, Vsg = 5.0 V, Vcc = 3.3 V the limit in resolution is found as 26nV noise. In this application the maximum output signal at maximum strain is

$$500\ \mu * 2 * 5\ V = 5\ mV$$

For the effective noise we get

$$5\ mV/90{,}000 = 55.5\ nV$$

This is within the capability of PSØ21.

Cycle Time/AVRate/Resolution:
The discharge time should be about 50 µs. This is roughly the optimum to get the maximum resolution-update rate ratio. From

$$C = t_{mess}/(R_{SG} * 0.7)$$

we get 204 nF for the capacitor. We recommend 2 * 100 nF CFCAP® (Multilayer ceramic Taiyo Yuden).

For the cycle time we select 65 µs. This allows 15,384 measurement cycles per second. In fullbridge mode we need 16 cycles for a single measurement (AVRate=1). This gives us 961 Hz update rate.

To each measurement we add the following actions:

- Gain compensation 1 cycle
- Mfake = 1 1 cycle
- Temperature measurement 2 cycles

So we have 4 additional cycles per single measurement. We get exactly 5 Hz when we select

AVRate = 961/5 – 4 = 192 – 4 = 188.

Getting the maximum performance:
When we look again at Table 1: Measurement range 2, Vsg = 5.0 V, Vcc = 3.3 V we find at 1 kHz update rate, which is approximately AVRate =1, a noise value of 440 nV. We need 55 nV, so we have to improve the noise by a factor 440/55 = 8. The AVRate must be increased by the square of this value, which is 64. Taking this value we get an update rate of approximately 15 Hz.
Of course, besides these pure mathematical and theoretical calculations, we have to consider some practical aspects like a good board layout. Therefore this calculation can be taken as approximation only. But all calculations show that the measurement task in this application can easily be covered by PSØ21. The maximum update rate will be at about 15 Hz.

To minimize the temperature-offset drift of the electronics we connect the two halfbridges in a way that we get the difference between them.

Further assumptions are:

- The offsets calculation is done in the microprocessor
- A temperature measurement is done with a KTY82, 2 kΩ at 25°C
- The result is calculated directly in the PSØ21 (30 kg scale, display in 10 gram/sd)
- Bridge output is exactly 2.15 mV/V, Rspan ≈ 30 Ohm
- ClkHS is built with a 4 MHz ceramic oscillator. The 32 kHz oscillator is not connected.
- The load cell is a standard cell used already as Wheatstone bridge. Just the wiring was modified.

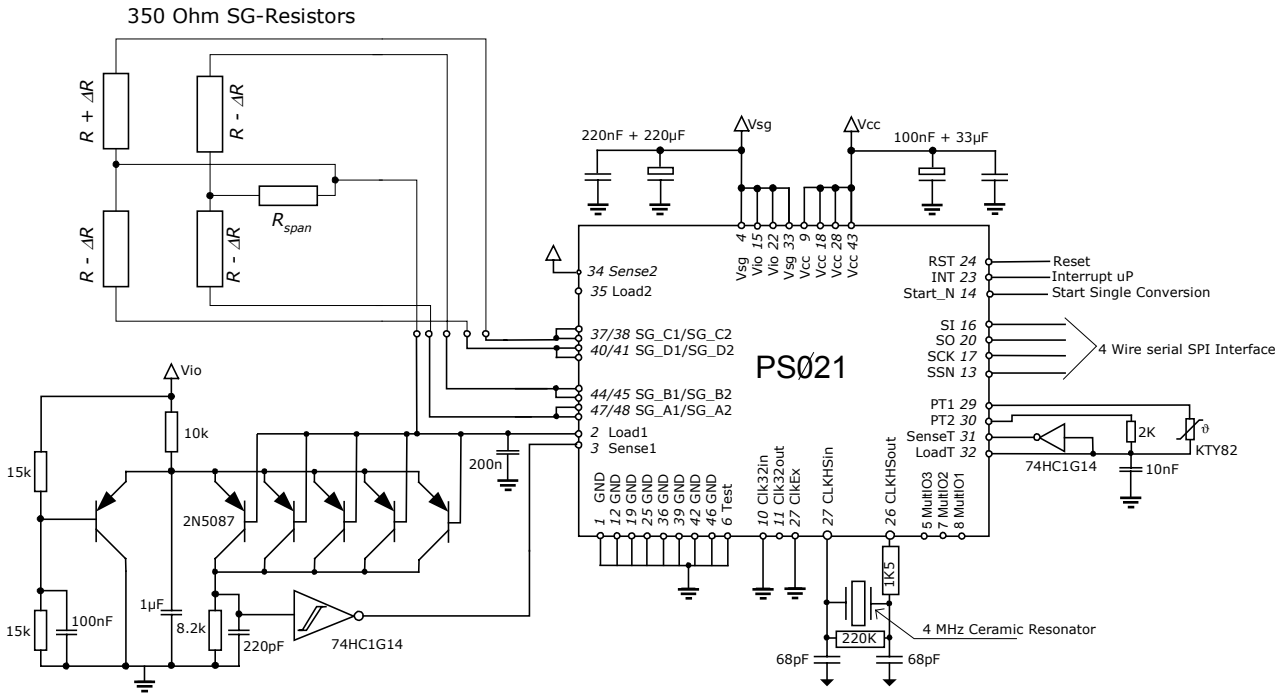


Figure 36

The register settings are the following:

Reg0	Bridge	= 1	Sinc3	= 1	NegSense1	= 0	MultEN	= 1
	HighSpeed	= 1	SubOffset	= 0	NegSense2	= 0	Cmeasure	= 0
	MRange2	= 1	DoubleBr	= 0	SumFB	= 0	ClkHSDiv	= 1
	HighRes	= 1	TempRate	= 1	SubFB	= 1	RdsonSimple	= 0
	SingleCon	= 0	NegSenseT	= 1	SelClk32	= 0	CalAvRate	= 3
Reg1	AVRate	= 188	CycleTime	= 260				
Reg2	CalCycle	= 1	GainCorRate	= 1	RdsonAvRate	= 10		
	OffsetAvRate	= 2	GainAvRate	= 4	RdsonModify	= 4		
Reg3	Mult	= Multiplication factor, to be evaluated in basic calibration						
Reg4	RD1	= 0x800000						
Reg5	RD2	= 0x800000						
Reg6	Mfake	= 1	WarmUp	= 7	s.c. 8, 10, 14, 20, 22 = 1			
Reg7	Use default values, do not write to this register							
Reg8	Use default values, do not write to this register							
Reg9	Use default values, do not write to this register							
Reg10	StartByLoad	= 1	ModSpanByT	= 1				
Reg11	Use default values, do not write to this register							
Reg12	TKOffs1	= bridge offset, see 5.10.4 Offset Compensation for details						
Reg13	TKOffs2	= bridge offset, see 5.10.4 Offset Compensation for details						
Reg14	TKGain1	= correction of bridge temperature compensation (0x010000 if compensation is already fine), see 5.10.3 Configuration of Span Compensation for details						
Reg15	TKGain2	= correction of bridge temperature compensation (0x010000 if compensation is already fine), see 5.10.3 Configuration of Span Compensation for details						

Note 1:
It is not necessary to write into registers 2, 4, 5, 6, 7, 8, 9, 11.

Note 2:
It is necessary to write into registers 12 to 15 when working with compensation. The data in these registers do not make sense after a power-on reset.
TKOffs: Tset TKGain = 0 and Mult1= Mult2 = 0.5. Further set in SubOffset = 0. Make a measurement with a high averaging rate. The result is the bridge offset given in ppm. Write this value into the offset register.
TKGain: If the bridge is already correctly temperature compensated, this value is 1 (write 0x010000 to the register). Otherwise it is necessary to make temperature measurements and take these data to correct TKGain.

Note 3:
This example is made for highest possible resolution. The total current consumption including electronics and strain gage is about 8.5 mA with a 350 Ohm strain gage. This is already a good value. But a closer look shows that the resolution is already 1 Bit better than needed. This surplus in resolution can be used to decrease the current consumption. T do this the AVRate is reduced by a factor 4 to 47 and the cycle time is increased by a factor 4 to 1040. The measuring rate is still 5 Hz but the resolution is 1 Bit less. This measure reduces the current consumption by a factor 4 to 2.2 mA. This is a very low value for scales with 350 Ohm strain gages.

Note 4:
The current consumption of this 3000e OIML approved scale can be reduced to 250 µA !!! at 5 Hz when using a 1 kOhm strain gage with the full span of 2 mV/V. This allows to make very powerful battery driven scales with a battery lifetime of years in continuous operation.

8.2 Pressure Sensor on a 4 to 20 mA Interface

In this example we describe the use of PSØ21 in a pressure sensor application based on a metal strain gage.

The pressure sensor has a 4 to 20 mA interface which has to provide the power supply of the complete sensor electronics. In total 18 mW are available, and the strain gage and PSØ21 is limited to 50 % of that.

The sensor's update rate shall be 1 kHz. The resolution should be as good as possible. The strain gage is made out of a fullbridge with 1 kOhm resistance.

It is recommended to connect the two halfbridges of the fullbridge in a way that the two measurement results are subtracted. This provides the best temperature compensation of the electronic circuit. The temperature drift of the total electronics (incl. comparator) will be in the range of 3 nV/K. You'll achieve better results than required.
The bridge itself is not compensated. It couldn't be compensated by a resistor because of the wide temperature range of –40°C to +85°C. The temperature compensation is done in the microprocessor on the basis of the PSØ21 temperature measurement.

Supply voltage:
The selection is 3 V supply voltage for the strain gage and the PSØ21. Reducing the voltage at the SG drastically reduces the current into the SG. The common supply for core and SG saves external components.

Measurement range:
As we look for maximum resolution and since the update rate is not too high, we select measurement range 2.

Capacitor:
We choose a 62 nF CFCAP capacitor (Taiyo Yuden).

AVRate and Update rate:
The discharge time is about 43 µs. The recharge time should be 2 µs + 62/120 ns = 8.4 µs. The total cycle time therefore should be in the range 51.4 µs. Setting CycleTime = 206 at 4 MHz reference give 51.5 µs. Temperature measurements are made each measurement (TempRate =1). GainCorRate is set to 1.

The only choice for AVRate is 1. According to 4.8 Update Rate this makes 19 cycles for each measurement.
#Cycles/measurement = #Halfbridges*AVRate*8 + GainCorRate + TempRate
#Cycles/measurement = 2*1*8+1+2 = 19

For a fullbridge the update rate is
f_{meas} = 1/(51.5 µs*19) = 1022 Hz

If exactly 1 kHz update rate is required this can be achieved by a slight increase of CycleTime to 210.

Resolution:
The output signal at maximum strain is
2 mV/V * 3 V = 6 mV
According to Table 2: Measurement range 2, Vsg = 3.0 V, Vcc = 3.0 V the effective noise is 0.38 µV. The resolution is then 6 mV/0.38 µV = 15,800 scale divisions or 14.9 Bit. This allows a display of 5000e ± 1.

Operating Current:
1. Current into SG and I/O-section of PSØ21

$$I_{strain} = \frac{f_{Cycle}}{CycleTime} \times C_{load} \times (k_{SG} \times V_{io} + k_{IO} \times R_{SG})$$

$$I_{strain} = \frac{4MHz}{210} \times 62nF \times (0.55 \times 3.0V + 270\mu A \times 1000\Omega)$$

$$I_{strain} = 1.95mA$$

The current into the PSØ21 core is

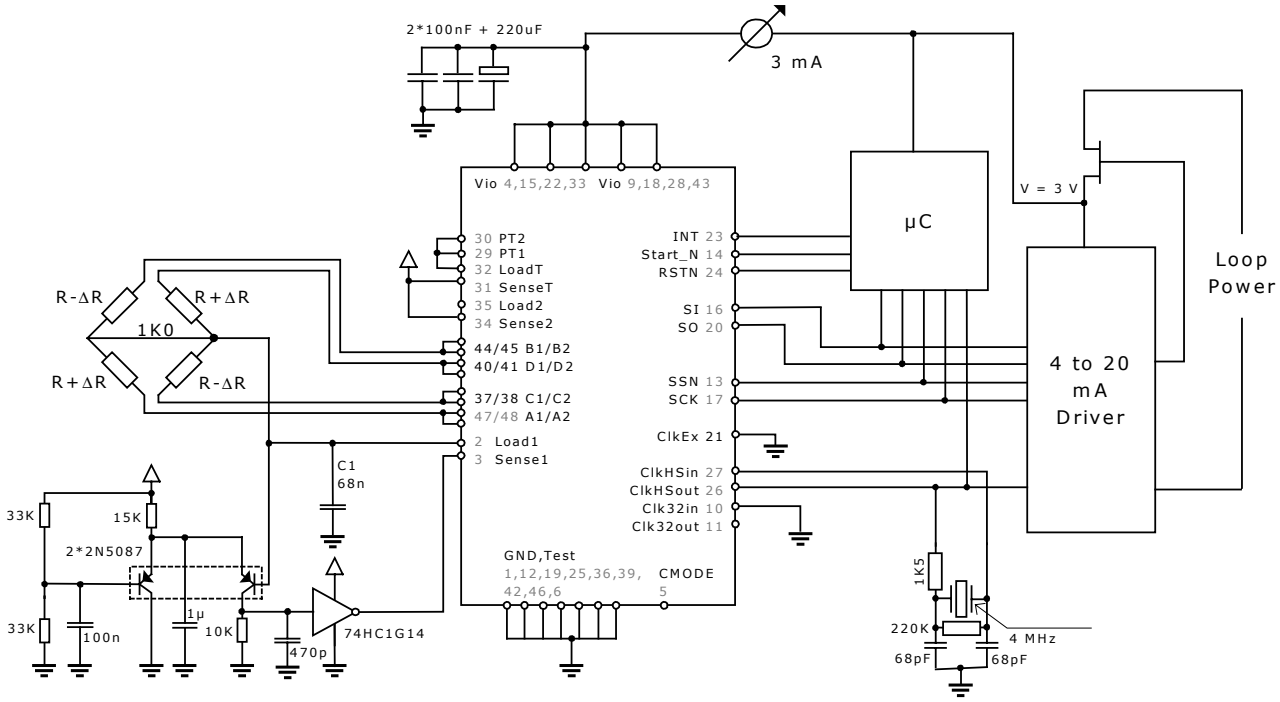
$$I_{PS02} = I_{PS02}(0) \times \frac{f_{cycle}}{CycleTime} = 28.3nAs \times \frac{4MHz}{210} = 539\mu A$$

In this application it is helpful to reduce the core current by reducing the number of calibration cycles by about 20% (set CalCycle = 10). With this action, the core current will be only 400 µA.

The total operating current of the front-end electronics is:

I_{DMS}	= 1.95 mA
I_{core}	= 0.4 mA
I_{komp}	= 0.16 mA
I_{osz}	= 0.15 mA
I_{tot}	= 2.66 mA

The total power dissipation of the front-end electronics is about 8.8 mW, exactly the maximum available.



Further assumptions

- The offset calculation is done in the PSØ21.
- The measurement results are displayed in ppm (µV/V), which is the default setting.
- A 4 MHz ceramic resonator is used for the high-speed clock reference.

The register settings are the following:

Reg0	Bridge	= 0	Sinc3	= 1	NegSense1	= 0	MultEN	= 0
	HighSpeed	= 0	SubOffset	= 0	NegSense2	= 0	Cmeasure	= 0
	MRange2	= 1	DoubleBr	= 1	SumFB	= 0	ClkHSDiv	= 0
	HighRes	= 1	TempRate	= 1	SubFB	= 1	RdsonSimple	= 0
	SingleCon	= 0	NegSenseT	= 1	SelClk32	= 0	CalAvRate	= 3
Reg1	AVRate	= 1	CycleTime	= 210				
Reg2	CalCycle	= 10	GainCorRate	= 1	RdsonAvRate	= 8		
	OffsetAvRate	= 4	GainAvRate	= 4	RdsonModify	= 4		
Reg3	Use default values, do not write to this register							
Reg4	Use default values, do not write to this register							
Reg5	Use default values, do not write to this register							
Reg6	Use default values, do not write to this register							
Reg7	Use default values, do not write to this register							
Reg8	Use default values, do not write to this register							
Reg9	Use default values, do not write to this register							
Reg10	Use default values, do not write to this register							
Reg11	Use default values, do not write to this register							
Reg12	Use default values, do not write to this register							
Reg13	Use default values, do not write to this register							
Reg14	Use default values, do not write to this register							
Reg15	Use default values, do not write to this register							

9. Background Knowledge

9.1 What's a TDC?

The basic inner measuring unit of the PSØ21 is a TDC or Time-to-Digital Converter. Digital TDCs use internal propagation delays of signals through gates to measure time intervals with very high precision.

9.1.1 Measuring Range 1

Figure 37 clarifies the principal structure of such an absolute-time TDC. Intelligent circuit structures, redundant circuitry and special methods of layout on the chip make it possible to reconstruct the exact number of gates passed by the signal. The maximum possible resolution strongly depends on the maximum possible gate propagation delay on the chip. With a basic design of the measuring unit, and using modern CMOS technologies it is possible to achieve about 25 ps resolution.

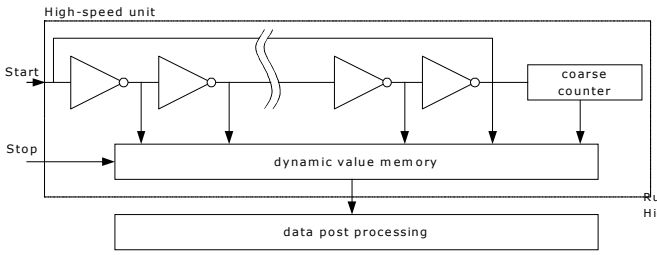


Figure 37

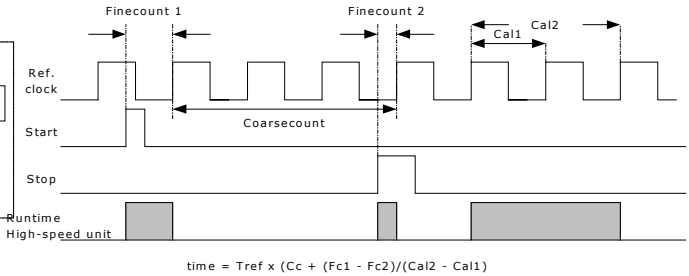
The measuring unit is actuated by a START signal and stopped by a START signal. Based on the position of the ring oscillator and the coarse counter the time interval between START and STOP is calculated with a 20 Bit measurement range.

The Bit size (LSB) is typically 28 ps at 3.3 V and 25 °C ambient temperature. By using a combination of two such circuits the precision of the measurement is doubled. This is called High-Resolution Mode. PSØ21 shows in high-resolution mode 14 ps LSB resolution.

The gate propagation delay times strongly depend on temperature and voltage. Usually this is solved doing a calibration. During such a calibration the TDC measures 1 and 2 periods of the reference clock. When working in measuring range 1 of PSØ21 this is not necessary because the resistance measurement is done calculating the ratio of two measurements.

9.1.2 Measurement Range 2

It is possible to extend the maximum time interval using a pre-divider. The resolution in LSB remains unchanged by that. In this mode the high-speed unit of the TDC does measure the whole time interval but only time intervals from START and STOP to the next rising edge of the reference clock (fine-counts). In between the fine-counts the TDC counts the number of periods of the reference clock (coarse-count).



With regard to the PSØ21 the signal-to-noise ratio can be drastically improved. In addition, the active time of the high-speed unit as the main current drain is reduced remarkably.

As opposed to measuring range 1, in measuring range 2 the result is the sum of different fine and coarse-count results. Therefore it is necessary in measuring range 2 to make a calibration. During a calibration the TDC measures 1 and 2 periods of the reference clock.

Last Changes:

27th June 2005: Section 6.1.1 capacitor values
02nd June 2006: Corrections in section 5.4 and in figure 21, 22 and figure 24

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