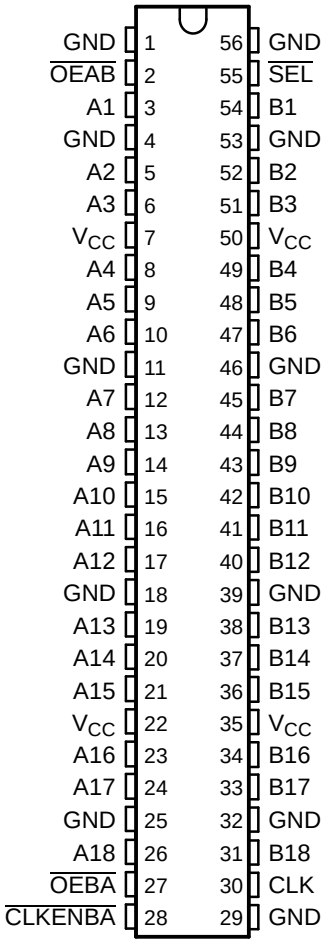
SN74ALVCH16524
18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES080E – JULY 1996 – REVISED OCTOBER 2004

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enable Mode**
- **Operates From 1.65 V to 3.6 V**
- **Max t_{pd} of 3.2 ns at 3.3 V**
- **±24-mA Output Drive at 3.3 V**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DGG OR DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock-enable ($\overline{CLKENBA}$) inputs. For the A-to-B data flow, the data flows through a single buffer. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of the select ($\overline{SEL}$) input.

Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate $\overline{CLKENBA}$ input is low. The B-to-A data transfer is synchronized with CLK.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40 to 85°C	SSOP - DL	Tube	SN74ALVCH16524DL	ALVCH16524
		Tape and reel	SN74ALVCH16524DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCH16524DGGR	ALVCH16524

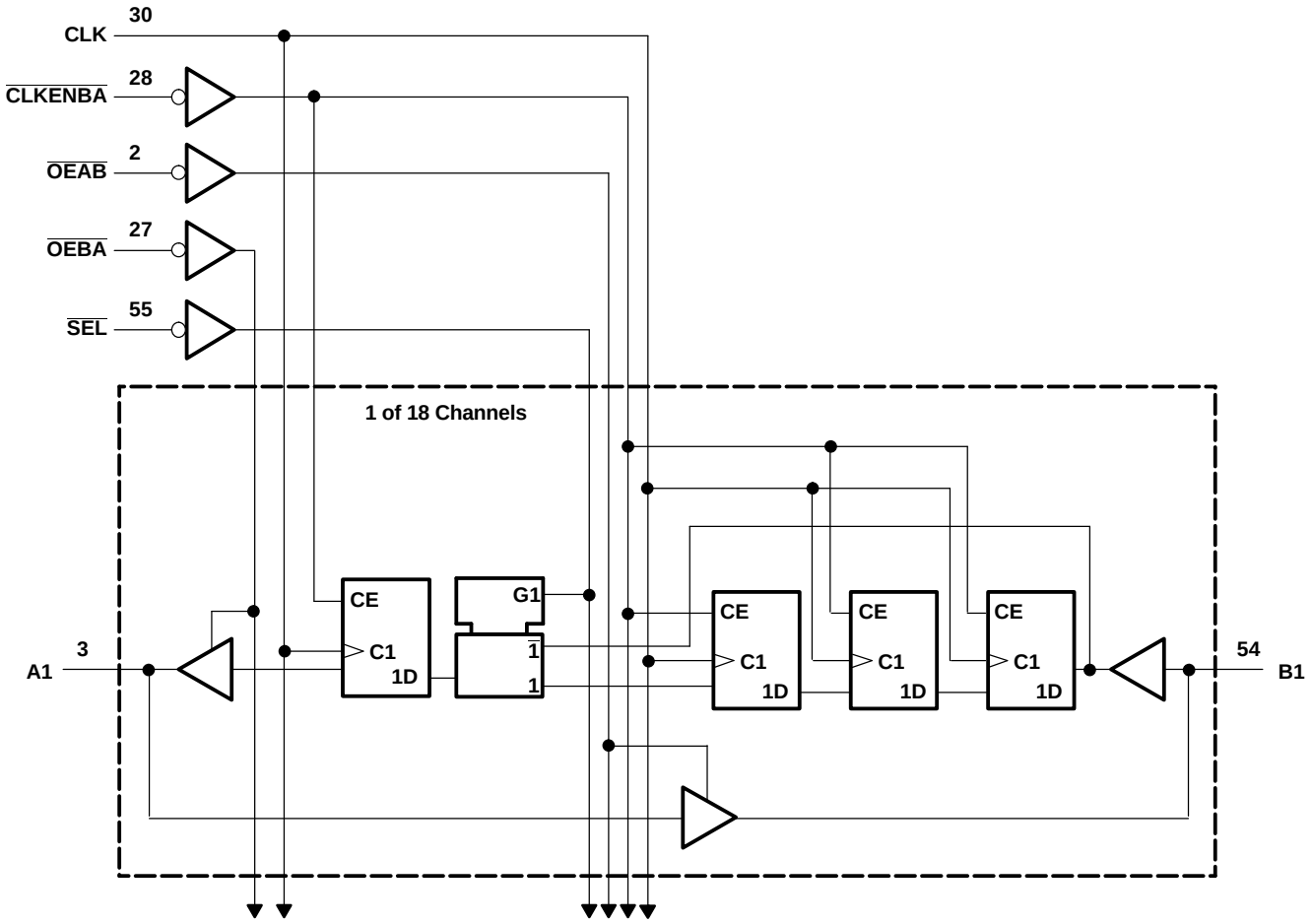
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
B-TO-A STORAGE ($\overline{OEBA}$ = L)

INPUTS				OUTPUT
$\overline{CLKENBA}$	CLK	$\overline{SEL}$	B	A
H	X	X	X	A_0 (1)
L	↑	H	L	L
L	↑	H	H	H
L	↑	L	L	L (2)
L	↑	L	H	H (2)

(1) Output level before the indicated steady-state input conditions were established
(2) Four positive CLK edges are needed to propagate data from B to A when $\overline{SEL}$ is low.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range	Except I/O ports(2)	-0.5	4.6	V
		I/O ports (2)(3)	-0.5	V_{CC} + 0.5	
V_O	Output voltage range(2)(3)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		-50	mA
I_{OK}	Output clamp current	V_O < 0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	DGG package		64	°C/W
		DL package		56	
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		-4	mA
		V_{CC} = 2.3 V		-12	
		V_{CC} = 2.7 V		-12	
		V_{CC} = 3 V		-24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		12	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = -100 µA	1.65 V to 3.6 V	V_{CC} - 0.2			V
		I_{OH} = -4 mA	1.65 V	1.2			
		I_{OH} = -6 mA	2.3 V	2			
		I_{OH} = -12 mA	2.3 V	1.7			
			2.7 V	2.2			
			3 V	2.4			
		I_{OH} = -24 mA	3 V	2			
V_{OL}		I_{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I_{OL} = 4 mA	1.65 V			0.45	
		I_{OL} = 6 mA	2.3 V			0.4	
		I_{OL} = 12 mA	2.3 V			0.7	
			2.7 V			0.4	
		I_{OL} = 24 mA	3 V			0.55	
I_I		V_I = V_{CC} or GND	3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.58 V	1.65 V	25			µA
		V_I = 1.07 V	1.65 V	-25			
		V_I = 0.7 V	2.3 V	45			
		V_I = 1.7 V	2.3 V	-45			
		V_I = 0.8 V	3 V	75			
		V_I = 2 V	3 V	-75			
		V_I = 0 to 3.6 V(2)	3.6 V			±500	
I_{OZ}(3)		V_O = V_{CC} or GND	3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V		3		pF
C_{io}	A or B ports	V_O = V_{CC} or GND	3.3 V		7		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V_{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			(1)		120		125		150	MHz
t_w	Pulse duration, CLK high or low		(1)		3.2		3.2		3		ns
t_{su}	Setup time	B data before CLK↑	(1)		1.5		1.2		1.1		ns
		$\overline{SEL}$ before CLK↑	(1)		2.7		2.4		2.1		
		$\overline{CLKENBA}$ before CLK↑	(1)		2.7		2.6		2		
t_h	Hold time	B data after CLK↑	(1)		1		0.6		1.2		ns
		$\overline{SEL}$ after CLK↑	(1)		0.5		0.2		0.8		
		$\overline{CLKENBA}$ after CLK↑	(1)		0.1		0.1		0.3		

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		120		125		150		MHz
t_{pd}	A	B		(1)	1	3.9		3.8	1	3.2	ns
	CLK	A		(1)	1	6.1		6.2	1	5.2	
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B		(1)	1	6.1		6.1	1	5.1	ns
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B		(1)	1	6.3		5.4	1	4.9	ns

(1) This information was not available at the time of publication.

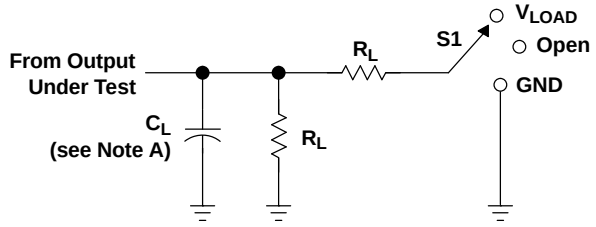
OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	(1)	160	160	pF
	Outputs disabled		(1)	160	160	

(1) This information was not available at the time of publication.

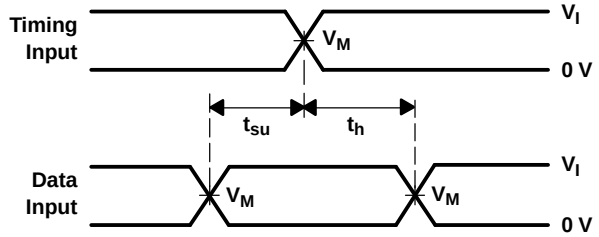
PARAMETER MEASUREMENT INFORMATION



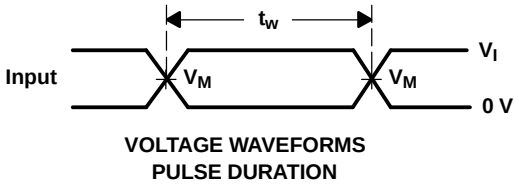
LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open V_{LOAD} GND

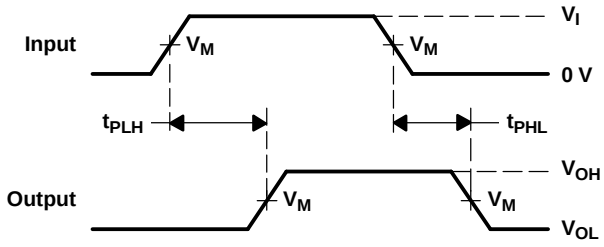
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



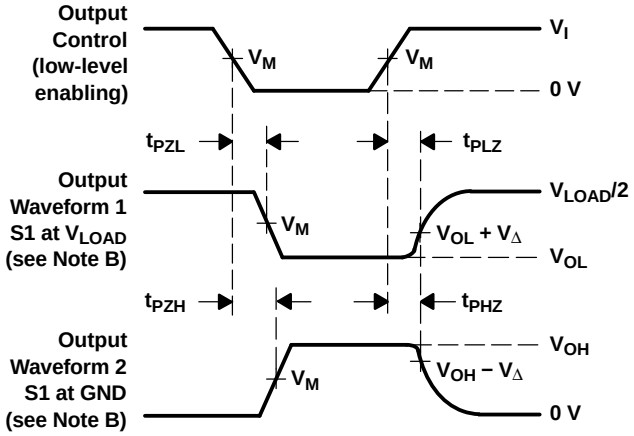
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVCH16524DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16524	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

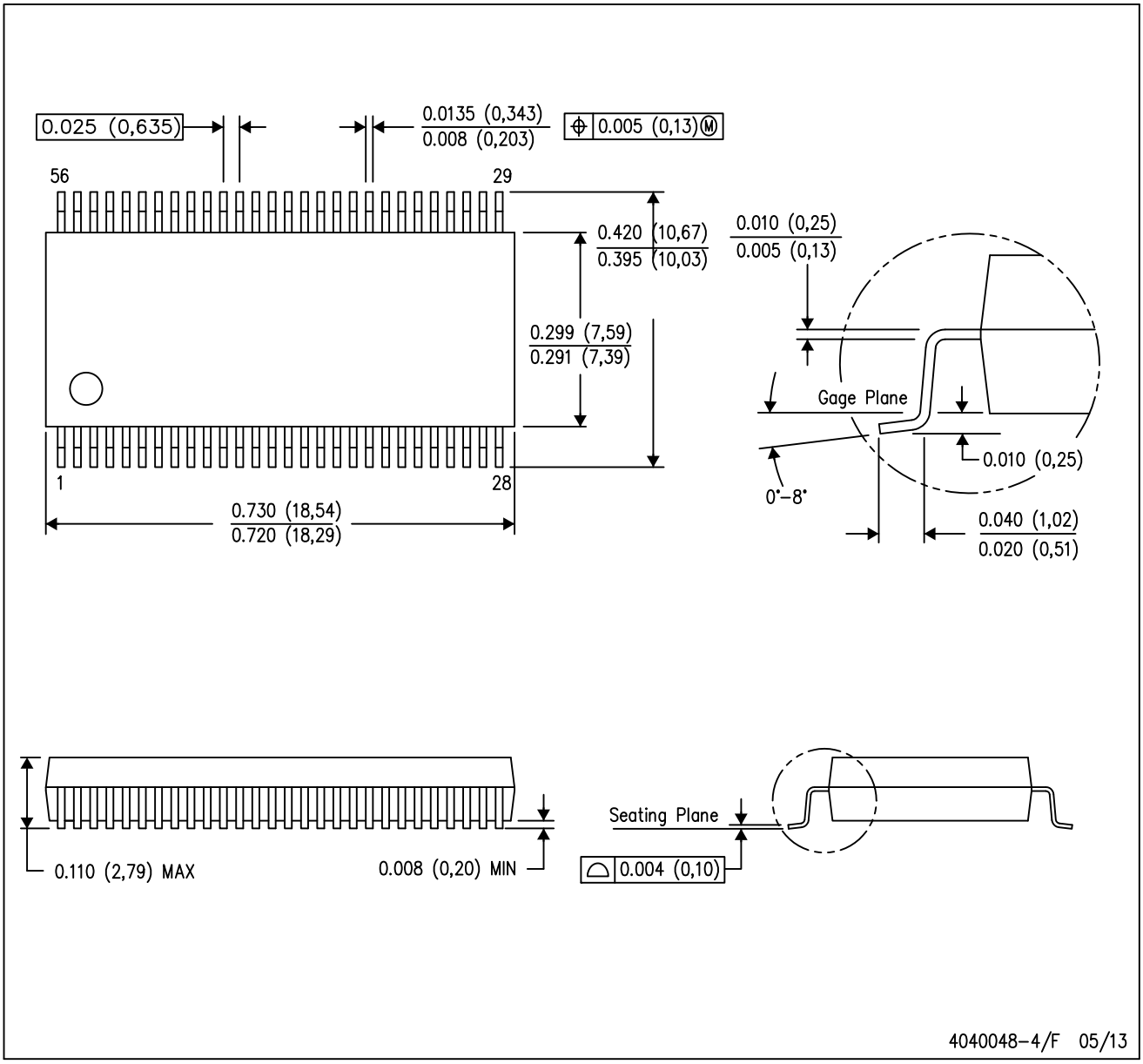
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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