



Click [here](#) for the 3D model.

Dimensions

D	9.845mm +/-0.955mm
L	6.35mm MIN
T	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
A	9.144mm MAX
C	10.16mm +/-0.635mm
E	11.18mm +/-0.25mm
G	1.4mm +/-0.254mm
LO	1.586mm MAX
LW	0.508mm +/-0.051mm

Packaging Specifications

Packaging	Waffle, Box
Packaging Quantity	36

General Information

Series	KPS LDD Comm SMPS
Style	Leaded Stacked Chip
Description	Low ESR, High Current Stacked Ceramic Chips
Features	Low ESR, High Current, High Performance
RoHS	No
Prop 65	⚠ WARNING: Cancer and reproductive harm - http://www.p65warnings.ca.gov .
SCIP Number	4221181d-d71c-4d0a-af45-5eab760732b2
Termination	60/40 Solder Coated
Lead	Wire Leads
Failure Rate	N/A
Testing and Reliability	Commercial
AEC-Q200	No

Notes
 Note: Number of chips in stack depends on design. Number of Chips in this stack = 3. Note: Lead alignment within pin rows shall be within ±0.13 mm.

Specifications

Capacitance	2.2 uF
Capacitance Tolerance	10%
Voltage DC	500 VDC
Dielectric Withstanding Voltage	750 VDC
Temperature Range	-55/+125°C
Temperature Coefficient	X7R
Dissipation Factor	2.5% 1 kHz 25C
Aging Rate	3% Loss/Decade Hour
Insulation Resistance	45.5 GOhms