Low Phase Noise, LVPECL XO (for 70MHz to 170MHz Fundamental Crystals)

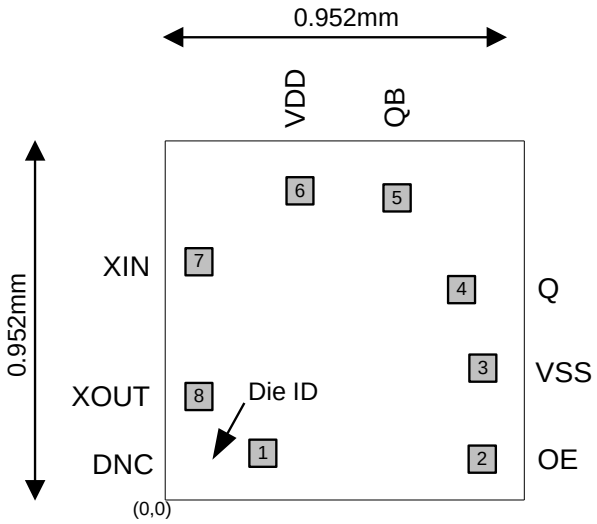
FEATURES

- Advanced non multiplier XO Design for High Performance Crystal Oscillators
- Input/Output Range: 70MHz to 170MHz
- Ultra Low Phase Noise: -163dBc @10MHz at 156.25MHz
- Ultra Low Phase Jitter: <50fs RMS
- Complementary LVPECL Outputs
- Power Supply: 3.3V ±10%
- Available in Die or Wafer Form

DESCRIPTION

The PL686-05 is a non-multiplier XO IC specifically designed for fundamental mode crystals from 70MHz to 170MHz. The phase noise performance, with <50fs phase jitter, makes this an ideal solution for all high end clocking applications such as SONET, WiMax, CPRI, OBSAI, Fiber Channel, and any application where performance and quality are required.

DIE CONFIGURATION



DIE SPECIFICATIONS

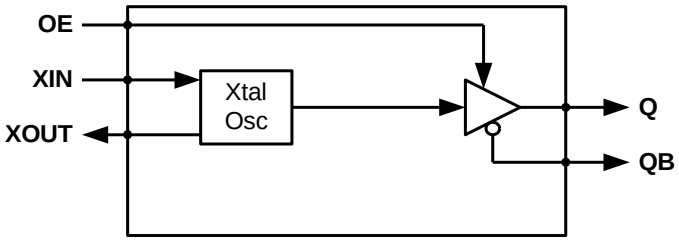
Name	Value
Size	952 micron x 952 micron
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	8 mil

OUTPUT ENABLE LOGIC

OE State (Pad 4)	Output Buffers State
0	Outputs Tri-Stated
1 (Default)	Outputs Enabled

* Internal 60KΩ pull-up resistor

BLOCK DIAGRAM



PAD ASSIGNMENT

Pad #	Name	X (µm)*	Y (µm)*	Description
1	DNC	-194	-365	Do Not Connect
2	XOUT	-372	-190	Crystal output connection
3	XIN	-372	158	Crystal input connection
4	VDD	-117	329	V_{DD} connection
5	QB	140	315	Complementary LVPECL output
6	Q	315	75	LVPECL output
7	VSS	373	-127	GND connection
8	OE	373	-373	Output enable pin. Internal pull up resistor.

* **Note:** Referenced to center of the die.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, DC	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, DC	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	-40	85	°C
HBM ESD Protection		2,000		V

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Fundamental Mode, AT cut	70		170	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$			8		pF
Shunt Capacitance	C_0				2.0	pF
Recommended ESR	R_E	$C_0 \leq$ 2.0pF, up to 135MHz			30	Ω
		$C_0 \leq$ 2.0pF, up to 160MHz			20	Ω
		$C_0 \leq$ 1.5pF, up to 170MHz			20	Ω

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	I_{DD}	Standard LVPECL Loading (See LVPECL Levels Test Circuit, page 4)			65	mA
Operating Voltage	V_{DD}		2.97	3.3	3.63	V
Output Clock Duty Cycle		@ V_{DD} – 1.3V (See LVPECL Transition Time Waveform, page 4)	45	50	55	%
Short Circuit Current				±50		mA

4. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period Jitter RMS	At 156.25MHz, with capacitive decoupling between V_{DD} and GND. Over 10,000 cycles		2.5		ps
Period Jitter pk-to-pk			20		
Integrated Jitter RMS at 156.25MHz	Integrated 12 kHz to 20 MHz		47		fs

5. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	@1MHz	@10MHz	UNITS
Phase Noise, relative to carrier	156.25MHz	-67	-97	-125	-149	-158	-162	-163	dBc/Hz

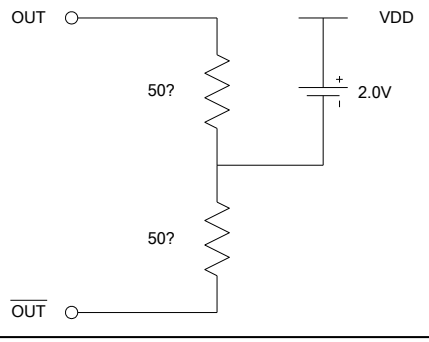
6. LVPECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025	V_{DD} – 0.950	V_{DD} – 0.880	V
Output Low Voltage	V_{OL}		V_{DD} – 1.810	V_{DD} – 1.700	V_{DD} – 1.620	V

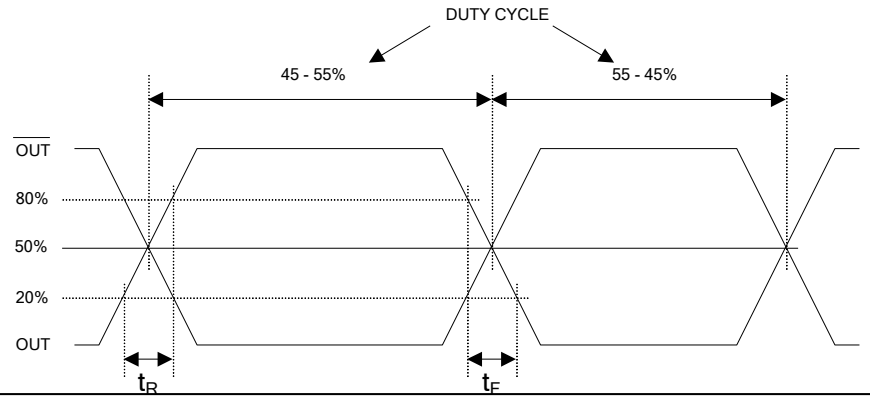
7. LVPECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% of output waveform			300	ps
Clock Fall Time	t_f	@80/20% of output waveform			300	ps

LVPECL Levels Test Circuit



LVPECL Transistion Time Waveform



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL686-05 XX

Part Number

Packaging Option
D = Die
W = Wafer

Temperature Range
C=Commercial (0°C to 70°C)

Order Number	Packaging
PL686-05DC	Die – Waffle Pack
PL686-05WC	Wafer