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APPLICATION NOTE 4118

DS33R11 Multichip-Module BSDL Testing

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Abstract: This application note describes how to alter the printed wiring board (PWB) netlist of a design containing the DS33R11T1/E1/J1 transceiver so that the netlist complies with the Joint Test Action Group (JTAG) specifications. These alterations are necessary because the DS33R11 was designed as a multichip module with multiple die in a single package which cannot be defined by the Boundary-Scan Description Language (BSDL) for board-level JTAG testing. The application note contains external pin mapping tables, internal die-pad bond tables, and contact information so the designer can quickly achieve accurate JTAG boundary-scan board testing.

Introduction

When manufacturing hardware for a telecommunications system, one of the basic tasks is to test the system for any production flaws. While there are many ways to test the hardware, one of the most popular methods uses the Joint Test Action Group (JTAG) boundary-scan method. The boundary-scan test method involves some minor changes to the hardware before production so that hardware verification can be performed after production. During design, all of the Integrated Circuit (IC) devices which support JTAG are connected in a serial daisy-chain fashion through the JTAG test access port. Verification is done by a specialized JTAG test system which connects to the test access port. The JTAG test system then uses a combination of the printed wiring board (PWB) netlist, Boundary-Scan Description Language (BSDL) files, and PWB connectivity test vectors to verify the pin-to-pin connections.

BSDL testing is straightforward. Nonetheless, multichip module devices like the DS33R11 Inverse-Multiplexing Ethernet Mapper with Integrated T1/E1/J1 Transceiver cannot be properly described by a single BSDL file because there are multiple die in a single package. This shortcoming can be overcome with simple modification to the PWB netlist and by using two BSDL files to describe the device package instead of just one.

Modifying the Printed Wiring Board Netlist

Before JTAG boundary scan testing can be performed, the portion of the PWB netlist that describes the external connections to the DS33R11 package must be modified to split those connections between the internal DS33Z11 die and DS2155 die. Once completed, the netlist will define the DS33R11 package with two independent reference designators. These reference designators allow two different BSDL files to individually describe the DS33Z11 and DS2155 connections inside the DS33R11 package.

Tables 1, **2**, and **3** and **Figure 1** make the task of modifying the netlist easy. Table 1 lists all of the external DS33R11 package pins which only connect to the DS33Z11 die. Table 2 lists all of the external DS33R11 package pins which only connect to the DS2155 die. Table 3 lists all of the external DS33R11

package pins which connect to both the DS33Z11 die and the DS2155 die. Figure 1 shows the same information in a format created for easier viewing.

This PWB netlist modification and JTAG boundary scan test have been performed using a Concise Net List format netlist of the DS33R11 engineering evaluation board designed with Cadence Concept. Designers can perform the operation in approximately 30 to 60 minutes, depending on the netlist type and individual's skill level. Most of the edits to the netlist file can be done with a simple text editor. Depending on the netlist type, however, it may be possible to edit the netlist in a program such as Microsoft® Excel which can sort rows based on column data. However the editing is done, it is important to pay careful attention to detail. Irregular data such as header and footer information must be maintained, and the netlist must always be saved in the original format.

The following is a list of steps needed to complete the process.

1. Open the netlist file in a text editor and group all of the nets connected to the DS33R11 reference designator. As an example, the DS33R11 package on the DS33R11 engineering evaluation board has a reference designator of U01.
2. Separate all of the nets isolated in step 1 among those connected to the DS33Z11 die, those connected to the DS2155 die, and those connected to both die. Use Tables 1, 2, and 3 and Figure 1 to complete this task.
3. Change the reference designator for all of the DS33Z11 nets from U01 to U01_D1 (short for reference designator U01, device 1). This step assumes that the DS33R11 reference designator is U01. If the reference designator is not U01, change U01_D1 appropriately.
4. Change the reference designator for all of the DS2155 nets from U01 to U01_D2 (short for reference designator U01, device 2). This assumes that the DS33R11 reference designator is U01. If it is not U01, change U01_D2 appropriately.
5. Duplicate the 22 shared nets so that there are exactly two of each. Split them into two groups.
6. Change the reference designator for first group of nets created in step 5 from U01 to U01_D1. This assumes that the DS33R11 reference designator is U01. If it is not U01, change U01_D1 appropriately.
7. Change the reference designator for second group of nets created in step 5 from U01 to U01_D2. This assumes that the DS33R11 reference designator is U01. If it is not U01, change U01_D2 appropriately.
8. Save the newly created netlist.

The newly created PCB netlist will actually contain two instances for the DS33R11 physical device. The first instance will describe the pin connections related to the DS33Z11 section; the second will describe pin connections related to the DS2155 section. The new netlist can be loaded into any JTAG test suite along with the two DS33R11 BSDL files and any associated test vectors.

Although the method documented here has been tested and verified to work properly, there can be some unforeseen complications with other netlist formats. If additional assistance is needed during JTAG boundary scan testing, please use the contact information below for further assistance.

Table 1. Device Pins for DS33Z11 Die Only

Pin	Description	Pin	Description	Pin	Description
A7	JTCLK1	L17	VDD3	V13	SDA[5]
A8	RST	L18	RXD[0]	V14	SDA[10]
A11	CS	L19	RXD[1]	V15	SMASK[3]
A15	VSS	L20	RXD[2]	V16	SMASK[2]
A19	REF_CLK	M17	VDD3	V17	SDATA[29]

A20	REF_CLKO	M18	RXD[3]	V18	SDATA[18]
B7	JTD1	M19	RX_CRS/CRS_DV	V19	SDATA[20]
B10	VDD1.8	M20	RX_CLK	V20	VSS
B15	VDD1.8	N17	VDD3	W1	SDATA[15]
B20	MODEC[1]	N18	COL_DET	W2	SDATA[0]
C7	JTRST1	N19	VSS	W3	SDATA[14]
C8	JTMS1	N20	VSS	W4	SDATA[9]
C9	JTDI1	P2	RDEN/RBSYNC	W5	SDATA[5]
C10	VSS	P17	VDD3	W6	SDATA[7]
C12	VDD1.8	P18	VDD1.8	W7	SCAS
C15	A9	P19	VDD1.8	W8	VSS
C16	A8	P20	VSS	W9	SRAS
C19	MDC	R17	VDD3	W10	SWE
C20	MDIO	R18	VDD3	W11	SDA[11]
D5	TDEN/TBSYNC	R19	VDD1.8	W12	SDA[1]
D8	VSS	R20	VDD1.8	W13	SDA[6]
D9	VSS	T17	VDD3	W14	SDA[0]
D10	VSS	T18	VDD3	W15	SDA[3]
D18	VSS	T19	SDATA[25]	W16	SDATA[31]
D19	VSS	T20	SDATA[26]	W17	SDATA[30]
D20	VDD3	U4	VSS	W18	VSS
E2	TSERO	U5	VSS	W19	SDATA[28]
E18	VSS	U6	VSS	W20	SDATA[23]
E19	TXD[3]	U7	VSS	Y1	VSS
E20	TXD[2]	U8	VSS	Y2	SDATA[2]
F1	TCLKE	U9	VSS	Y3	SDATA[4]
F2	RCLKI	U10	VSS	Y4	SDATA[1]
F3	VDD1.8	U11	VSS	Y5	SDATA[3]
F17	VDD3	U12	VSS	Y6	SMASK[0]
F18	TXD[1]	U13	VSS	Y7	VSS
F19	TXD[0]	U14	VSS	Y8	SDCLKO
F20	TX_EN	U15	VSS	Y9	VDD1.8
G17	VDD3	U16	VSS	Y10	SDA[9]
G18	VDD3	U17	VDD3	Y11	SBA[0]
G19	RMIIMIIS	U18	VSS	Y12	SDA[7]
G20	DCEDTES	U19	SDATA[22]	Y13	VDD1.8
H1	RSERI	U20	SDATA[24]	Y14	SDA[4]
H17	VDD3	V1	SDATA[13]	Y15	SDA[2]
H18	QOVF	V2	SDATA[11]	Y16	SDATA[16]
H19	TX_CLK	V3	SDATA[12]	Y17	SDATA[17]

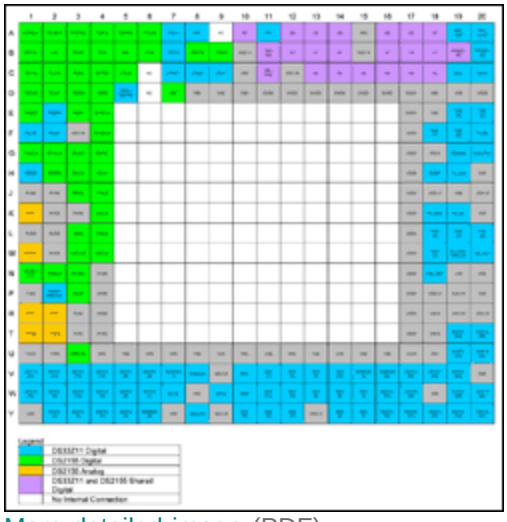
H20	VSS		V4	SDATA[10]		Y18	SDATA[27]
J17	VDD3		V5	SDATA[6]		Y19	SDATA[19]
J18	VDD1.8		V6	SDATA[8]		Y20	SDATA[21]
J19	VSS		V7	SMASK[1]			
J20	VDD1.8		V8	SYSCLKI			
K17	VDD3		V9	VDD1.8			
K18	RX_ERR		V10	SDCS			
K19	RX_DV		V11	SBA[1]			
K20	VSS		V12	SDA[8]			

Table 2. Device Pins for DS2155 Die Only

Pin	Description		Pin	Description		Pin	Description
A1	RCHBLK		D13	DVDD		L2	RVSS
A2	TCHBLK		D14	DVDD		L3	RSIG
A3	RFSYNC		D15	DVDD		L4	RNEGI
A4	TDATA		D16	DVDD		M1	RRING
A5	TSSYNC		D17	DVDD		M2	RVSS
A6	JTCLK2		E1	TPOSO		M3	RDCLKO
B1	BPCLK		E3	TSERI		M4	RDCLKI
B2	LIUC		E4	TSYSCLK		N1	RLOS/LTC
B3	TPOSI		E17	DVDD		N2	RNEGO
B4	TSIG		F4	RSYSCLK		N3	RPOSO
B5	RCL		G1	TCHCLK		N4	DVSS
B6	JTDI2		G2	RCHCLK		P1	TVSS
B8	JTRST2		G3	RCLKO		P3	RSIGF
B9	JTMS2		G4	RSYNC		P4	DVSS
C1	TSYNC		H2	RSERO		R1	TTIP
C2	TDCLKO		H3	RDATA		R2	TTIP
C3	TNEGI		H4	MCLK		R3	TVSS
C4	TSTRST		J1	RVSS		R4	DVSS
C5	JTDO2		J2	RVSS		T1	TRING
D1	TDCLKI		J3	RPOSI		T2	TRING
D2	TCLKT		J4	XTALD		T3	TVSS
D3	TNEGO		K1	RTIP		T4	DVSS
D4	TESO		K2	RVSS		U1	TVDD
D7	CST		K3	RVDD		U2	TVSS
D11	DVDD		K4	8XCLK		U3	RMSYNC
D12	DVDD		L1	RVDD			

Table 3. Shared Device Pins for DS33Z11 and DS2155 Die

Pin	Description
A10	INT
A12	D6
A13	D3
A14	D0
A16	A6
A17	A3
A18	A0
B11	RD/DS
B12	D7
B13	D4
B14	D1
B16	A7
B17	A4
B18	A1
B19	MODEC[0]
C11	WR/RW
C13	D5
C14	D2
C17	A5
C18	A2



More detailed image (PDF)

Figure 1. DS33R11 256-ball BGA, color-coded pinout and die map.

References

If you have additional questions on the JTAG testing of the DS33R11, please contact the Telecommunication Applications support team by email, telecom.support@maximintegrated.com, or telephone at 01-972-371-6555.

For more information about the DS33R11 Inverse-Multiplexing Ethernet Mapper with Integrated T1/E1/J1 Transceiver, please consult the appropriate data sheet at: T/E Carrier and Packetized Communications.

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Related Parts		
DS33R11	Ethernet Mapper with Integrated T1/E1/J1 Transceiver	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 4118: http://www.maximintegrated.com/an4118
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