

Very Low Output Low Dropout Regulator

■ GENERAL DESCRIPTION

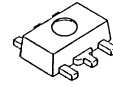
The NJM2842 is a very low output voltage, low drop out regulators.

It delivers up to 1A output current with the output voltage from 0.8V to 1.8V.

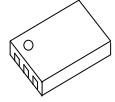
The use of an external bias voltage can improve the transient response and the ripple rejection characteristics while maintaining minimum input to output voltage.

The NJM2842 suitable for constant-voltage source such as CPU, DSP and ASIC.

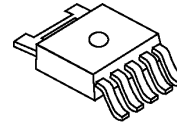
■ PACKAGE OUTLINE



NJM2842U2



NJM2842KH1

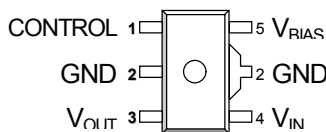


NJM2842DL3

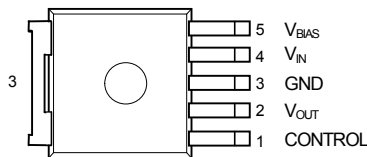
■ FEATURES

- Output Voltage Range 0.8V to 1.8V
- High Ripple Rejection 91 dB typ. @ $V_O=1.2V$
- Output Noise Voltage $V_{NO}=44 \mu V_{rms}$ typ. @ $V_O=1.2V$
- Output Current $I_O(\min)=1.0A$
- High Precision Output $V_O \pm 1.0\%$
- Dual input Voltage Type V_{IN}, V_{BIAS} (sequence free)
- High Stability for Load 0.002%/mA (max)
- Output Capacitor with 4.7 μF ceramic capacitor
- Low Dropout Voltage 0.1V typ. @ $I_O=600mA$
- ON/OFF Control
- Built-in Thermal Overload Protection and Current Limit Protection
- Bipolar Technology
- Package Outline SOT-89-5, DFN6-H1 (ESON6-H1), TO-252-5

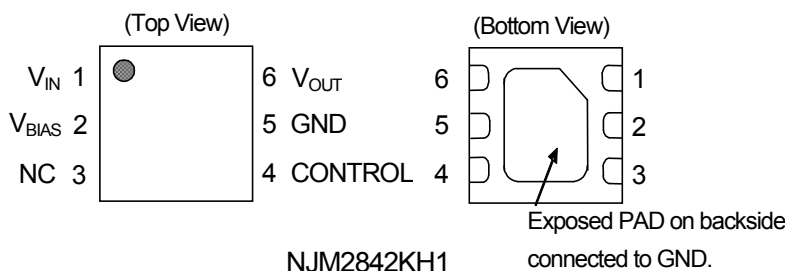
■ PIN COFIGURATION



NJM2842U2



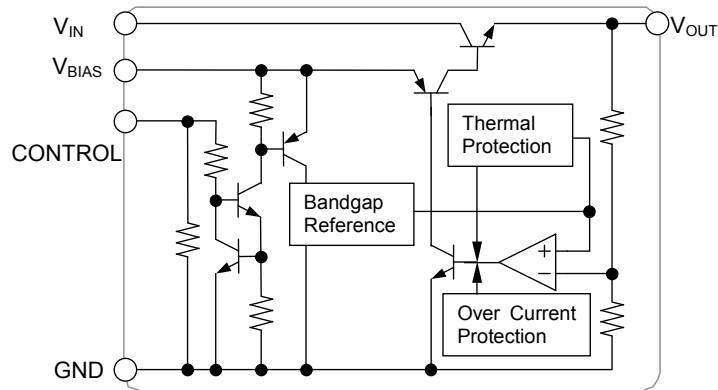
NJM2842DL3



NJM2842KH1

NJM2842

■ BLOCK DIAGRAM



■ OUTPUT VOLTAGE RANK LIST

Device Name SOT-89-5	V _O	Device Name DFN6-H1 (ESON6-H1)	V _O	Device Name TO-252-5	V _O
NJM2842U2-008	0.8V	NJM2842KH1-008	0.8V	NJM2842DL3-011	1.1V
NJM2842U2-010	1.0V	NJM2842KH1-010	1.0V	NJM2842DL3-012	1.2V
NJM2842U2-011	1.1V	NJM2842KH1-012	1.2V		
NJM2842U2-012	1.2V	NJM2842KH1-015	1.5V		
NJM2842U2-0145	1.45V	NJM2842KH1-018	1.8V		
NJM2842U2-015	1.5V				
NJM2842U2-018	1.8V				

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS		UNIT
Input Voltage	V _{IN}	+7		V
Bias Voltage	V _{BIAS}	+7		V
Control Voltage	V _{CONT}	+7		V
Power Dissipation	P _D	SOT-89-5	625 (*1)	mW
			2400 (*2)	
		TO-252-5	1190(*1)	
			3125(*2)	
DFN6-H1 (ESON6-H1)	440 (*3)			
	1200 (*4)			
Operating Temperature	T _{opr}	-40 ~ +125		°C
Storage Temperature	T _{stg}	-40 ~ +150		°C

(*1): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard size, 2Layers, Cu area 100mm²)

(*2): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard, 4Layers)

(4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

(*3): Mounted on glass epoxy board based on EIA/JEDEC. (101.5x 114.5x1.6mm, 2Layers, Use the Exposed Pad)

(*4): Mounted on glass epoxy board based on EIA/JEDEC. (101.5x 114.5x1.6mm, 4Layers, Use the Exposed Pad)

(4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ BIAS VOLTAGE INPUT RANGE

V_{BIAS} = +2.5V to +5.5V (V_O < 1.5V)

V_{BIAS} = V_O + 1V to +5.5V (V_O ≥ 1.5V)

■ ELECTRICAL CHARACTERISTICS

($V_{BIAS}=2.5V(V_O \geq 1.5V)$: $V_{BIAS}=V_O+1V$, $V_{IN}=V_O+1V$, $C_{BIAS}=0.1\mu F$, $C_{IN}=4.7\mu F$, $C_O=4.7\mu F$, $T_a=25^\circ C$)

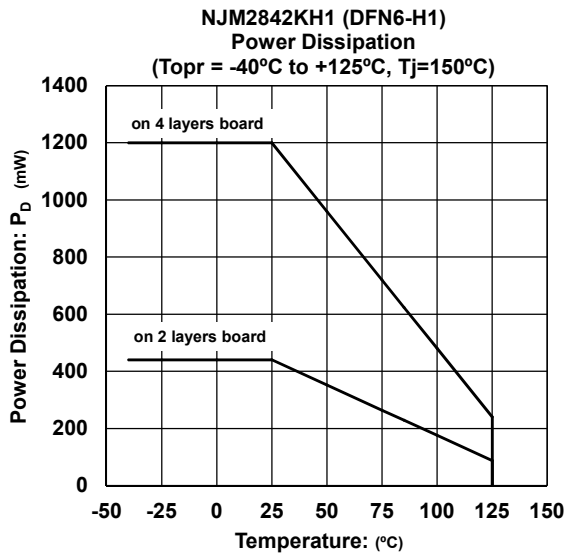
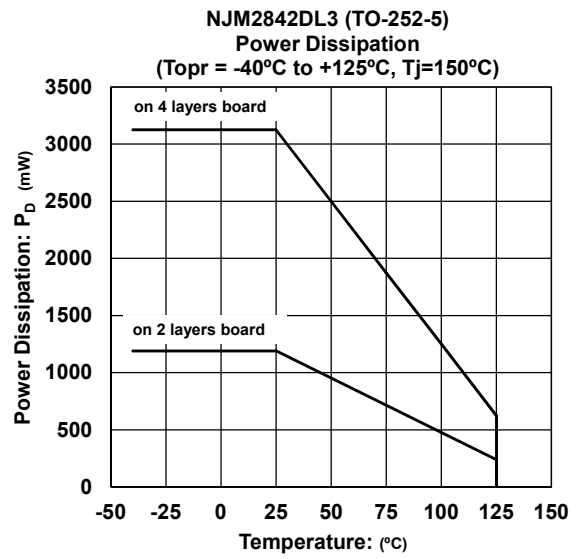
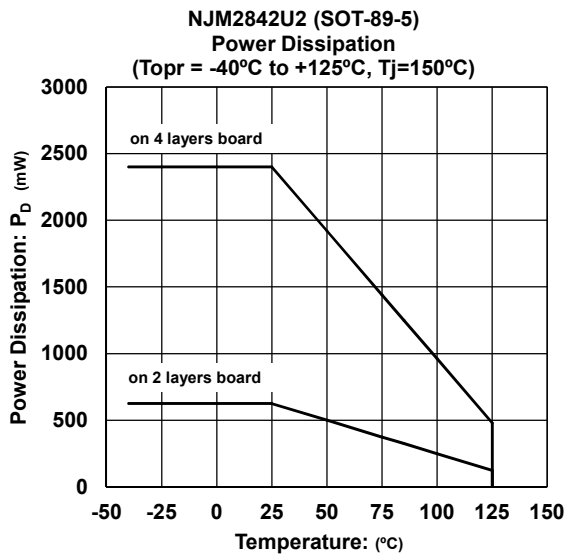
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_O	$I_O=30mA$	-1.0%	-	+1.0%	V
Unloaded Bias Current	I_{BIAS}	$I_O=0mA$, except I_{CONT}	-	300	500	μA
Unloaded Input Current	I_{IN}	$I_O=0mA$, except I_{CONT}	-	-	20	μA
Bias Current at Control OFF	$I_{BIAS(OFF)}$	$V_{CONT}=0V$	-	-	100	nA
Input Current at Control OFF	$I_{IN(OFF)}$	$V_{CONT}=0V$	-	-	100	nA
Output Current	I_O	$V_O \times 0.9$	1000	-	-	mA
Line Regulation 1 (V_{BIAS})	$\Delta V_O/\Delta V_{BIAS}$	$V_{BIAS}=2.5V$ to $+5.5V(V_O < 1.5V)$ $V_{BIAS}=V_O+1V$ to $+5.5V(V_O \geq 1.5V)$ $I_O=30mA$	-	-	0.10	%/V
Line Regulation 2 (V_{IN})	$\Delta V_O/\Delta V_{IN}$	$V_{IN}=V_O+1V$ to $+5.5V$, $I_O=30mA$	-	-	0.10	%/V
Load Regulation	$\Delta V_O/\Delta I_O$	$I_O=30mA$ to $1000mA$	-	-	0.002	%/mA
Dropout Voltage	ΔV_{I-O}	$I_O=600mA$	-	0.10	0.18	V
Ripple Rejection Ratio 1 (V_{BIAS})	$RR(V_{BIAS})$	$V_{BIAS}=3.5V(V_O < 1.5V)$ $V_{BIAS}=3.8V(V_O \geq 1.5V)$ $e_{bias}=200mV_{rms}$, $f=1kHz$, $I_O=10mA$	Refer to Table 1			dB
Ripple Rejection Ratio 2 (V_{IN})	$RR(V_{IN})$	$e_{in}=200mV_{rms}$, $f=1kHz$, $I_O=10mA$	Refer to Table 1			dB
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T_a$	$T_a=0$ to $+85^\circ C$, $I_O=10mA$	-	± 50	-	ppm/ $^\circ C$
Output Noise Voltage	V_{NO}	$f=10Hz$ to $80kHz$, $I_O=10mA$	Refer to Table 1			μV_{rms}
Control Current	I_{CONT}	$V_{CONT}=1.6V$	-	3	12	μA
Control Voltage for ON-state	$V_{CONT(ON)}$		1.6	-	-	V
Control Voltage for OFF-state	$V_{CONT(OFF)}$		-	-	0.6	V
Bias Voltage	V_{BIAS}		-	-	5.5	V
Input Voltage	V_{IN}		-	-	5.5	V

Table1

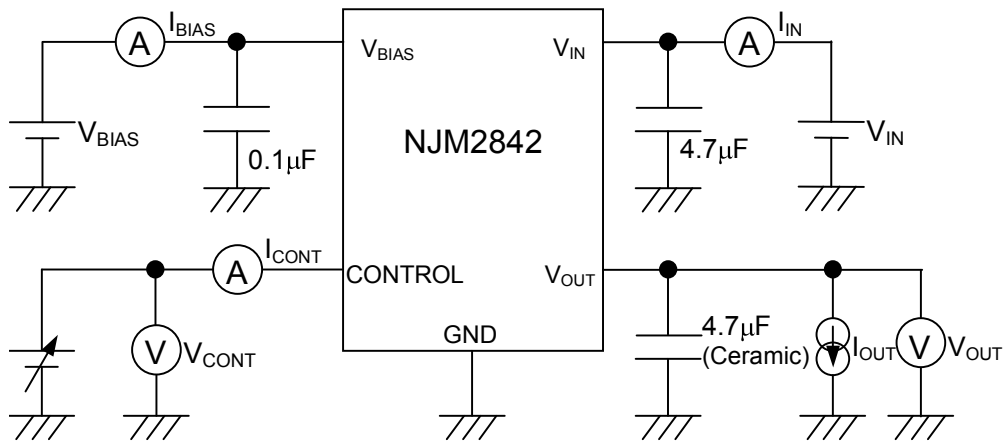
Voltage Rank	Ripple Rejection Ratio 1 (V_{BIAS})				Ripple Rejection Ratio 2 (V_{IN})				Output Noise Voltage			
	MIN.	TYP.	MAX.	UNIT	MIN.	TYP.	MAX.	UNIT	MIN.	TYP.	MAX.	UNIT
0.8V	-	77	-	dB	-	93	-	dB	-	34	-	μV_{rms}
1.0V	-	75	-		-	92	-		-	38	-	
1.1V	-	74	-		-	91	-		-	41	-	
1.2V	-	73	-		-	91	-		-	44	-	
1.45V	-	71	-		-	90	-		-	47	-	
1.5V	-	71	-		-	90	-		-	47	-	
1.8V	-	70	-		-	89	-		-	51	-	

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POWER DISSIPATION vs. AMBIENT TEMPERATURE

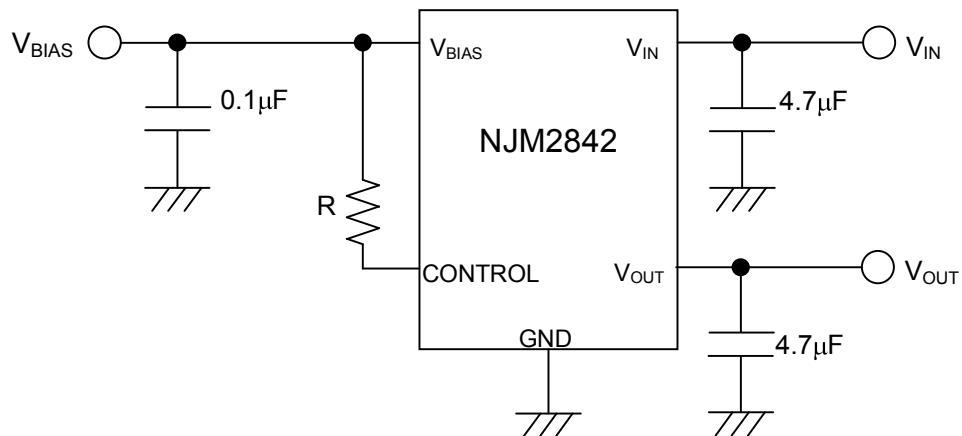


TEST CIRCUIT

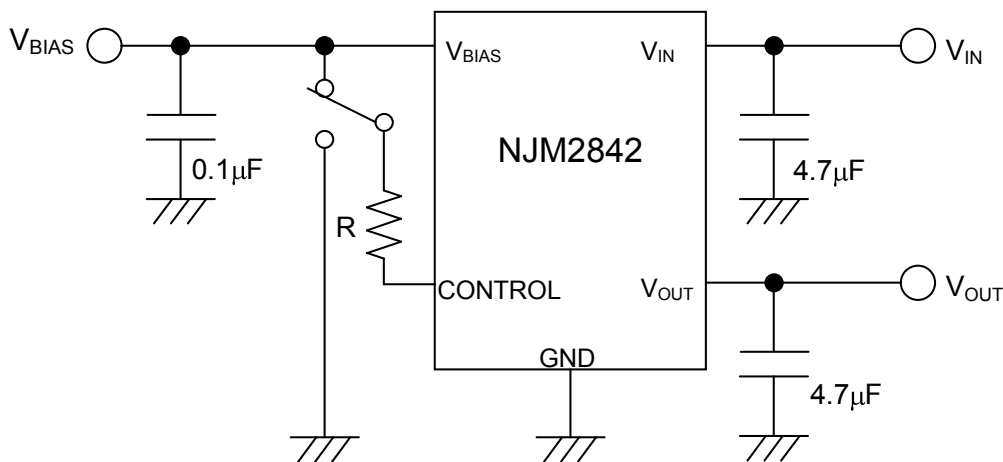


TYPICAL APPLICATION

a) In case of where ON/OFF control is not required:



b) In use of ON/OFF control:



State of control pin:

"H" → output is enabled.

"L" or "open" → output is disabled.

*In the case of using a resistance "R" between V_{BIAS} and control.

If this resistor is inserted, it can reduce the control current when the control voltage is high.

The applied voltage to control pin should set to consider voltage drop through the resistor "R" and the minimum control voltage for ON-state.

The $V_{CONT(ON)}$ and I_{CONT} have temperature dependence as shown in the "Control Current vs. Temperature" and "Control Voltage vs. Temperature" characteristics. Therefore, the resistance "R" should be selected to consider the temperature characteristics.

* Bias Capacitance (C_{BIAS}) and an Input Capacitance (C_{IN})

C_{BIAS} and C_{IN} are required to prevent oscillation and reduce power supply ripple for applications when high power supply impedance or a long power supply line.

Therefore, use the recommended C_{BIAS} and C_{IN} value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between $V_{BIAS-GND}$ and V_{IN-GND} as shortest path as possible to avoid the problem.

*Output Capacitor C_O

Output capacitor (C_O) will be required for a phase compensation of the internal error amplifier.

The capacitance and the equivalent series resistance (ESR) influence to stable operation of the regulator.

Use of a smaller C_O may cause excess output noise or oscillation of the regulator due to lack of the phase compensation.

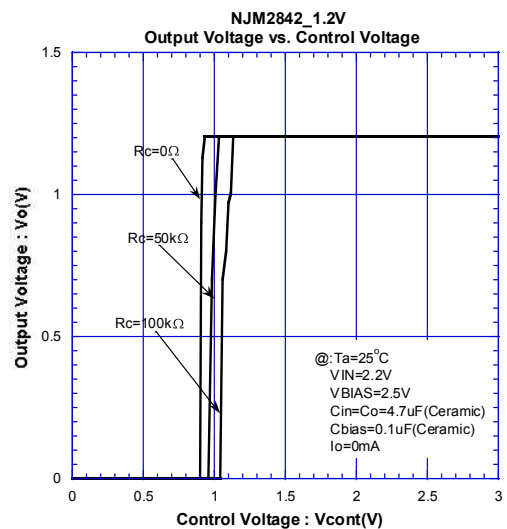
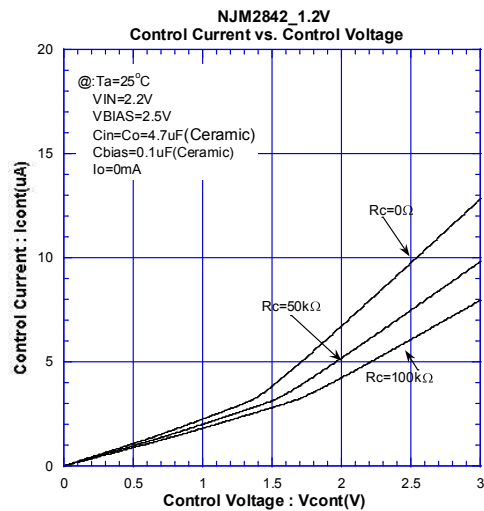
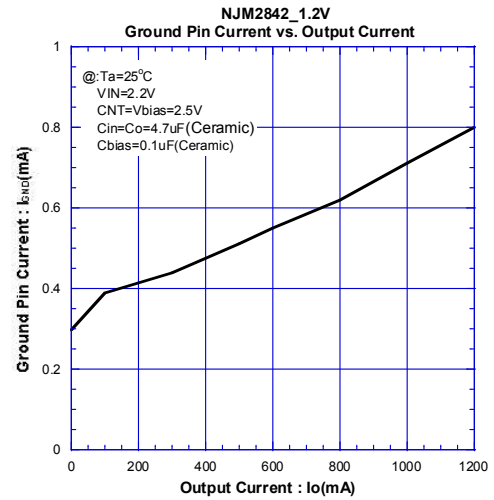
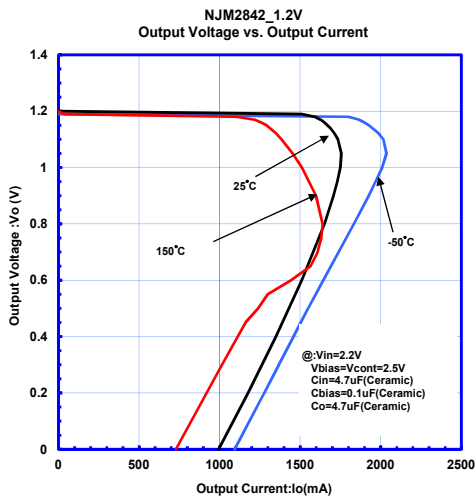
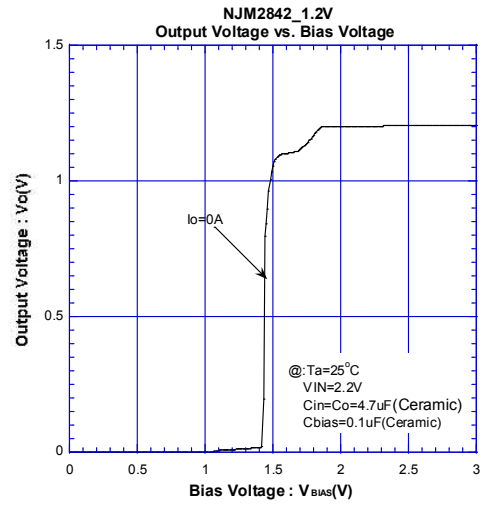
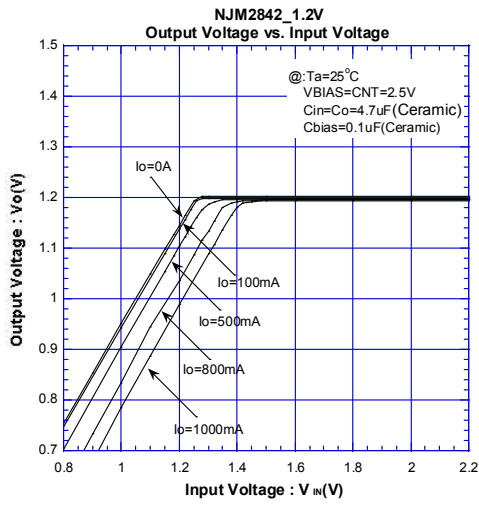
On the other hand, Use of a larger C_O reduces output noise and ripple output, and also improves output transient response when rapid load change.

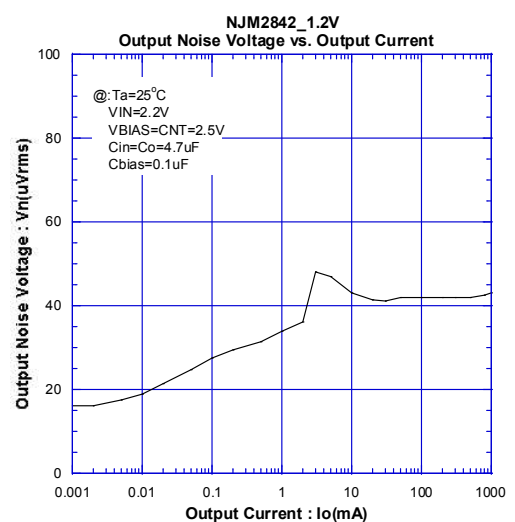
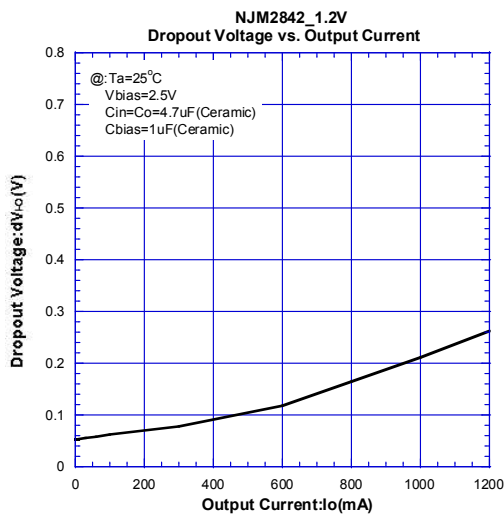
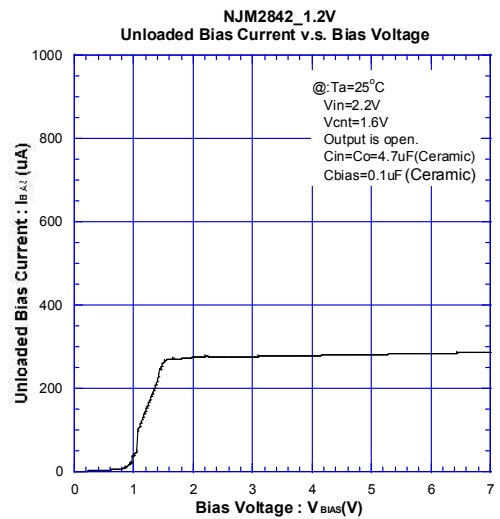
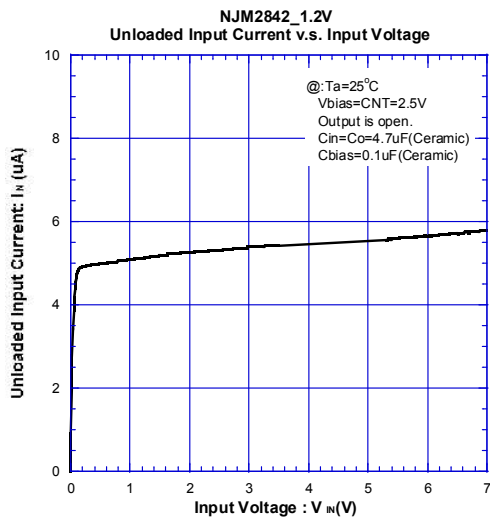
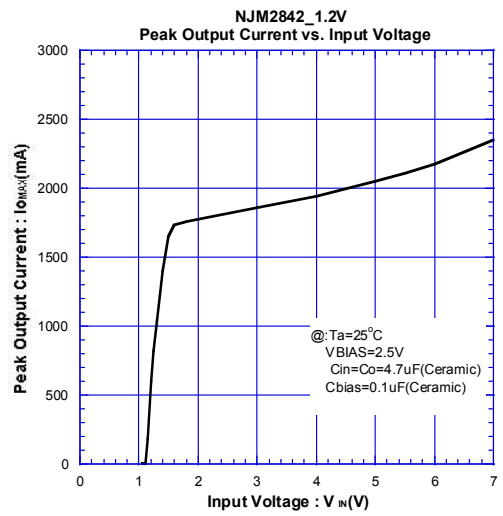
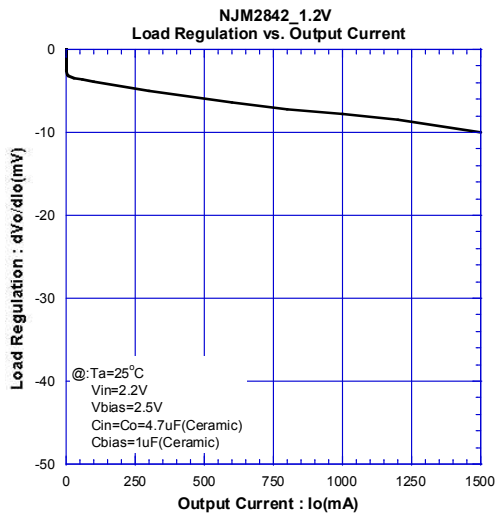
Therefore, use the recommended C_O value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and V_{OUT} as shortest path as possible for stable operation

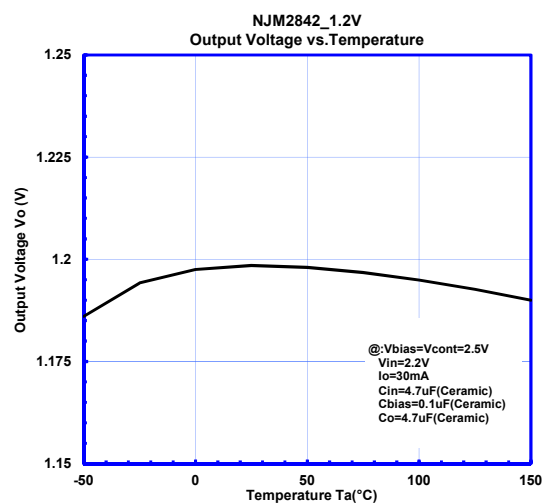
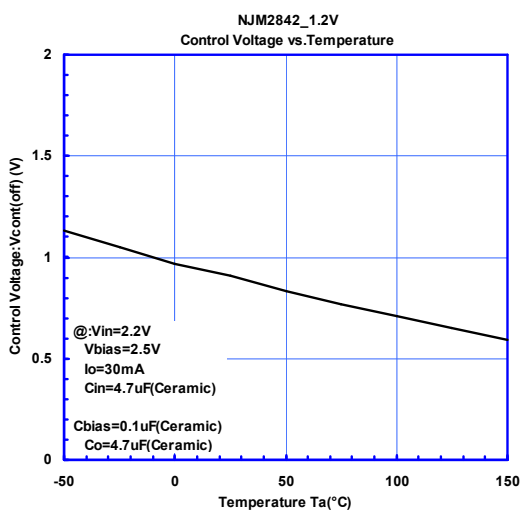
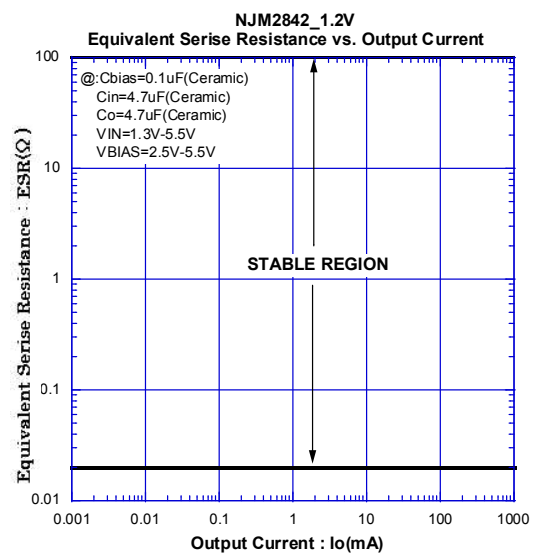
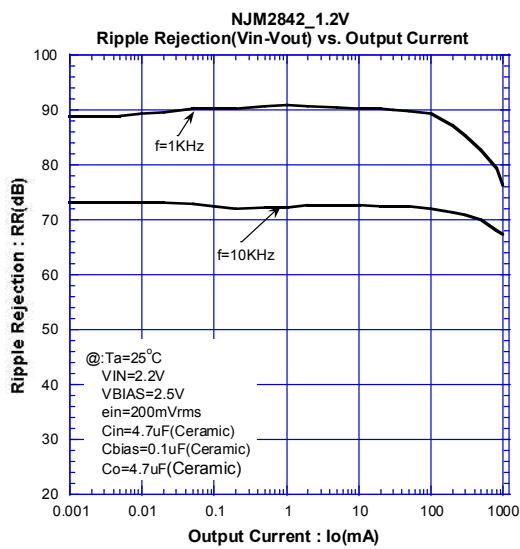
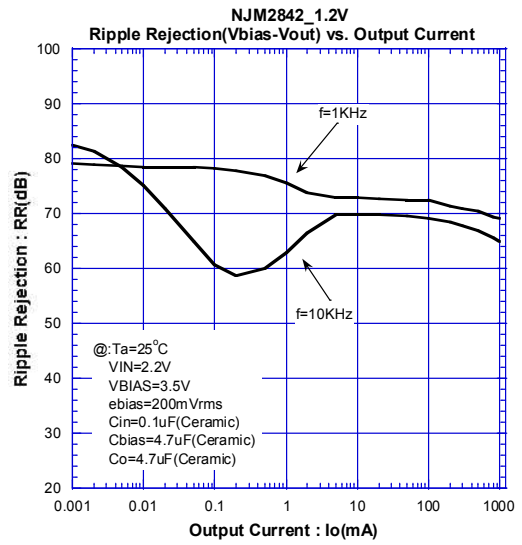
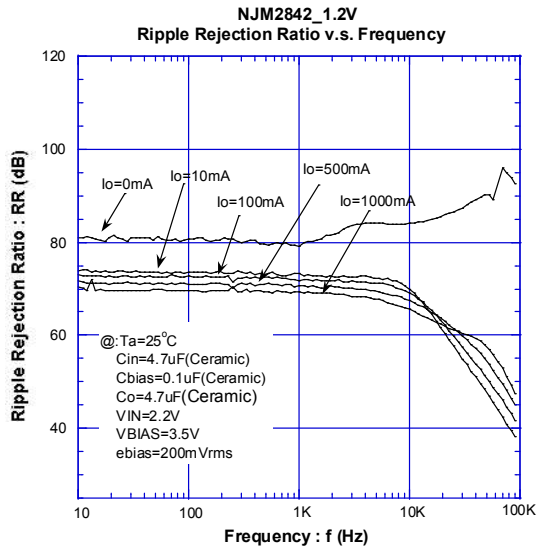
In addition, you should consider varied characteristics of capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

When selecting C_O , recommend that have withstand voltage margin against output voltage and superior temperature characteristic.

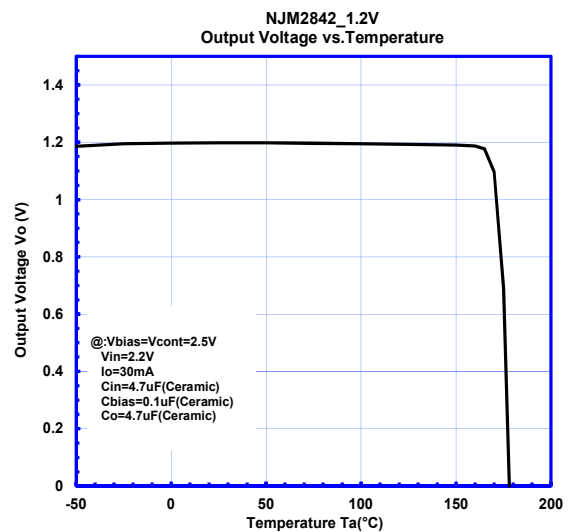
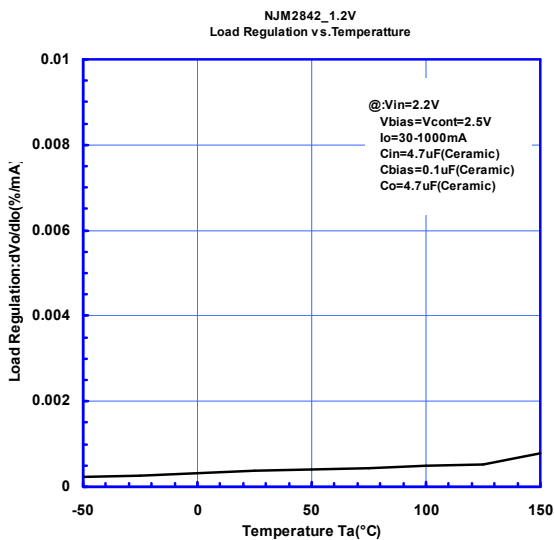
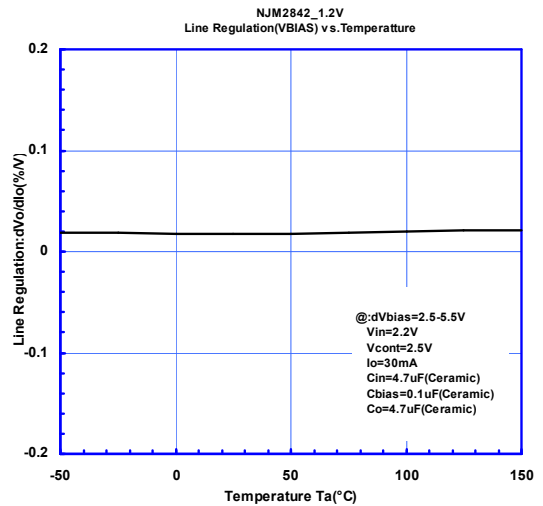
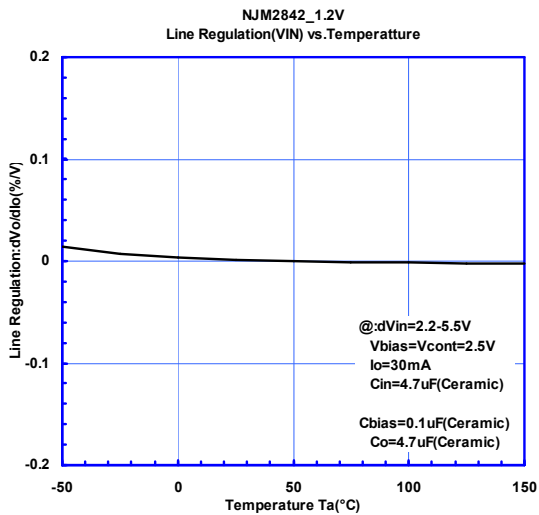
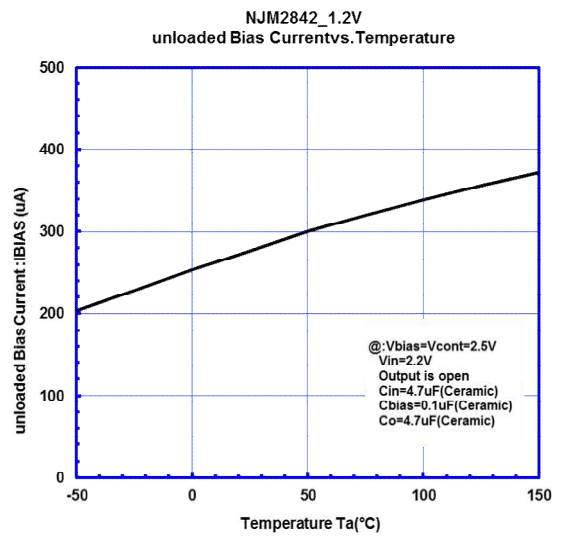
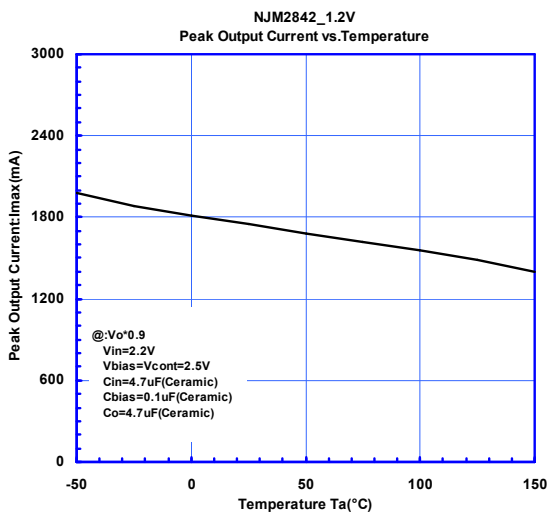
■ TYPICAL CHARACTERISTICS

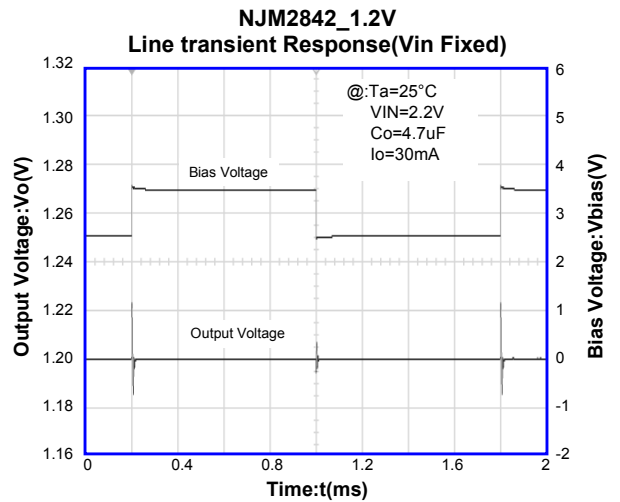
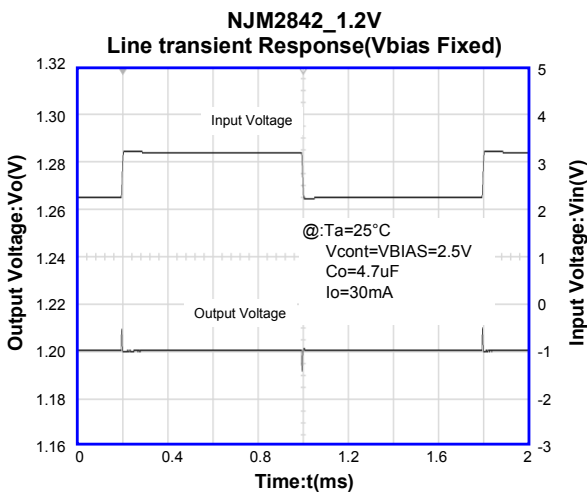
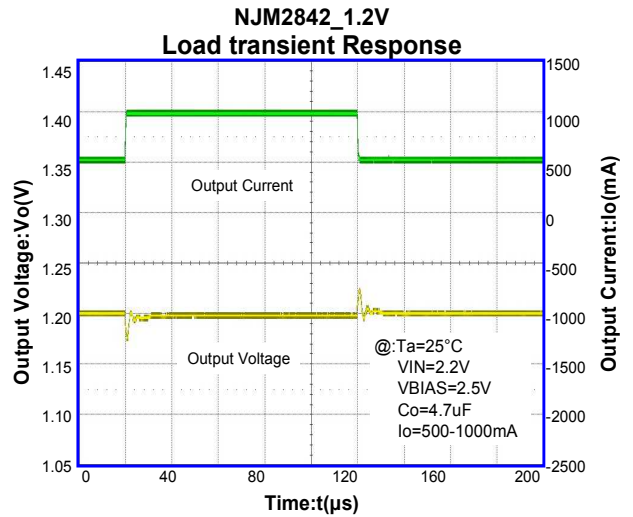
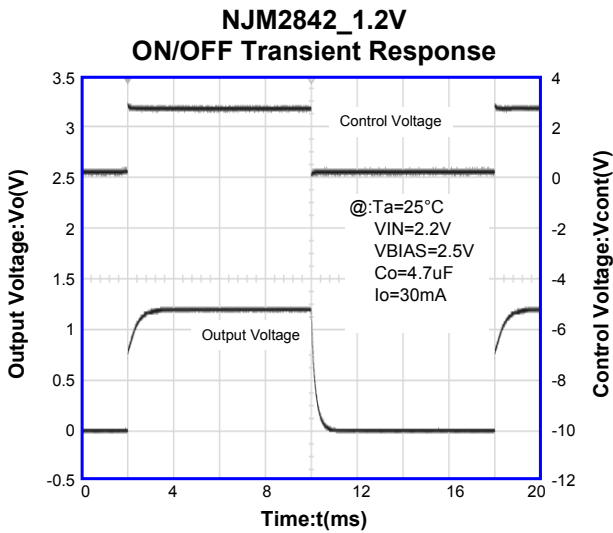
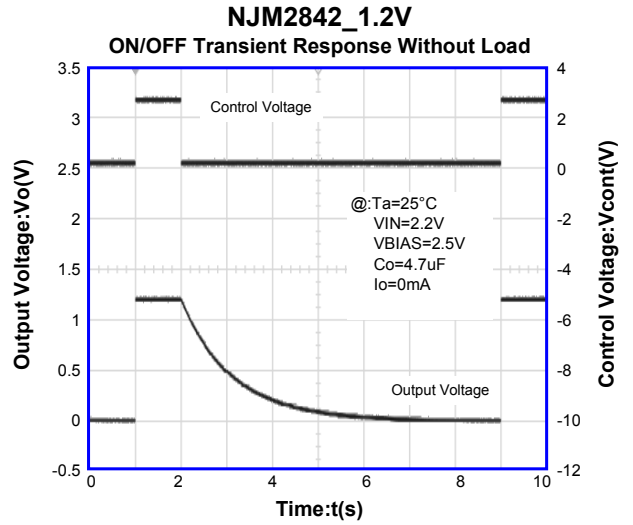
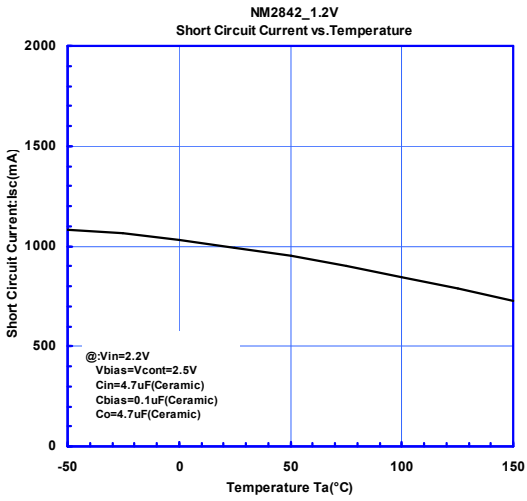






NJM2842





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