TEXAS INSTRUMENTS

TPS61300, TPS61301
TPS61305, TPS61305A, TPS61306

SLVS957E – JUNE 2009 – REVISED APRIL 2016

TPS6130xx 1.5-A and 4.1-A Multiple LED Camera Flash Driver With I²C Compatible Interface

1 Features

- Four Operational Modes
  - DC Light and Flashlight
  - Voltage Regulated Converter: 3.8 V to 5.7 V
  - Standby: 2 µA (Typical)
- Storage Capacitor Friendly Solution
- Automatic V_F and ESR Calibration
- Power-Save Mode for Improved Efficiency at Low Output Power, Up to 95% Efficiency
- Output Voltage Remains Regulated When Input Voltage Exceeds Nominal Output Voltage
- I²C Compatible Interface up to 3.4 Mbits/s
- Zero Latency Tx-Masking Input
- Hardware Voltage Mode Selection Input (TPS61300, TPS61301)
- DC Light Mode Selection Input (TPS61300, TPS61306)
- Hardware Reset Input (TPS61301, TPS61305)
- LED Temperature Monitoring (TPS61305)
- Privacy Indicator LED Output
- Integrated LED Safety Timer
- Total Solution Size of Less Than 25 mm² (< 1 mm height)
- Available in a 20-Pin NanoFree™ (DSBGA)

2 Applications

- Single, Dual, or Triple White LED Flashlight Supply for Cell Phones and Smart-Phones
- LED Based Xenon *Killer* Flashlight
- Audio Amplifier Power Supply

3 Description

The TPS6130xx device is based on a high-frequency synchronous boost topology with constant current sinks to drive up to three white LEDs in parallel (400-mA, 800-mA, and 400-mA maximum flash current). The extended high-current mode (HC_SEL) allows up to 1025-mA, 2050-mA, and 1025-mA flash current out of the storage capacitor.

The high-capacity storage capacitor on the output of the boost regulator provides the high-peak flash LED current, thereby reducing the peak current demand from the battery to a minimum.

The 2-MHz switching frequency allows the use of small and low profile 2.2-µH inductors. To optimize overall efficiency, the device operates with a 400-mV LED feedback voltage.

The TPS6130xx device not only operates as a regulated current source, but also as a standard voltage boost regulator. The device keeps the output voltage regulated even when the input voltage exceeds the nominal output voltage. The device enters power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

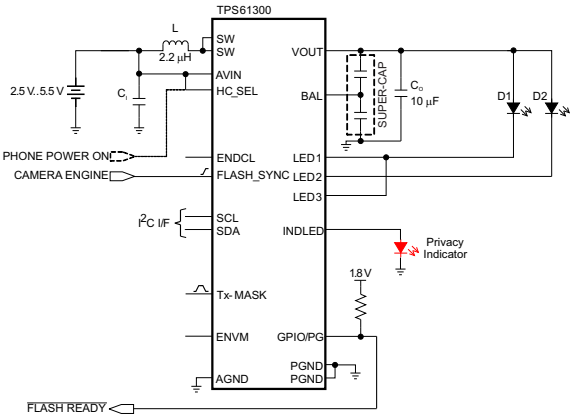
To simplify flashlight synchronization with the camera module, the device offers a trigger pin (FLASH_SYNC) for zero latency LED turnon time.

Table 1. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6130xx	DSBGA (20)	1.90 mm × 2.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Figure 1. Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2012) to Revision E — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (August 2012) to Revision D — **Page**

- Added note specifying silicon revision ID bits can differ depending on the product die revision number. ... 49

Changes from Revision B (September 2011) to Revision C — **Page**

- Changed active cell balancing circuitry maximum quiescent current into VOUT from 3.0 to 6.0 µA ... 7
- Added additional information related to the DC-DC input current limiting scheme. ... 36
- Added additional information related to the DC-DC input current limiting scheme. ... 36
- Added note 2 to REGISTER1 DESCRIPTION (TPS61300, TPS61301) table ... 40
- Added note 2 to REGISTER1 DESCRIPTION (TPS61305, TPS61306) table ... 41

Changes from Revision A (September 2010) to Revision B — **Page**

- Changed I_{STBY} MAX current from 5 µA to 12 µA ... 6

Changes from Original (June 2009) to Revision A — **Page**

- Deleted product preview device number TPS61306 from data sheet header ... 1

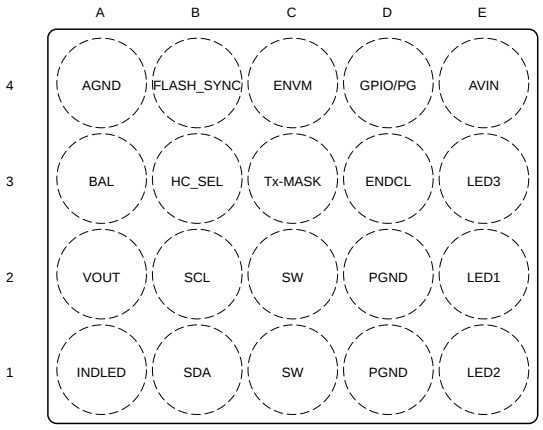
5 Device Comparison Table

PACKAGE MARKING	DEVICE SPECIFIC FEATURES(1)
TPS61300	Hardware enable DC light input (ENDCL)
TPS61301	Hardware enable / Disable input (NRESET)
TPS61305	Hardware enable / Disable input (NRESET) LED temperature monitoring input (TS)
TPS61305A	Hardware enable / Disable input (NRESET) LED temperature monitoring input (TS)
TPS61306(2)	Hardware enable DC light input (ENDCL) LED temperature monitoring input (TS)

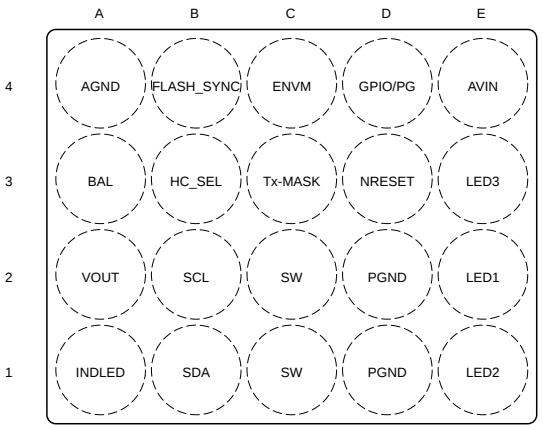
(1) For more details, see *Feature Description*.
(2) Device status is Product Preview. Contact TI for more details.

6 Pin Configuration and Functions

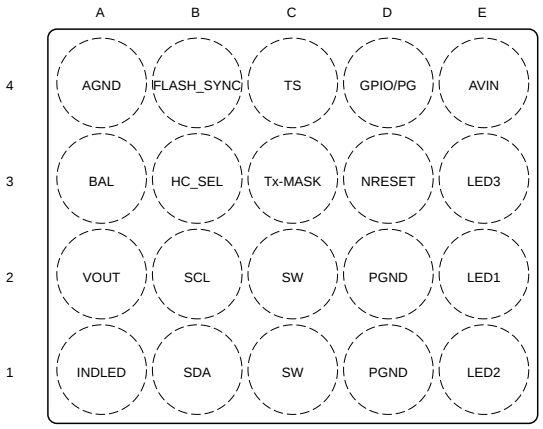
TPS61300
YFF Package
20-Pin DSBGA
Top View



TPS61301
YFF Package
20-Pin DSBGA
Top View



TPS61305 and TPS61305A
YFF Package
20-Pin DSBGA
Top View



TPS61306
YFF Package
20-Pin DSBGA
Top View

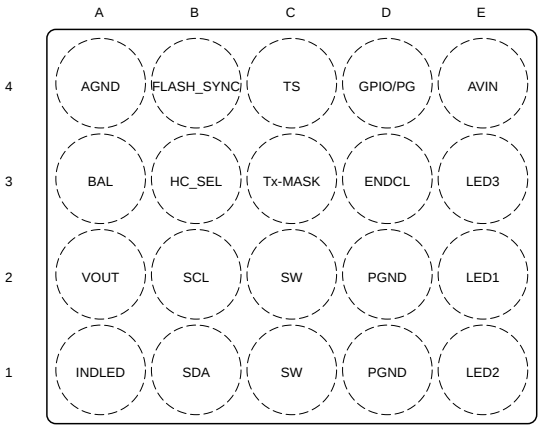


Table 2. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	A4	—	Analog ground.
AVIN	E4	I	This is the input voltage pin of the device. Connect directly to the input bypass capacitor.
BAL	A3	O	Balancing output for dual cells super-capacitor. In steady-state operation, this output compensates for leakage current mismatch between the cells.
ENDCL(1)	D3	I	Hardware control pin for DC light operation. Pulling this pin high forces the device into DC light operation. The ENDCL input is only active when the device is programmed into shutdown or voltage mode regulation. LED1–3 inputs are controlled according to ENLED[3:1] bit settings.
ENVM(2)	C4	I	Enable pin for voltage mode converter. Pulling this pin high forces the device into voltage regulation mode (V_{OUT} is preset to a fixed value, 4.95 V).
FLASH_SYNC	B4	I	Flashlight strobe pulse synchronization input. FLASH_SYNC = LOW: The device is operating and regulating the LED current to the DC light current level (DCLC). FLASH_SYNC = HIGH: The device is operating and regulating the LED current to the flashlight current level (FC).
GPIO/PG	D4	I/O	This pin can either be configured as a general purpose input/output pin (GPIO) or either as an open-drain or a push-pull output to signal when the converters output voltage is within the regulation limits (PG). Per default, the pin is configured as an open-drain power-good output.
HC_SEL	B3	I	Extended high-current mode selection input. This pin must not be left floating and must be terminated. **HC_SEL = LOW: LED direct drive mode.** The power stage is active and the maximum LED currents are defined as 400 mA (ILED1), 800 mA (ILED2), and 400 mA (ILED3). **HC_SEL = HIGH: Energy storage mode.** In flash mode, the power stage is either active with reduced current capability or disabled. The maximum LED current is defined as 925 mA (ILED1), 1850 mA (ILED2), and 925 mA (ILED3).
INDLED	A1	O	This pin provides a constant current source to drive low V_F LEDs. Connect to LED anode.
LED1	E2	I	LED return input. This feedback pin regulates the LED current through the internal sense resistor by regulating the voltage across it. The regulation operates with typically 400-mV (HC_SEL = L) or 400-mV (HC_SEL = H) dropout voltage. Connect to the cathode of the LEDs.
LED2	E1	I	
LED3	E3	I	
NRESET(3)	D3	I	Master hardware reset input. NRESET = LOW: The device is forced in shutdown mode and the I^2C control I/F is reset. NRESET = HIGH: The device is operating normally under the control of the I^2C interface.
PGND	D1, D2	—	Power ground. Connect to AGND underneath IC.
SCL	B2	I	Serial interface clock line. This pin must not be left floating and must be terminated.
SDA	B1	I/O	Serial interface address/data line. This pin must not be left floating and must be terminated.
SW	C1, C2	I/O	Inductor connection. Drain of the internal power MOSFET. Connect to the switched side of the inductor. SW is high impedance during shutdown.
TS(4)	C4	I/O	NTC resistor connection. This pin can be used to monitor the LED temperature. Connect a 220-kΩ NTC resistor from the TS input to ground. In case this functionality is not desired, the TS input must be tied to AVIN or left floating.
Tx-MASK	C3	I	RF PA synchronization control input. Pulling this pin high turns the LED from flashlight to DC light operation, thereby reducing almost instantaneously the peak current loading from the battery.
VOUT	A2	O	This is the output voltage pin of the converter.

(1) Applicable to the TPS61300 and TPS61306 only.
(2) Applicable to the TPS61300 and TPS61301 only.
(3) Applicable to the TPS61301 and TPS61305A only.
(4) Applicable to the TPS61305A and TPS61306 only.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range(2)	AVIN, VOUT, SW, LED1, LED2, LED3, SCL, SDA, FLASH_SYNC, ENDCL, NRESET, ENVM, GPIO/PG, HC_SEL, Tx-MASK, TS, BAL	–0.3	7	V
Current on GPIO/PG			±25	mA
Power dissipation		Internally limited		
Operating ambient temperature(3), T_A		–40	85	°C
Maxium operating junction temperature, $T_{J(MAX)}$			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(MAX)}$] is dependent on the maximum operating junction temperature [$T_{J(MAX)}$], the maximum power dissipation of the device in the application [$P_{D(MAX)}$], and the junction-to-ambient thermal resistance of the part and package in the application (θ_{JA}), as given by the following equation: $T_{A(MAX)} = T_{J(MAX)} – (\theta_{JA} \times P_{D(MAX)})$

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6130xx YFF (DSBGA) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Unless otherwise noted the specification applies for V_{IN} = 3.6 V over an operating junction temperature T_J = –40°C to 125°C; Circuit of (unless otherwise noted). Typical values are for T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.5		5.5	V
I_Q	Operating quiescent current into AVIN	I_{OUT} = 0 mA, device not switching –40°C ≤ T_J ≤ 85°C		590	700	µA
		$I_{OUT(DC)}$ = 0 mA, PWM operation V_{OUT} = 4.95 V, voltage regulation mode		11.3		mA
I_{SD}	Shutdown current	HC_SEL = 0, –40°C ≤ T_J ≤ 85°C		1	5	µA
I_{STBY}	Standby current	HC_SEL = 1, storage capacitor balanced –40°C ≤ T_J ≤ 85°C		2	12	µA
	Precharge current	V_{OUT} = 2.3 V, 2.5 V ≤ V_{IN} ≤ 5.5 V	150			mA
	Precharge hysteresis (referred to V_{OUT})		40	75		mV
V_{UVLO}	Undervoltage lockout threshold (analog circuitry)	V_{IN} falling		2.3	2.4	V
OUTPUT						
V_{OUT}	Output voltage range	Current regulation mode	VIN		5.5	V
		Voltage regulation mode	3.825		5.7	
	Internal feedback voltage accuracy	2.5 V ≤ V_{IN} ≤ 4.8 V, –20°C ≤ T_J ≤ 125°C Boost mode, PWM voltage regulation	–2%		2%	
0.85	Power-save mode ripple voltage	I_{OUT} = 10 mA		0.015 × V_{OUT}		$V_{P–P}$
OVP	Output overvoltage protection	V_{OUT} rising, 0000 ≤ OV[3:0] ≤ 0100	4.5	4.65	4.8	V
		V_{OUT} rising, 0101 ≤ OV[3:0] ≤ 1111	5.8	6	6.2	
	Output overvoltage protection hysteresis	V_{OUT} falling, 0101 ≤ OV[3:0] ≤ 1111		0.15		
POWER SWITCH						
$r_{DS(on)}$	Switch MOSFET ON-resistance	V_{OUT} = V_{GS} = 3.6 V		90		mΩ
	Rectifier MOSFET ON-resistance	V_{OUT} = V_{GS} = 3.6 V		135		mΩ
$I_{lkg(SW)}$	Leakage into SW	V_{OUT} = 0 V, SW = 3.6 V, –40°C ≤ T_J ≤ 85°C		0.3	4	µA
I_{lim}	Rectifier valley current limit (open loop)	VOUT = 4.95 V, HC_SEL = 0, –20°C ≤ T_J ≤ 85°C PWM operation, relative to selected ILIM	–15%		15%	
OSCILLATOR						
f_{OSC}	Oscillator frequency			1.92		MHz
f_{ACC}	Oscillator frequency		–10%		7%	
THERMAL SHUTDOWN, HOT DIE DETECTOR						
	Thermal shutdown(1)		140	160		°C
	Thermal shutdown hysteresis(1)			20		°C
	Hot die detector accuracy(1)		–8		8	°C

(1) Verified by characterization. Not tested in production.

Electrical Characteristics (continued)

Unless otherwise noted the specification applies for V_{IN} = 3.6 V over an operating junction temperature T_J = –40°C to 125°C; Circuit of (unless otherwise noted). Typical values are for T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
LED CURRENT REGULATOR							
	LED1/3 current accuracy(1)	HC_SEL = 0	0.4 V ≤ $V_{LED1/3}$ ≤ 2 V 00 ≤ DCLC13[1:0] ≤ 11, T_J = 85°C	–10%		10%	
			0.4 V ≤ $V_{LED1/3}$ ≤ 2 V 00 ≤ FC13[1:0] ≤ 11, T_J = 85°C	–7.5%		7.5%	
	LED2 current accuracy(1)		0.4 V ≤ V_{LED2} ≤ 2 V 000 ≤ DCLC2[2:0] ≤ 111, T_J = 85°C	–10%		10%	
			0.4 V ≤ V_{LED2} ≤ 2 V 000 ≤ FC2[2:0] ≤ 111, T_J = 85°C	–7.5%		7.5%	
	LED1/3 current accuracy(1)	HC_SEL = 1	0.4 V ≤ $V_{LED1/3}$ ≤ 2 V 00 ≤ DCLC13[1:0] ≤ 11, T_J = 85°C	–10%		10%	
			0.4 V ≤ $V_{LED1/3}$ ≤ 2 V 00 ≤ FC13[1:0] ≤ 11, T_J = 85°C	–10%		10%	
	LED2 current accuracy(1)		0.4 V ≤ V_{LED2} ≤ 2 V 000 ≤ DCLC2[2:0] ≤ 111, T_J = 85°C	–10%		10%	
			0.4 V ≤ $V_{LED1/3}$ ≤ 2 V 000 ≤ FC2[2:0] ≤ 111, T_J = 85°C	–10%		10%	
	LED1/3 current matching(1)			–10%		10%	
	LED1/2/3 current temperature coefficient				0.05		%/°C
	INDLED current accuracy		1.5 V ≤ (VIN – VINDLED) ≤ 2.5 V 2.6 mA ≤ IINDLED ≤ 7.9 mA, T_J = 25°C	–20%		20%	
	INDLED current temperature coefficient				0.04		%/°C
V_{DO}	LED1/2/3 sense voltage		$I_{LED1–3}$ = full-scale current, HC_SEL = 0		400		mV
	LED1/2/3 sense voltage		$I_{LED1–3}$ = full-scale current, HC_SEL = 1		400	450	
	VOUT dropout voltage		I_{OUT} = –7.5 mA, device not switching			220	
	LED1/2/3 input leakage current		$V_{LED1/2/3}$ = V_{OUT} = 5 V, –40°C ≤ T_J ≤ 85°C		0.1	4	µA
	INDLED input leakage current		V_{INDLED} = 0 V, –40°C ≤ T_J ≤ 85°C		0.1	1	µA
STORAGE CAPACITOR ACTIVE CELL BALANCING							
	Active cell balancing circuitry quiescent current into VOUT		HC_SEL = 1, storage capacitor balanced –40°C ≤ T_J ≤ 85°C		1.7	6	µA
	Active cell balancing accuracy		(VOUT – BAL) vs BAL voltage difference Storage capacitor balanced HC_SEL = 1 V_{OUT} = 5.7 V	–100		100	mV
	BAL output drive capability		V_{OUT} = 4.95 V, Sink and source current	±10	±15		mA
	Active discharge resistor		HC_SEL = 0, device in shutdown mode VOUT to BAL and BAL to GND		0.85	1.5	kΩ
LED TEMPERATURE MONITORING (TPS61305, TPS61035A)							
$I_{O(TS)}$	Temperature Sense Current Source		Thermistor bias current		23.8		µA
	TS Resistance (Warning Temperature)		LEDWARN bit = 1, T_J ≥ 25°C	39	44.5	50	kΩ
	TS Resistance (Hot Temperature)		LEDHOT bit = 1, T_J ≥ 25°C	12.5	14.5	16.5	kΩ
SDA, SCL, GPIO/PG, ENVM, Tx-MASK, ENDCL, NRESET, FLASH_SYNC, HC_SEL							
$V_{(IH)}$	High-level input voltage			1.2			V
$V_{(IL)}$	Low-level input voltage					0.4	V
$V_{(OL)}$	Low-level output voltage (SDA)		I_{OL} = 8 mA			0.3	V
	Low-level output voltage (GPIO)		DIR = 1, I_{OL} = 5 mA			0.3	
$V_{(OH)}$	High-level output voltage (GPIO)		DIR = 1, GPIOTYPE = 0, I_{OH} = 8 mA	V_{IN} – 0.4			V

Electrical Characteristics (continued)

Unless otherwise noted the specification applies for V_{IN} = 3.6 V over an operating junction temperature T_J = –40°C to 125°C; Circuit of (unless otherwise noted). Typical values are for T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(LKG)}$	Logic input leakage current	Input connected to VIN or GND –40°C ≤ T_J ≤ 85°C		0.01	0.1	µA
R_{PD}	ENVM pull-down resistance	ENVM ≤ 0.4 V		350		kΩ
	ENDCL, NRESET pull-down resistance	ENDCL, NRESET ≤ 0.4 V		350		
	FLASH_SYNC pull-down resistance	FLASH_SYNC ≤ 0.4 V		350		
	Tx-MASK pull-down resistance	Tx-MASK ≤ 0.4 V		350		
	HC_SEL pull-down resistance	HC_SEL ≤ 0.4 V		350		
$C_{(IN)}$	SDA input capacitance	SDA = VIN or GND		9		pF
	SCL input capacitance	SCL = VIN or GND		4		
	GPIO/PG input capacitance	DIR = 0, GPIO/PG = VIN or GND		9		
	ENVM input capacitance	ENVM = VIN or GND		4		
	ENDCL input capacitance	ENDCL = VIN or GND		3		
	HC_SEL input capacitance	HC_SEL = VIN or GND		3.5		
	Tx-MASK input capacitance	Tx-MASK = VIN or GND		4		
	FLASH_SYNC input capacitance	FLASH_SYNC = VIN or GND		3		
TIMING						
t_{NRESET}	Reset pulse width		10			µs
	Start-up time	From shutdown into DC light mode HC_SEL = 0, I_{LED} = 100 mA		1.4		ms
		From shutdown into voltage mode through ENVM, HC_SEL = 0, I_{OUT} = 0 mA		550		µs
	LED current settling time(2) triggered by a rising edge on FLASH_SYNC	MODE_CTRL[1:0] = 10, HC_SEL = 0 I_{LED2} = from 0 mA to 800 mA		400		µs
		MODE_CTRL[1:0] = 10, HC_SEL = 1 I_{LED2} = from 0 mA to 1800 mA		16		
	LED current settling time(2) triggered by Tx-MASK	MODE_CTRL[1:0] = 10, HC_SEL = 0 I_{LED2} = from 800 mA to 350 mA		15		µs

(2) Settling time to ±15% of the target value.

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency	Standard mode		100	kHz
		Fast mode		400	
		High-speed mode (write operation), C_B – 100 pF maximum		3.4	MHz
		High-speed mode (read operation), C_B – 100 pF maximum		3.4	
		High-speed mode (write operation), C_B – 400 pF maximum		1.7	
		High-speed mode (read operation), C_B – 400 pF maximum		1.7	
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7		µs
		Fast mode	1.3		
t_{HD}, t_{STA}	Hold time (repeated) START condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		

Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7		µs
		Fast mode	1.3		
		High-speed mode, C_B – 100 pF maximum	160		ns
		High-speed mode, C_B – 400 pF maximum	320		
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode, C_B – 100 pF maximum	60		
		High-speed mode, C_B – 400 pF maximum	120		
t_{SU}, t_{STA}	Setup time for a repeated START condition	Standard mode	4.7		µs
		Fast mode	600		ns
		High-speed mode	160		
t_{SU}, t_{DAT}	Data setup time	Standard mode	250		ns
		Fast mode	100		
		High-speed mode	10		
t_{HD}, t_{DAT}	Data hold time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	
		High-speed mode, C_B – 100 pF maximum	0	70	ns
		High-speed mode, C_B – 400 pF maximum	0	150	
t_{RCL}	Rise time of SCL signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	
		High-speed mode, C_B – 100 pF maximum	10	40	
		High-speed mode, C_B – 400 pF maximum	20	80	
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge BIT	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	
		High-speed mode, C_B – 100 pF maximum	10	80	
		High-speed mode, C_B – 400 pF maximum	20	160	
t_{FCL}	Fall time of SCL signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	
		High-speed mode, C_B – 100 pF maximum	10	40	
		High-speed mode, C_B – 400 pF maximum	20	80	
t_{RDA}	Rise time of SDA signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	
		High-speed mode, C_B – 100 pF maximum	10	80	
		High-speed mode, C_B – 400 pF maximum	20	160	
t_{FDA}	Fall time of SDA signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	
		High-speed mode, C_B – 100 pF maximum	10	80	
		High-speed mode, C_B – 400 pF maximum	20	160	
t_{SU}, t_{STO}	Setup time for STOP condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		
C_B	Capacitive load for SDA and SCL			400	pF

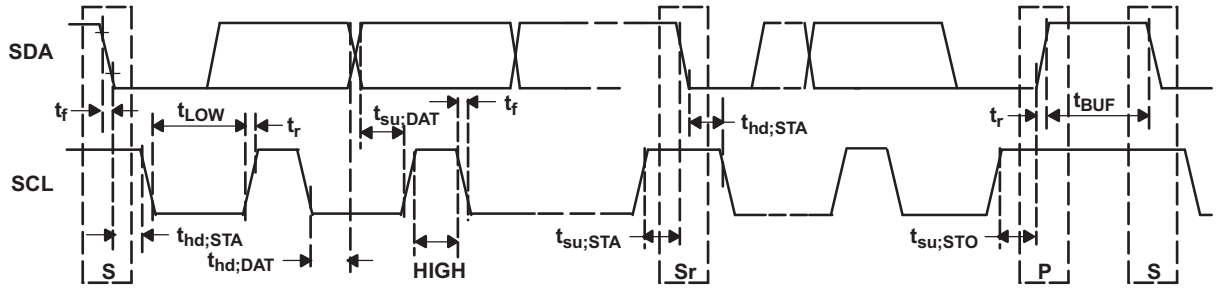
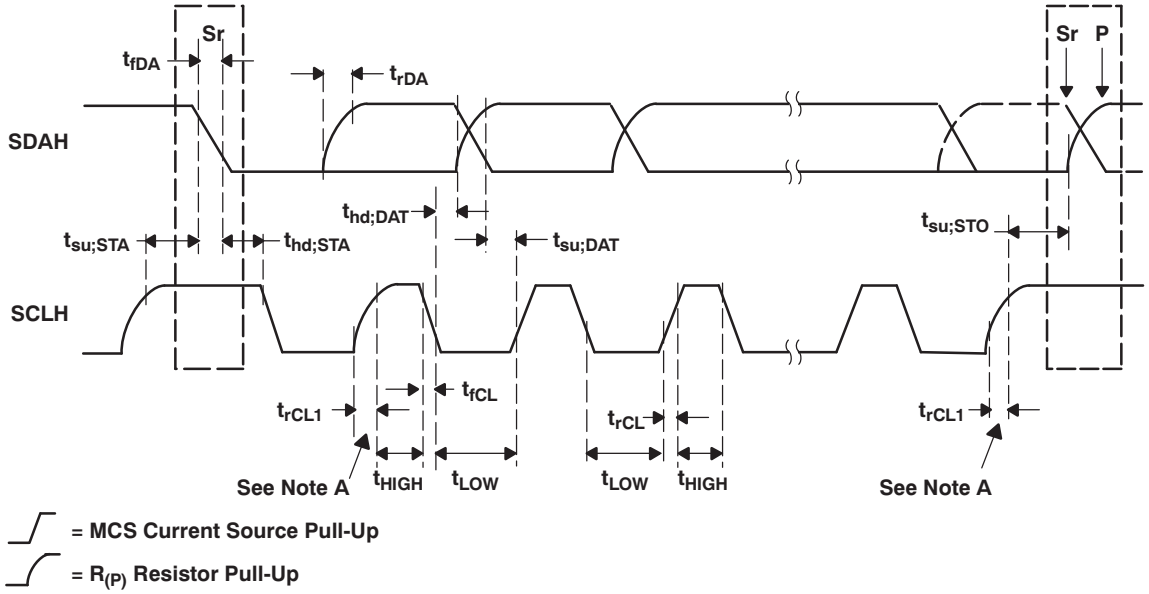


Figure 2. Serial Interface Timing for F/S-Mode



Note A: First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 3. Serial Interface Timing for HS-Mode

7.7 Typical Characteristics

TABLE OF GRAPHS		FIGURE NO.
LED Power Efficiency	vs Input Voltage	Figure 4, Figure 5
DC Input Current	vs Input Voltage	Figure 6
LED Current	vs LED Pin Headroom Voltage	Figure 7, Figure 8, Figure 9
LED Current	vs LED Current Digital Code	Figure 10, Figure 11, Figure 12, Figure 13
INDLED Current	vs LED Pin Headroom Voltage	Figure 14
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Maximum Output Current	vs Input Voltage	Figure 19
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Valley Current Limit		Figure 22, Figure 23
Balancing Current	vs Balance Pin Voltage	Figure 24
Supply Current	vs Input Voltage	Figure 25
Standby Current	vs Ambient Temperature	Figure 26
Temperature Detection Threshold		Figure 27, Figure 28
Junction Temperature	vs Port Voltage	Figure 29

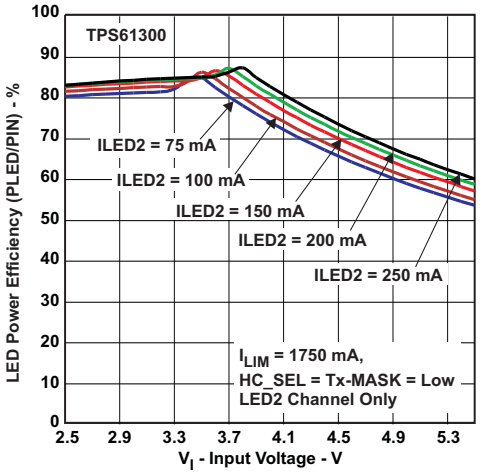

Figure 4. LED Power Efficiency vs Input Voltage

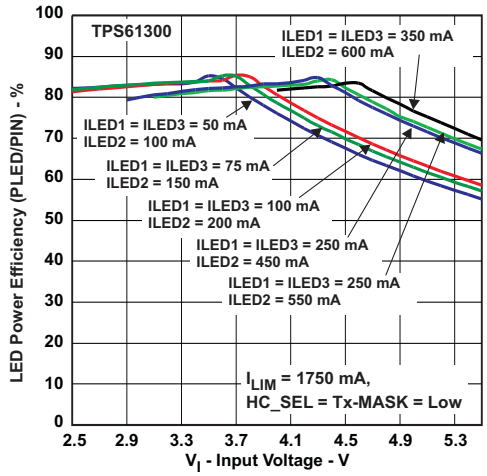

Figure 5. LED Power Efficiency vs Input Voltage

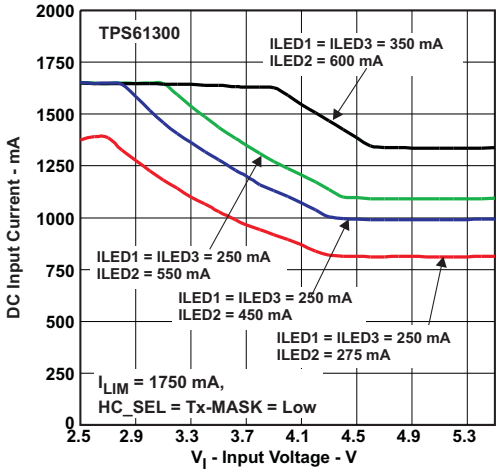

Figure 6. DC Input Current vs Input Voltage

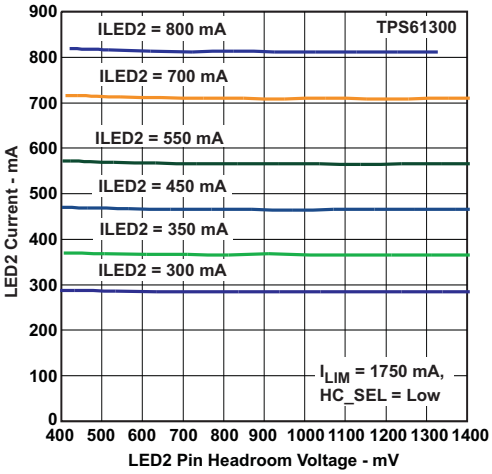

Figure 7. LED2 Current vs LED2 Pin Headroom Voltage (HC_SEL = 0)

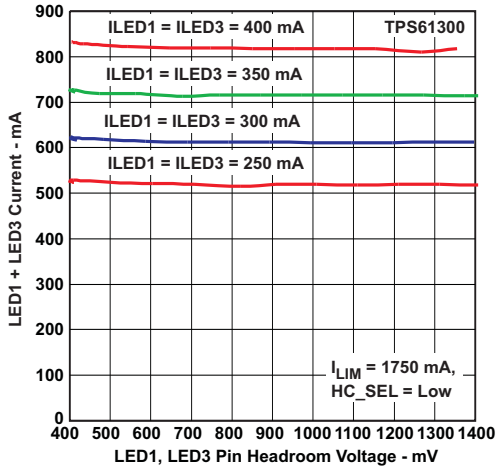

Figure 8. LED1+LED3 Current vs LED1+LED3 Pin Headroom Voltage (HC_SEL = 0)

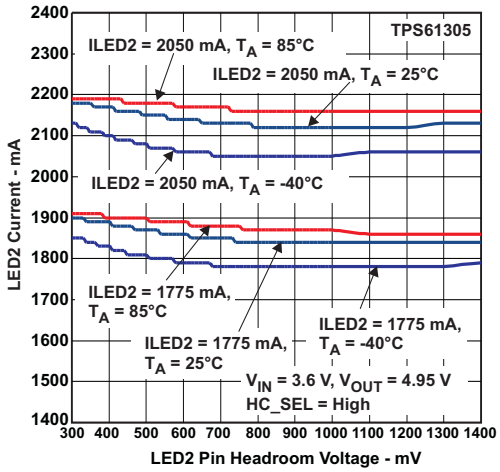

Figure 9. LED2 Current vs LED2 Pin Headroom Voltage (HC_SEL = 1)

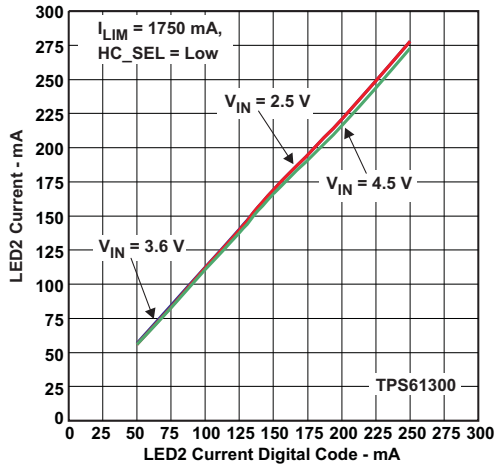

Figure 10. LED2 Current vs LED2 Current Digital Code (HC_SEL = 0)

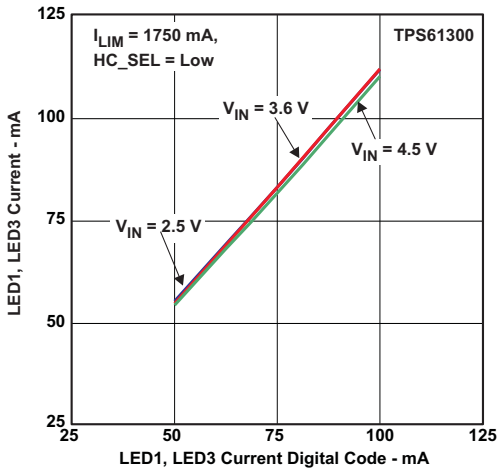

Figure 11. LED1, LED3 Current vs LED1, LED3 Current Digital Code (HC_SEL = 0)

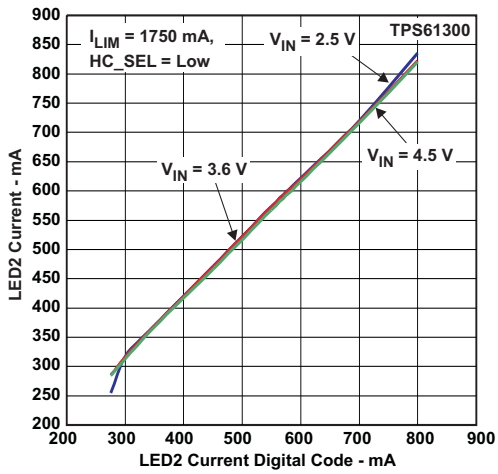

Figure 12. LED2 Current vs LED2 Current Digital Code (HC_SEL = 0)

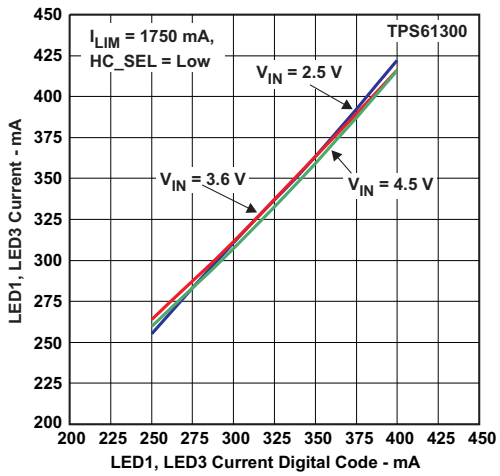

Figure 13. LED1, LED3 Current vs LED1, LED3 Current Digital Code (HC_SEL = 0)

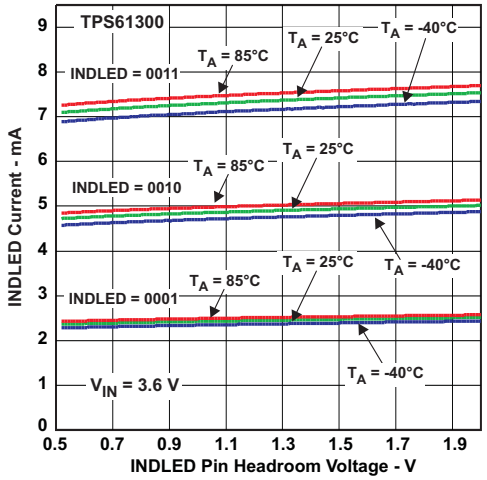

Figure 14. INDLED Current vs INDLED Pin Headroom Voltage

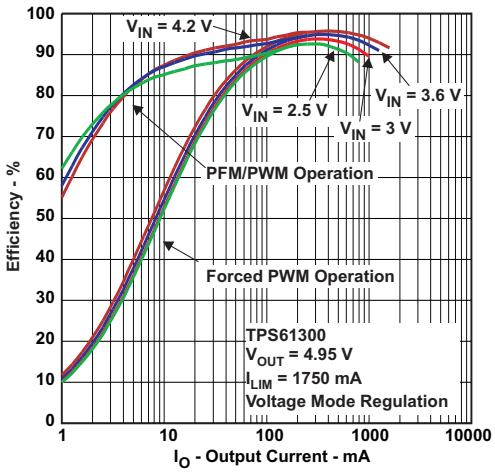

Figure 15. Efficiency vs Output Current

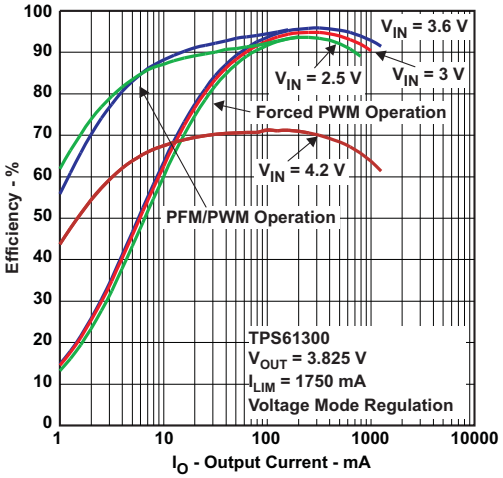

Figure 16. Efficiency vs Output Current

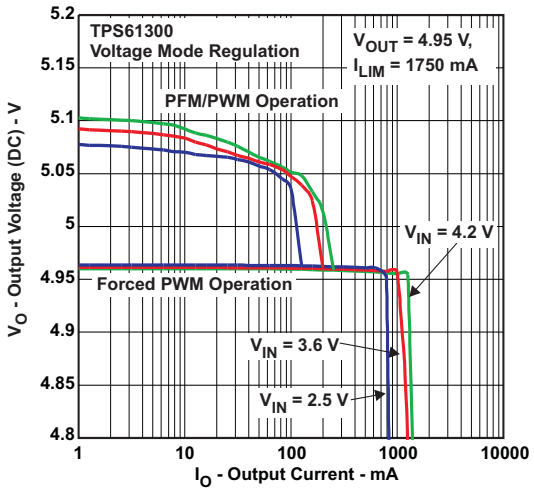

Figure 17. DC Output Voltage vs Load Current

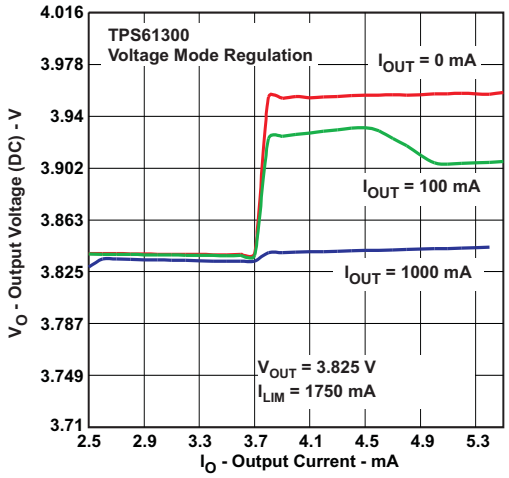

Figure 18. DC Output Voltage vs Load Current

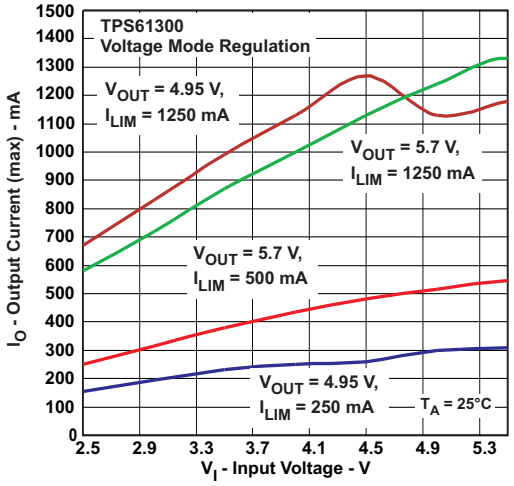

Figure 19. Maximum Output Current vs Input Voltage

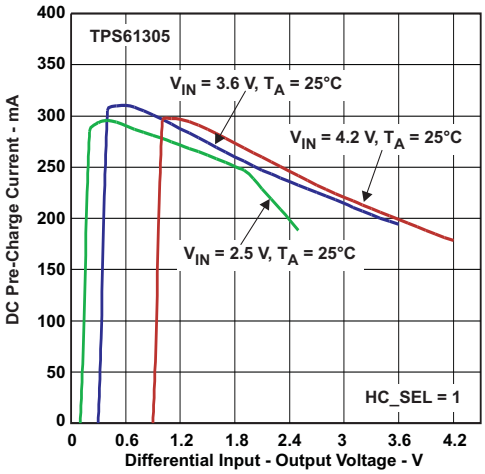

Figure 20. DC Precharge Current vs Differential Input-Output Voltage (HC_SEL = 1)

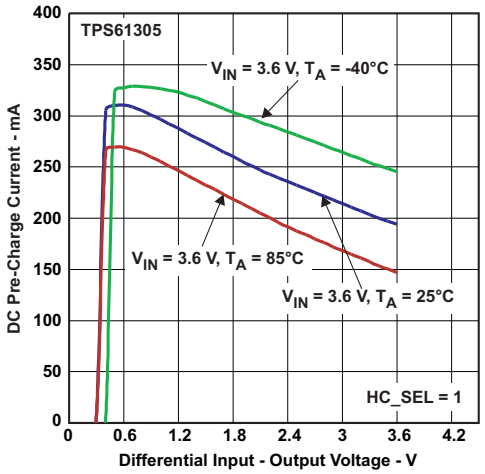

Figure 21. DC Precharge Current vs Differential Input-Output Voltage (HC_SEL = 1)

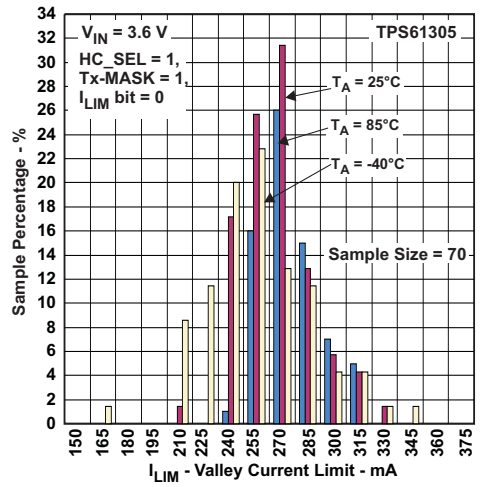

Figure 22. Valley Current Limit (HC_SEL = 1)

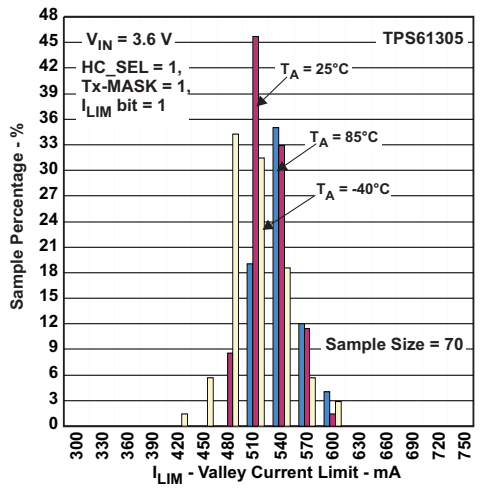

Figure 23. Valley Current Limit (HC_SEL = 1)

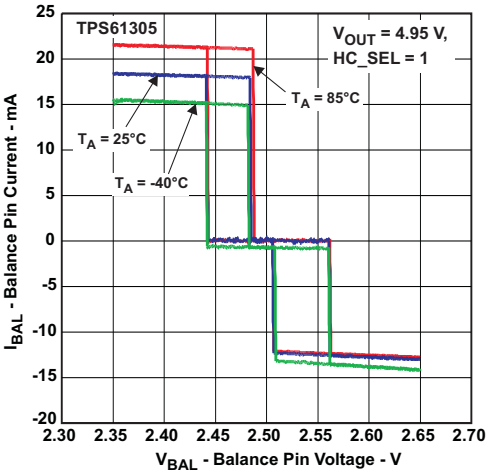

Figure 24. Balancing Current vs Balance Pin Voltage

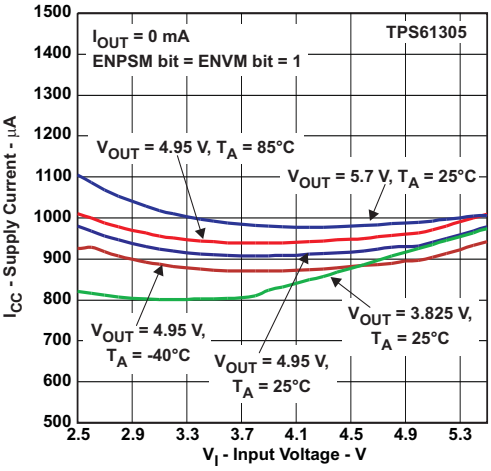

Figure 25. Supply Current vs Input Voltage

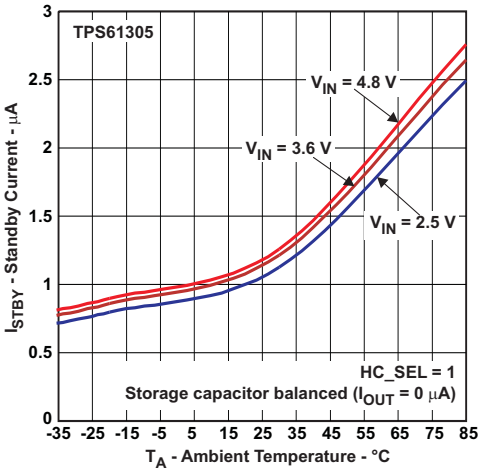

Figure 26. Standby Current vs Ambient Temperature (HC_SEL = 1)

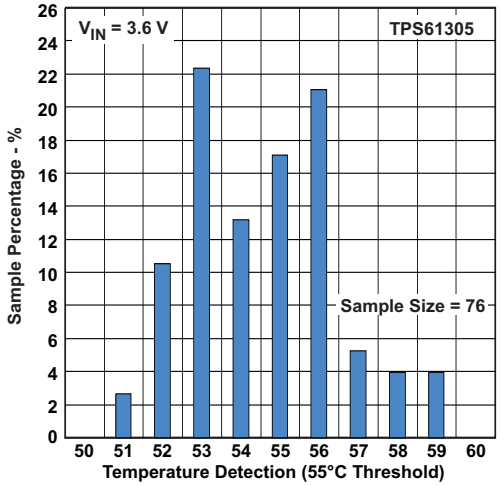

Figure 27. Temperature Detection Threshold

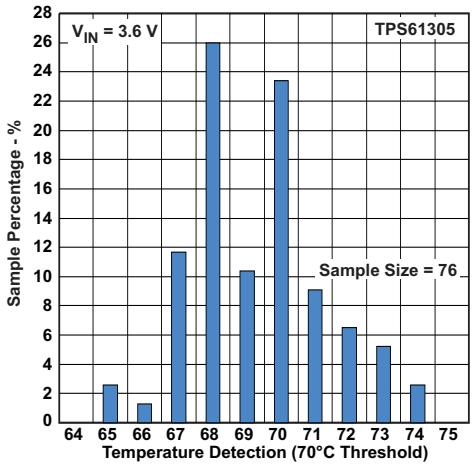

Figure 28. Temperature Detection Threshold

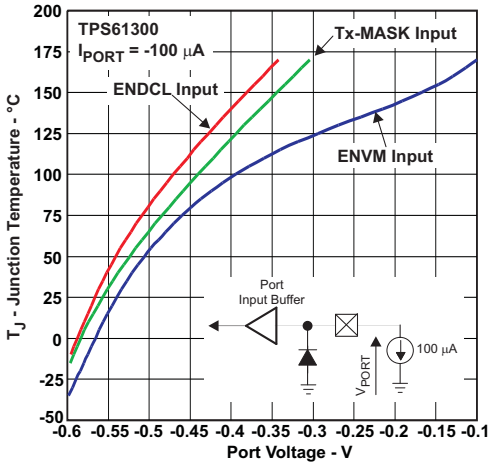

Figure 29. Junction Temperature vs Port Voltage

8 Detailed Description

8.1 Overview

The TPS6130xx family employs a 2-MHz fixed ON-time, PWM current-mode converter to generate the output voltage required to drive up to three high-power LEDs in parallel. The device integrates a power stage based on an NMOS switch and a synchronous PMOS rectifier. The device also implements a set of linear low-side current regulators to control the LED current when the battery voltage is higher than the diode forward voltage.

A special circuit is applied to disconnect the load from the battery during shutdown of the converter. In conventional synchronous rectifier circuits, the back-gate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device, however, uses a special circuit which takes the cathode of the back-gate diode of the high-side PMOS and disconnects it from the source when the regulator is in shutdown (HC_SEL = L).

The TPS6130xx device cannot only operate as a regulated current source but also as a standard voltage boost regulator featuring power-save mode for improved efficiency at light load. The voltage mode operation can be activated either by a software command or by means of a hardware signal (ENVM). This additional operating mode can be useful to properly synchronize the converter when supplying other high power consuming devices in the system, such as hands-free audio power amplifiers, or any other component requiring a supply voltage higher than the battery voltage.

The TPS6130xx device also supports storage capacitor on its output (so called energy storage mode). In this operating mode (HC_SEL = H), the inductive power stage is used to charge up the super-capacitor to a user-selectable value. Once the charge-up is complete, the LEDs can be fired up to 1025 mA (LED1 and LED3) and 2050 mA (LED2) without causing a battery overload.

In general, a boost converter only regulates output voltages which are higher than the input voltage. This device operates differently. For example, in the voltage mode operation the device is capable of regulating 4.2 V at the output from a battery voltage pulsing as high 5.5 V. To control these applications properly, a down-conversion mode is implemented.

If the input voltage reaches or exceeds the output voltage, the converter changes to a down-conversion mode. In this mode, the control circuit changes the behavior of the rectifying PMOS. It sets the voltage drop across the PMOS as high as needed to regulate the output voltage. This means the power losses in the converter increase. This must be considered for thermal consideration.

In direct drive mode (HC_SEL = L), the power stage is capable of supplying a maximum total current of roughly 1300 to 1500 mA. The TPS61300 provides three constant current inputs, capable of sinking up to 400 mA (LED1 and LED3) and 800 mA (LED2) in flashlight mode.

The TPS6130xx integrates an I^2C compatible interface allowing transfers up to 3.4 Mbits/s. This communication interface can be used to set the operating mode (shutdown, constant output current mode vs constant output voltage mode), to control the brightness of the external LED (DC light and flashlight modes), to adjust the output voltage (between 3.825 V and 5.7 V in 125-mV steps) or to program the safety timer for instance. See *Register Maps*.

In the TPS6130xx device, the DC light and flash can be controlled either by the I^2C interface or by the means of hardware control signals (ENDCL and FLASH_SYNC). To simplify flashlight synchronization with the camera module, the device offers a FLASH_SYNC strobe input pin to turn, with zero latency, the LED current from DC light to flashlight.

The maximum duration of the flashlight pulse can be limited by means of an internal user programmable safety timer (STIM). To avoid the LEDs to be kept accidentally ON in DC light mode by software control, the device implements a 11.2-s watchdog timer.

8.2 Functional Block Diagrams

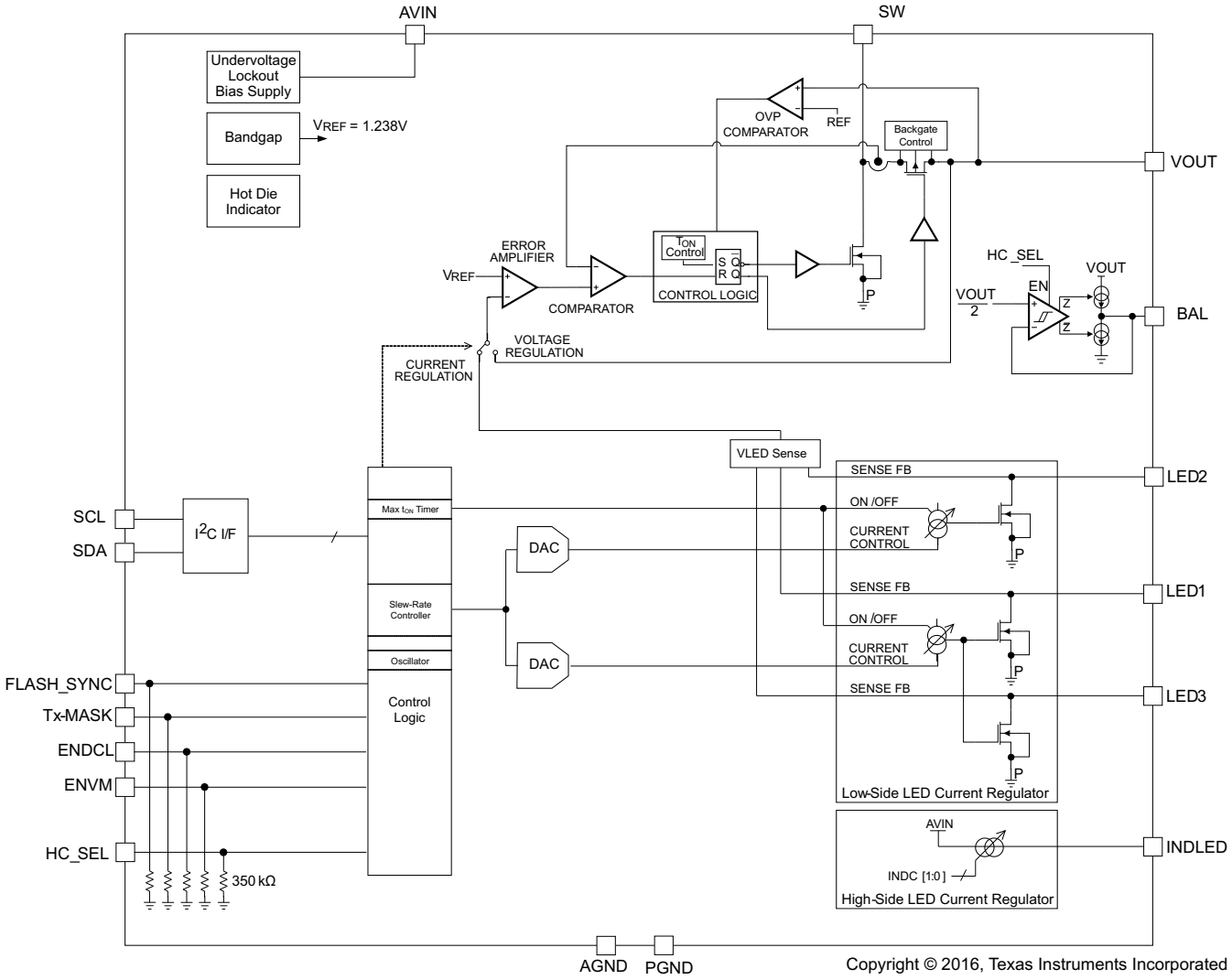

Figure 30. TPS61300 Block Diagram

Functional Block Diagrams (continued)

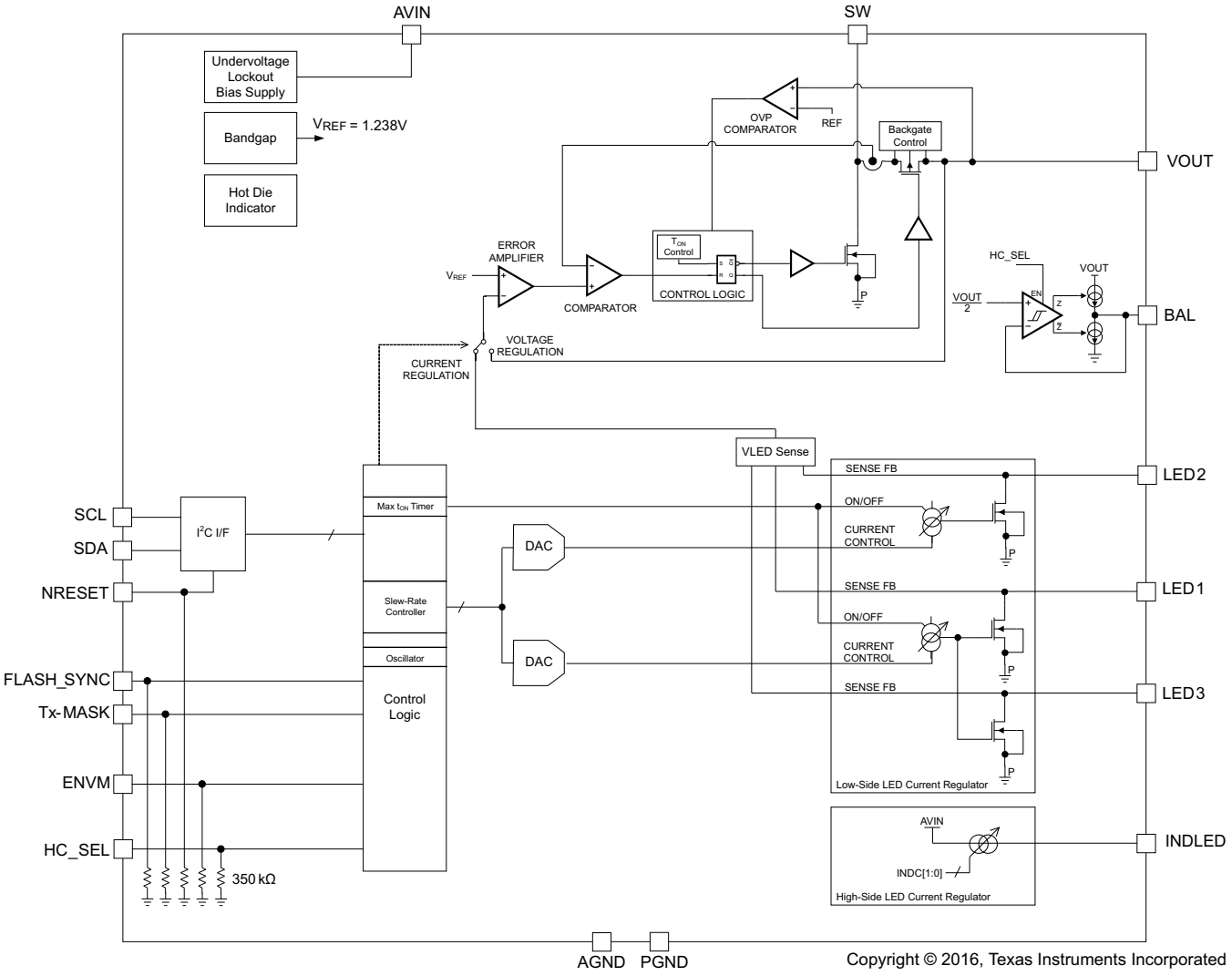

Figure 31. TPS61301 Block Diagram

Functional Block Diagrams (continued)

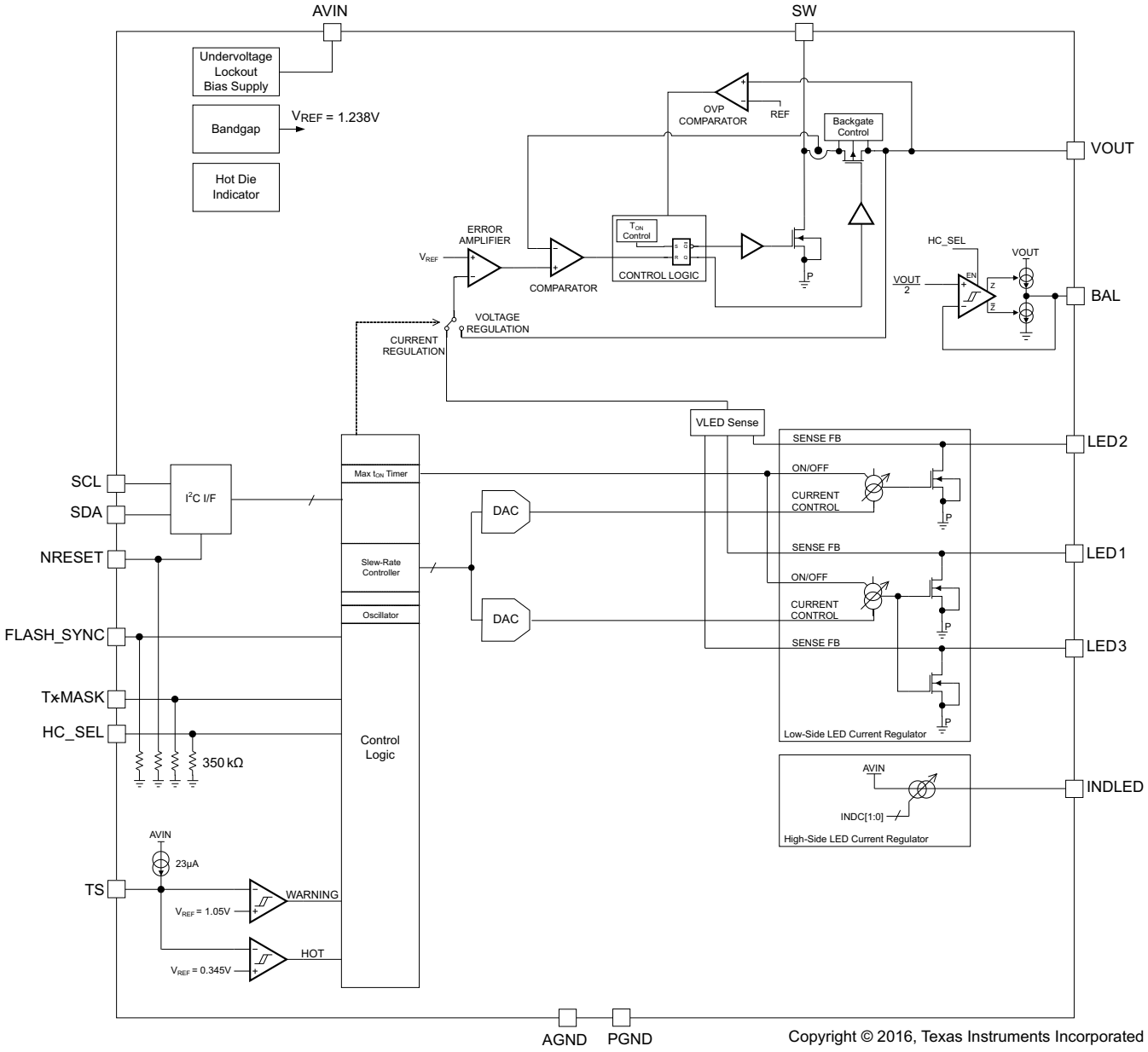

Figure 32. TPS61305, TPS61305A Block Diagrams

Functional Block Diagrams (continued)

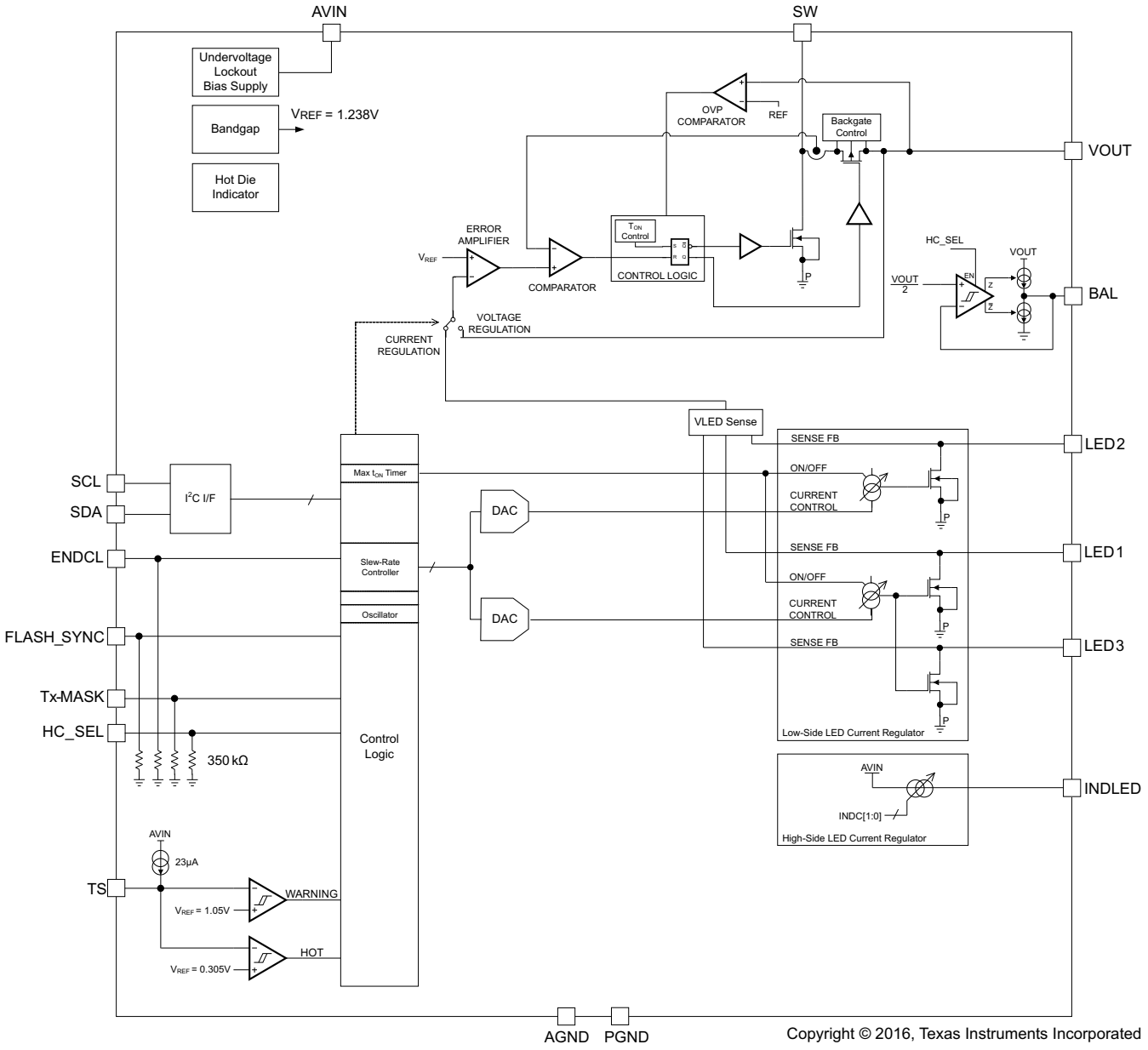

Figure 33. TPS61306 Block Diagram

Functional Block Diagrams (continued)

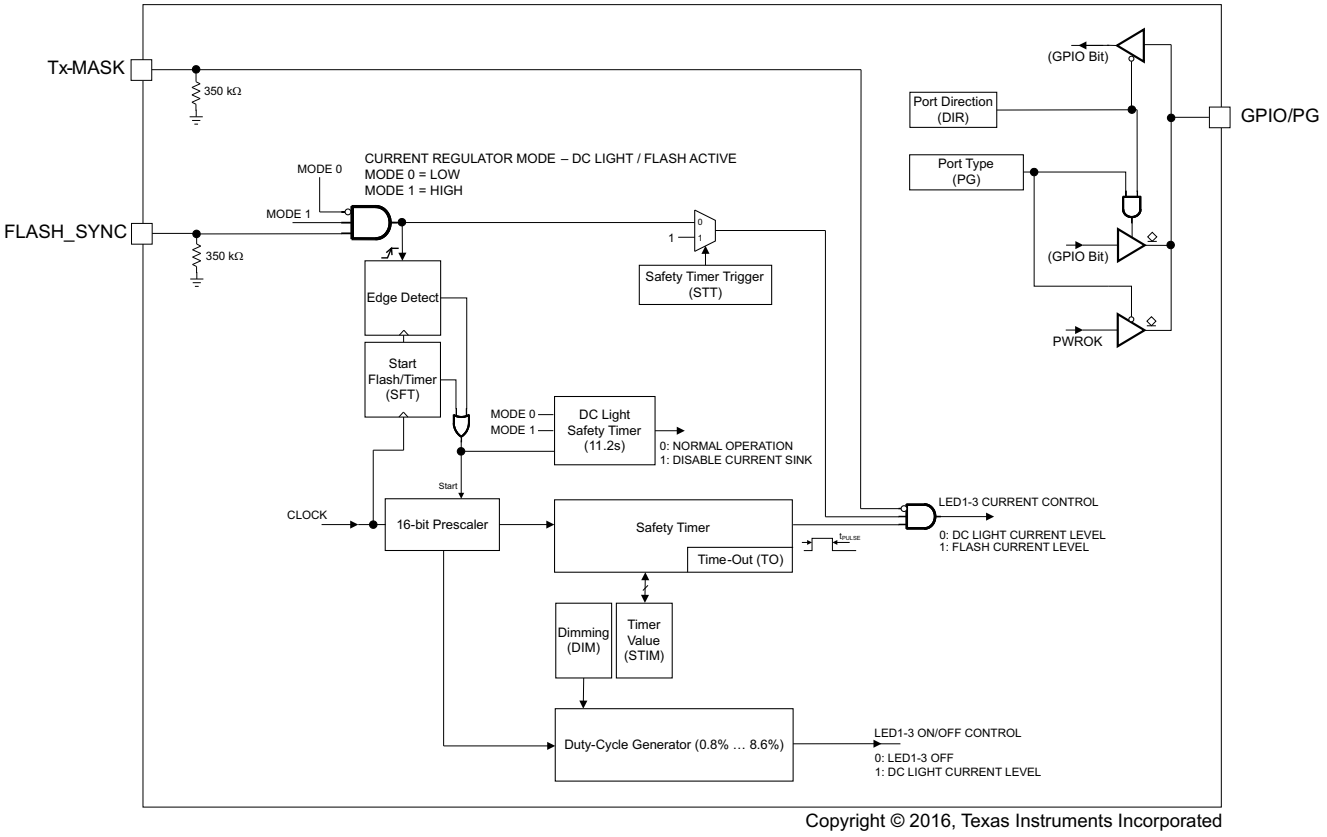

Figure 34. Timer Block Diagram Block Diagram

8.3 Feature Description

8.3.1 Safety Timer Accuracy

The LED strobe timer uses the internal oscillator as reference clock. The timer execution speed (see *REGISTER3* for more information on STIM[2:0]) scales according to the reference clock accuracy.

Table 3. Frequency for Safety Timer

OSCILLATOR FREQUENCY	SAFETY TIMER DURATION
Minimum	Maximum = Typical × (1 + f_{ACC})(1)
Typical	Typical(2)
Maximum	Minimum = Typical x (1 – f_{ACC})(1)

(1) See *REGISTER3* for more information.
(2) See *Electrical Characteristics*.

8.3.2 LED Failure Modes and Overvoltage Protection

If a high-power LED fails as a short circuit, the low-side current regulator will limit the maximum output current and the HIGH-POWER LED FAILURE (HPLF) flag will be set.

If a high-power LED fails as an open circuit, the control loop will initially attempt to regulate off of its low-side current regulator feedback signal. This will drive VOUT higher. Because the open-circuited LED will never accept its programmed current, V_{OUT} must be voltage-limited by means of a secondary control loop.

The TPS6130xx device limits V_{OUT} according to the overvoltage protection settings (refer to the OVP specification). In this failure mode, V_{OUT} is either limited to 4.65 V (typical) or 6 V (typical) and the HIGH-POWER LED FAILURE (HPLF) flag is set.

Table 4. Overvoltage Protection Threshold

OVP THRESHOLD	OPERATING CONDITIONS
4.65-V typical	HC_SEL = L and 0000 ≤ OV[3:0] ≤ 0100
6-V typical	HC_SEL = H or 0101 ≤ OV[3:0] ≤ 1111

See *LED High-Current Regulators, Unused Inputs* for more information.

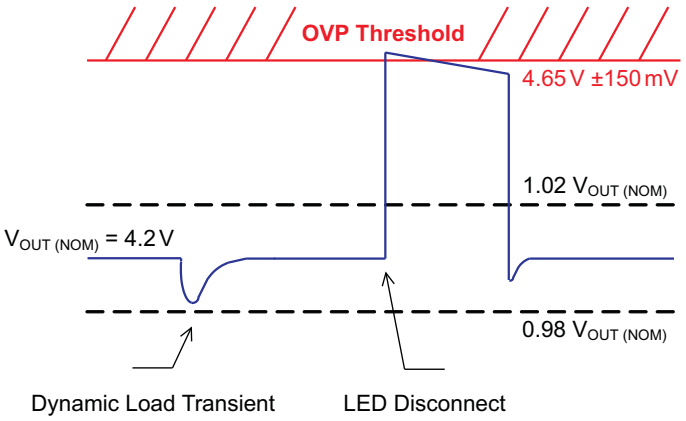

Figure 35. Overvoltage Protection Operation (4.65-V Typical)

8.3.3 Start-Up Sequence

To avoid high inrush current during start-up, take special care to control the inrush current. When the device enables, the internal start-up cycle starts with the first step, the precharge phase.

During precharge, the rectifying switch is turned on until the output capacitor is either charged to a value close to the input voltage or ≈3.3 V, whichever occurs first. The rectifying switch is current-limited during that phase. The current limit increases with decreasing input to output voltage difference. This circuit also limits the output current under short-circuit conditions at the output. Figure 36 shows the typical precharge current vs input minus the output voltage for a specific input voltage.

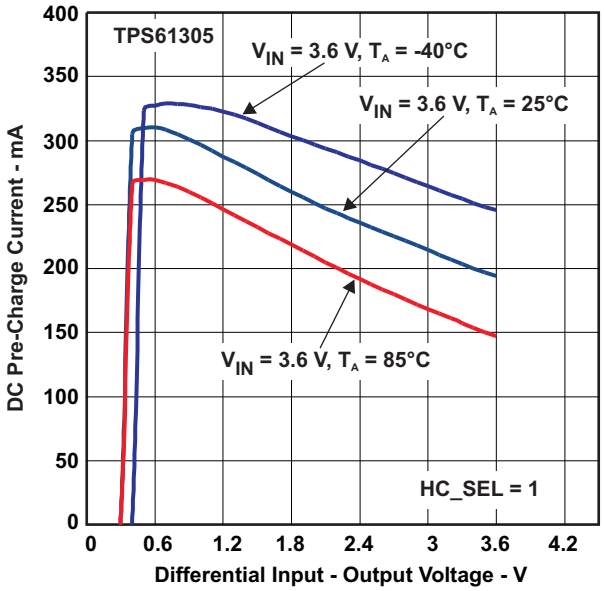

Figure 36. Typical DC Precharge and Short-Circuit Current

In direct drive mode (HC_SEL = L, TPS6130xx), after having precharged the output capacitor, the device starts-up switching and increases its current limit in three steps of typically 250 mA, 500 mA, and full current limit (ILIM setting). The current limit transitions from the first to the second step occurs after a milli-second operation. Full current limit operation is set once the output voltage has reached its regulation limits. In this mode, the active balancing circuit is disabled.

In high-current mode (HC_SEL = H), the precharge voltage of the storage capacitor is depending on the input voltage and operating mode (for example, voltage regulation vs current regulation mode). In case the device is set for exclusive current regulation operation (that is, MODE_CTRL[1:0] = 01 or 10 and ENVM = 0), the output capacitor precharge voltage will be close to the input voltage. Under all other operating conditions, the precharge voltage will either be close to the input voltage or to approximately 3.3 V, whichever is lower.

After having precharged the storage capacitor, the device starts-up switching. During down-mode operation, the inductor valley current is actively limited either to 250 mA or 500 mA (refer to ILIM setting). As the device enters boost mode operation, the current limit transitions to its full capability (refer to ILIM setting and Tx-MASK input logic state). As a consequence, the output voltage ramps up linearly and the start-up time needed to reach the programmed output voltage (see *REGISTER6 (TPS61300, TPS61301)* or *REGISTER6 (TPS61305, TPS61305A)* for the OV[3:0] bits) will mainly depend on the super-capacitor value and load current. In this mode, the active balancing circuit is enabled.

8.3.4 Power Good (Flash Ready)

The TPS6130xx integrates a power good circuitry that is activated when the device is operating in voltage regulation mode (MODE_CTRL[1:0] = 11 or ENVM = 1). In shutdown mode (MODE_CTRL[1:0] = 00, ENDCL = 0 and ENVM = 0), the GPIO/PG pin state is defined in Table 5.

Table 5. GPIO Connection

GPIOTYPE	GPIO/PG SHUTDOWN STATE
0	Reset/pulled to ground
1	Open-drain

Depending on the GPIO/PG output stage type selection (push-pull or open-drain), the polarity of the power-good output signal (PG) can be inverted or not. The power-good software bit and hardware signal polarity is defined in Table 6.

Table 6. GPIO and PG Status

GPIOTYPE	PG BIT	GPIO/PG OUTPUT PORT	COMMENTS
0: push-pull output	0	0	Output is active high signal polarity
	1	1	
1: open-drain output	0	Open-drain	Output is active low signal polarity
	1	Low	

The power good signal is valid when the output voltage is within –1.5% and 2.5% of its nominal value. Conversely, it is asserted low when the voltage mode operation gets suspended (MODE_CTRL[1:0] ≠ 11 and ENVM = 0).

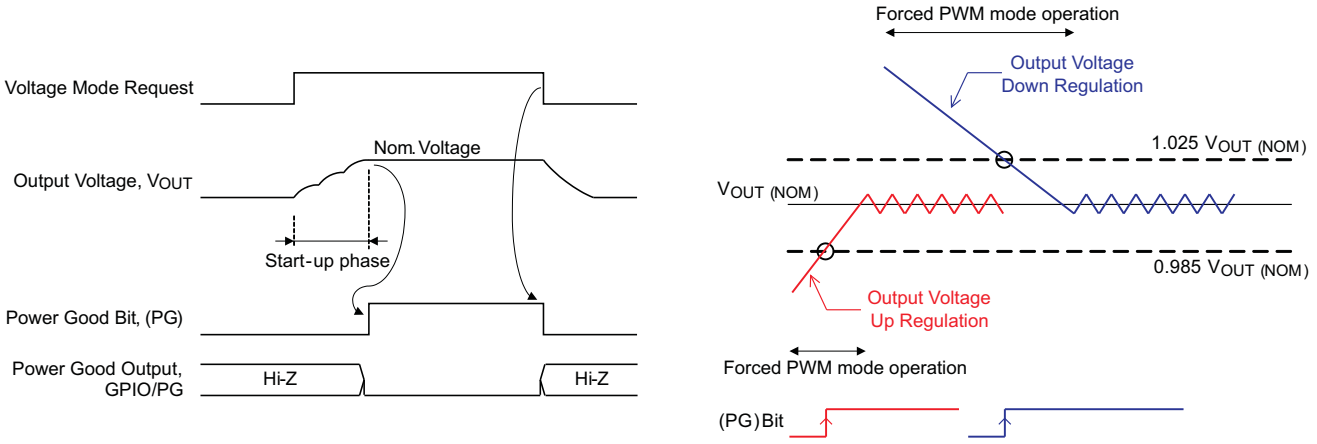

Figure 37. Power Good Operation (DIR = 1, GPIOTYPE = 1)

The TPS6130xx device uses a control architecture that allows recycling of excessive energy that might be stored in the output capacitor. By reversing the operation of the boost power stage, the converter is capable of transferring energy from its output back into the input source. In this case, the power good signal is deasserted whilst the output voltage is decreasing towards its target value. For example the closest fit voltage the converter can support. See *Down-Mode in Voltage Regulation Mode* for additional information.

8.3.5 LED Temperature Monitoring (TPS61305, TPS61305A, TPS61306)

The TPS61305, TPS61305A, and TPS61306 devices monitor the LED temperature by measuring the voltage between the TS and AGND pins. An internal current source provides the bias (≈24 µA) for a negative-temperature coefficient resistor (NTC), and the TS pin voltage is compared to internal thresholds (1.05 V and 0.345 V) to protect the LEDs against overheating.

The temperature monitoring related blocks are always active in DC light or flashlight modes. In voltage mode operation (MODE_CTRL[1:0] = 11), the device only activates the TS input when the ENTS bit is set to high. In shutdown mode, the LED temperature supervision is disabled and the quiescent current of the device is dramatically reduced.

The LEDWARN and LEDHOT bits reflect the LED temperature. The LEDWARN bit is set when the voltage seen at the TS pin is lower than 1.05 V. This threshold corresponds to an LED warning temperature value, the device operation is still permitted.

While regulating LED current (for example, DC light or flashlight modes), the LEDHOT bit is latched when the voltage seen at the TS pin is lower than 0.345 V. This threshold corresponds to an excessive LED temperature value, the device operation is immediately suspended (MODE_CTRL[1:0] bits are reset and HOTDIE[1:0] bits are set).

8.3.6 Hot Die Detector

The hot die detector monitors the junction temperature but does not shutdown the device. It provides an early warning to the camera engine to avoid excessive power dissipation thus preventing from thermal shutdown during the next high-power flash strobe.

The hot die detector (HOTDIE[1:0] bits) reflects the instantaneous junction temperature and is always enabled excepted when the device is in shutdown mode (MODE_CTRL[1:0] = 00, ENVM = 0 and ENDCL = 0).

8.3.7 NRESET Input: Hardware Enable and Disable

Some devices out of the TPS6130xx family feature a hardware reset pin (NRESET). This reset pin allows the device to be disabled by an external controller without requiring an I^2C write command. Under normal operation, the NRESET pin must be held high to prevent an unwanted reset. When the NRESET is driven low, the I^2C control interface and all internal control registers are reset to the default states and the part enters shutdown mode.

8.3.8 ENDCL Input: DC Light Hardware Control

Some devices out of the TPS6130xx family feature a dedicated DC light control input (ENDCL). This logic input can be used to turn on the LEDs for DC light operation. This hardware control pin can be useful to control the torch light functionality from a separate engine (for example, base-band). In this mode of operation, the DC light safety timer is not activated.

The ENDCL input is only active when the device is programmed into shutdown (MODE_CTRL[1:0] = 00) or into voltage regulation mode (MODE_CTRL[1:0] = 11 or ENVM = 1) and the indicator control is turned off (INDC[3:0] = 0000). LED1–3 inputs are controlled according to ENLED[3:1] bit settings.

8.3.9 Flashlight Blanking (Tx-MASK)

In direct drive mode (HC_SEL = 0), the Tx-MASK input signal can be used to disable the flashlight operation, for example, during a RF PA transmission pulse. This blanking function turns the LED from flashlight to DC light thereby reducing almost instantaneously the peak current loading from the battery. The Tx-MASK function has no influence on the safety timer duration.

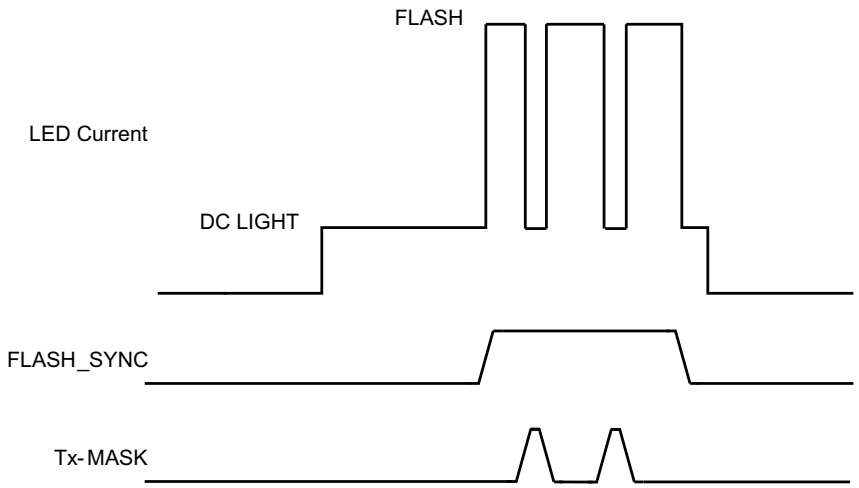

Figure 38. Synchronized Flashlight With Blanking Periods

In high-current mode (HC_SEL = 1), the Tx-MASK input pin is also used to dynamically adjusts the device's current limit setting which controls the maximum current drawn from the input source. See *Current Limit Operation* for more information.

8.3.10 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from mis-operation at low input voltages. It prevents the converter from turning on the switch-MOSFET, or rectifier-MOSFET for battery voltages below 2.3 V. The I^2C compatible interface is fully functional down to 2.1-V input voltage.

8.3.11 Storage Capacitor Active Cell Balancing

A fully charged super-capacitor will typically have leakage current of under 1 µA. The TPS6130xx device integrates an active balancing feature to cut the total leakage current from the super-capacitor and balance circuit to less than 1.7 µA typically.

The device integrates a window comparator monitoring the tap point of the multi-cell super-capacitor. The balancing output (BAL) is substantially half the actual output voltage (V_{OUT}). If the internal leakage current in one of the capacitors is larger than that in the other, then the voltage at their junction will tend to change in such a way that the voltage on the capacitor with the larger (or largest) leakage current will reduce.

When this happens, a current will begin to flow from the BAL output in such a direction as to reduce the amount by which the voltage changes. The current that will flow after a long period of steady-state conditions will be approximately equal to the difference between the leakage currents of the pair of capacitors which is being balanced by the circuit. The output resistance of the balancing circuit (≈250 Ω) determines how quickly an imbalance will be corrected.

8.3.12 RED Light Privacy Indicator

The TPS6130xx device provides a high-side linear constant current source to drive low VF LEDs. The LED current is directly regulated off the battery and can be controlled through the INDC[3:0] bits. Operation is understood best by referring to the Figure 39 and Figure 40.

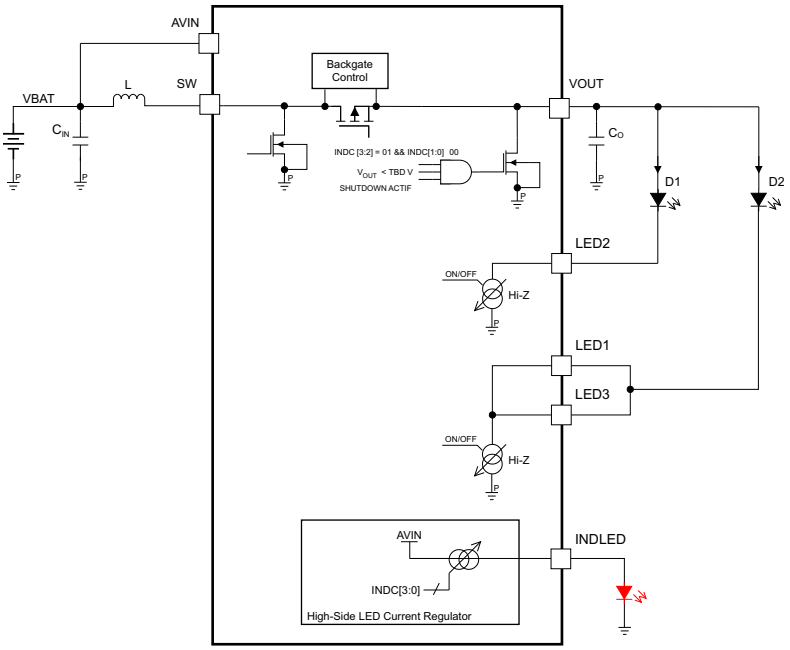

Figure 39. RED Light Indicator, Configuration 1

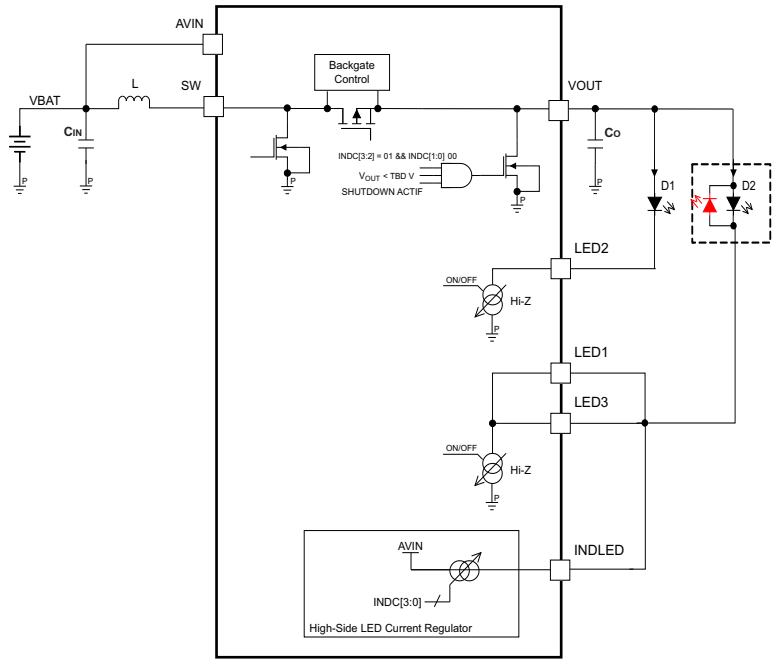

Figure 40. RED Light Indicator, Configuration 2

The device can provide a path to allow for reverse biasing of white LEDs (see Figure 40). To do so, the output of the converter (VOUT) is pulled to ground, thus allowing a reverse current to flow. This mode of operation is only possible when the converter's power stage is in shutdown (MODE_CTRL[1:0] = 00, ENVM = 0, ENDCL = 0 and HC_SEL = 0).

8.3.13 White LED Privacy Indicator

The TPS6130xx device features white LED drive capability at very low light intensity. To generate a reduced LED average current, the device employs a 122-Hz fixed frequency PWM modulation scheme. Operation is understood best by referring to the timer block diagram.

The DC light current is modulated with a duty cycle defined by the INDC[3:0] bits. The low light dimming mode can only be activated in the software controlled DC light only mode (MODE_CTRL[1:0] = 01, ENVM = X, ENDCL = 0) and applies to the LEDs selected through ENLED[3:1] bits. In this mode, the DC light safety timeout feature is disabled.

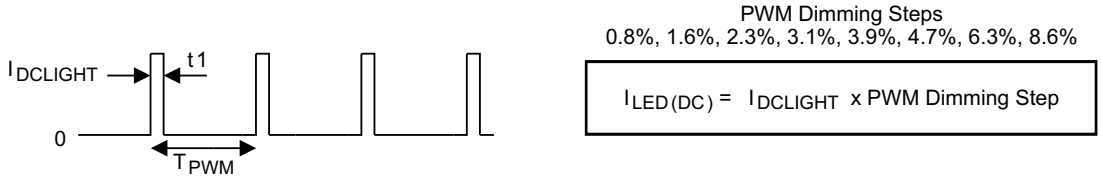

Figure 41. PWM Dimming Principle

8.3.14 Storage Capacitor, Precharge Voltage Calibration

High-power LEDs tend to exhibit a wide forward voltage distribution. The TPS6130xx device integrates a self-calibration procedure that can be used to determine the optimum super-capacitor precharge voltage based on the actual worst case LED forward voltage and ESR of the storage capacitor. This calibration procedure is meant to start-off at a minimum output voltage and can be initiated by setting the SELFCAL bit (preferably with MODE_CTRL[1:0] = 00, ENVM = 0, ENDCL = 0).

The calibration procedure monitors the sense voltage across the low-side current regulators (according to ENLED[3:1] bits setting) and registers the worst case LED (the LED featuring the largest forward voltage). The TPS6130xx device automatically sweeps through its output voltage range and performs a short duration flash strobe for each step (see *REGISTER2 (TPS61300, TPS61301)* or *REGISTER2 (TPS61305, TPS61305A, TPS61306)* for FC13[1:0] and FC2[2:0] bits settings).

In direct drive mode (HC_SEL = L), the energy is being directly transferred from the battery to the LEDs. In high-current mode (HC_SEL = H), the energy is supplied exclusively by the output reservoir capacitor and the inductive power stage is turned off for the flash strobe period of time.

The sequence is stopped as soon as the device detects that each of the low-side current regulators have enough headroom voltage (400-mV typical). The device returns the according output voltage in the register OV[3:0] and sets the SELFCAL bit. This bit is only being reset at the or restart of a calibration cycle. In other words, when SELFCAL is asserted the output voltage register (OV[3:0]) returns the result of the last calibration sequence.

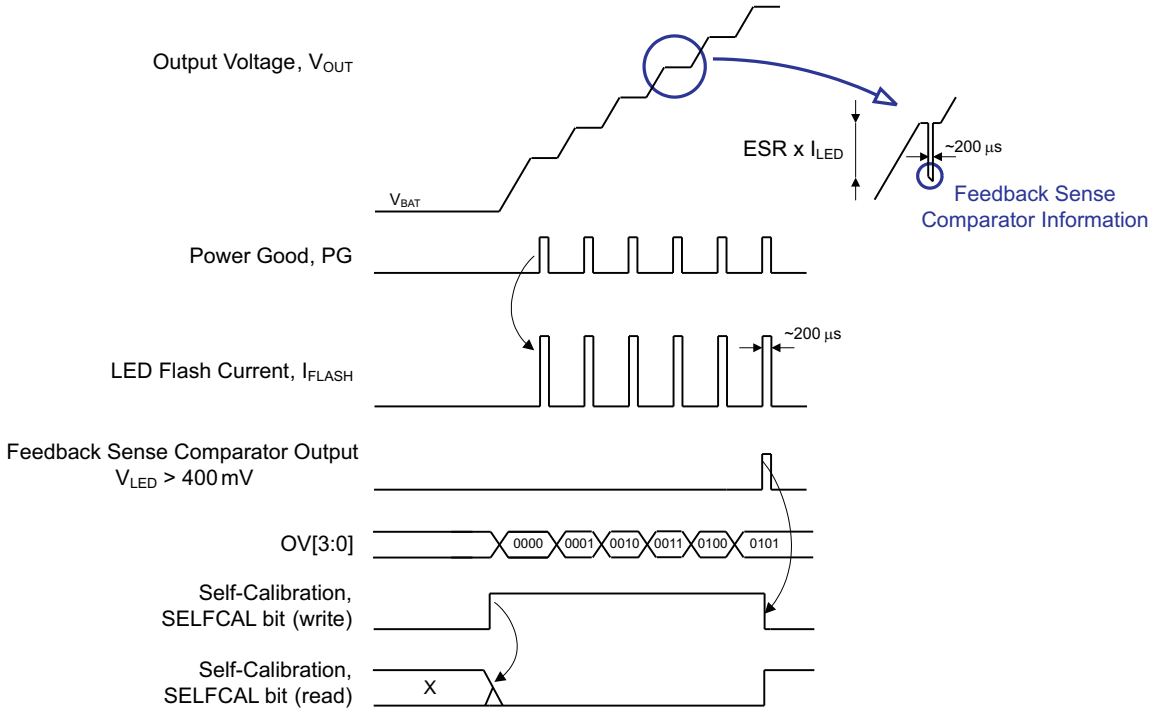

Figure 42. LED Forward Voltage Self-Calibration Principle

8.3.15 Storage Capacitor, Adaptive Precharge Voltage

In high-power LED camera flash applications, the storage capacitor is supposed to be charged to an optimum voltage level in order to:

- Maintain sufficient headroom voltage across the LED current regulators for the entire strobe time.
- Minimize the power dissipation in the device.

High-power LEDs tend to exhibit large dynamic forward voltage variation relating to own self-heating effects. In addition, the energy storage capacitor (Electrochemical Double-Layer Capacitor or Super-Capacitor) also shows a relatively large effective capacitance and ESR spread. The main factors contributing to these variations are:

- Flash strobe duration
- Temperature
- Ageing effects

In practice, it normally becomes very challenging to compensate for all these variations and a worst-case design would presumably be too pessimistic. As a consequence, designers would have to give up the benefits that come with the *Storage Capacitor, Precharge Voltage Calibration* approach.

The TPS6130xx device offers the possibility of controlling the storage capacitor precharge voltage in a closed-loop manner. The principle is to dynamically adjust the initial prevoltage to the minimum value, as required for the particular components characteristic and operating conditions.

The reference criteria used to evaluate proper operation is the headroom voltage across the LED current regulators. In case of a critical headroom voltage (V_{LED1-3}) at the end of a flash strobe (n cycle), the precharge voltage must be increased before the next capture sequence (n+1 cycle).

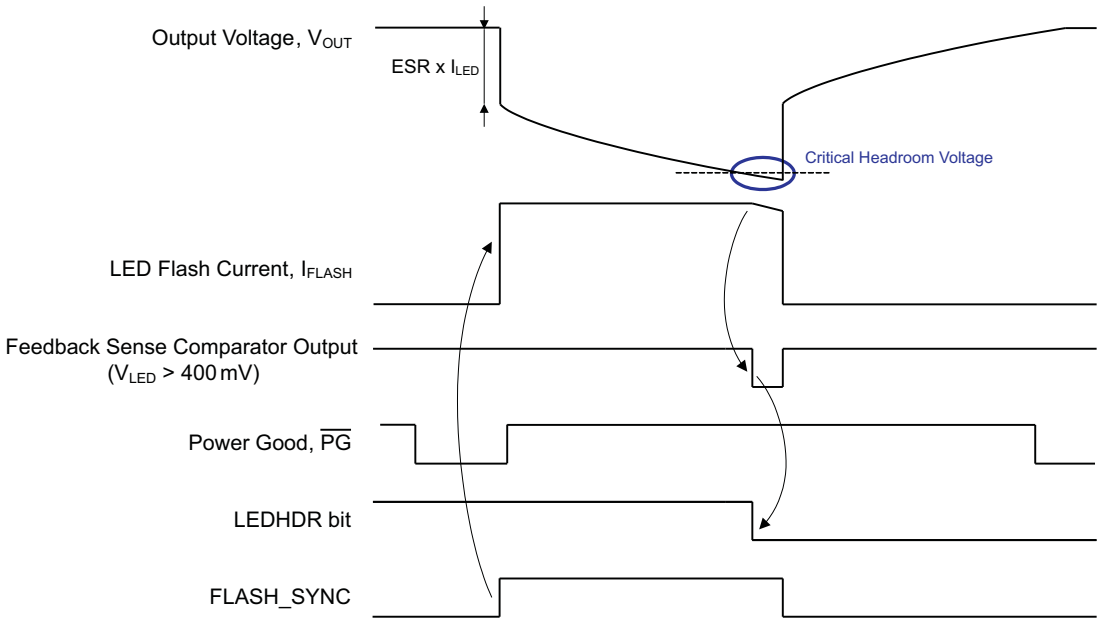

Figure 43. Storage Capacitor, Simple Adaptive Precharge Voltage

8.3.16 Serial Interface Description

I^2C is a 2-wire serial interface. The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open-drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives or transmits data on the bus under control of the master device.

The TPS6130xx device works as a *slave* and supports the following data transfer *modes*, as defined in the I^2C-Bus Specification: standard mode (100 kbps) and fast mode (400 kbps), and high-speed mode (3.4 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.1 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and it is referred to as HS-mode. The TPS6130xx device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is defined as 011 0011.

8.4 Device Functional Modes

8.4.1 Down-Mode in Voltage Regulation Mode

In general, a boost converter only regulates output voltages which are higher than the input voltage. The featured devices come with the ability to regulate 4.2 V at the output with an input voltage being has high as 5.5 V. To control these applications properly, a down-conversion mode is implemented.

In voltage regulation mode, if the input voltage reaches or exceeds the output voltage, the converter changes to the down-conversion mode. In this mode, the control circuit changes the behavior of the rectifying PMOS. It sets the voltage drop across the PMOS as high as needed to regulate the output voltage. This means the power losses in the converter increase. This must be considered for thermal consideration. The down-conversion mode is automatically turned off as soon as the input voltage falls about 200 mV below the output voltage.

For proper operation in down-conversion mode, the output voltage must not be programmed higher than ≈5.3 V. Take care not to violate the absolute maximum ratings at the SW pins.

Device Functional Modes (continued)

The TPS6130xx device uses a control architecture that allows to *recycle* excessive energy that might be stored in the output capacitor. By reversing the operation of the boost power stage, the converter is capable of transferring energy from its output back into the input source.

In high-current mode (HC_SEL = 1), this feature becomes useful to dynamically adjust the output voltage (V_{OUT}) depending on the operating conditions. For example, 4.95-V constant output voltage to support audio applications or variable storage capacitor precharge voltage. See *Storage Capacitor, Precharge Voltage Calibration* for more information.

Notice that this reverse operating mode can only perform within an output voltage range higher than the input supply. For example, if the storage capacitor is initially precharged to 4.95 V, the input voltage is around 4.1 V and the target output voltage is set to 3.825 V, the converter will only be able to lower the output node down to the input level.

8.4.2 LED High-Current Regulators, Unused Inputs

The TPS6130xx device uses LED forward voltage sensing circuitry on LED1-3 pins to optimize the power stage boost ratio for maximum efficiency. TI recommends not to leave any of the LED1, LED2, or LED3 pins unused if operations has been selected through ENLED[3:1] bits, due to the nature of the sensing circuitry. Leaving LED1-3 pins unconnected, whilst the respective ENLEDx bits have been set, will force the control loop into high gain and eventually trip the output overvoltage protection.

The LED1-3 inputs may be connected together to drive one or two LEDs at higher currents. Connecting the current sink inputs in parallel does not affect the internal operation of the TPS6130xx. For best operation, TI recommends disabling the LED inputs that are not used (see *REGISTER5* for ENLED[3:1] bits description).

To achieve smooth LED current waveforms, the TPS61300 device actively controls the LED current ramp-up or down sequence.

Table 7. LED Current Ramp-Up or Down Control vs Operating Mode

	DIRECT DRIVE MODE (HC_SEL = 0)	HIGH-CURRENT MODE (HC_SEL = 1)
LED CURRENT RAMP-UP	I_{STEP} = 25 mA	I_{STEP} = 56.25 mA
	t_{RISE} = 12 µs	t_{RISE} = 0.5 µs
	Slew-rate ≠ 2.08 mA/µs	Slew-rate ≠ 112.5 mA/µs
LED CURRENT RAMP-DOWN	I_{STEP} = 25 mA	I_{STEP} = 56.25 mA
	t_{FALL} = 0.5 µs	t_{FALL} = 0.5 µs
	Slew-rate ≠ 50 mA/µs	Slew-rate ≠ 112.5 mA/µs

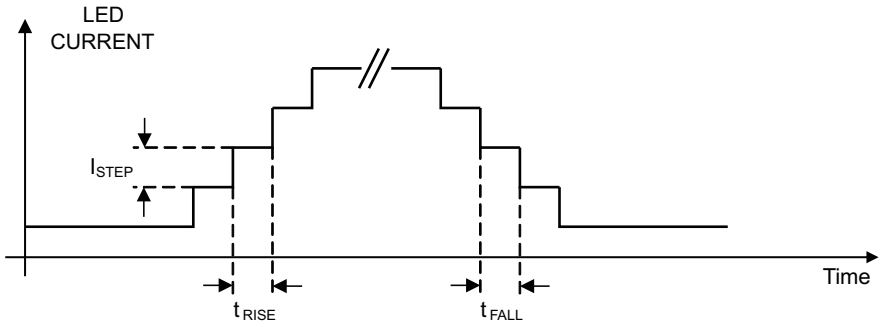

Figure 44. LED Current Slew-Rate Control

In high-current mode (HC_SEL = 1), the LED current settings are defined as a fixed ratio (×2.25) versus the direct drive mode values (HC_SEL = L).

8.4.3 Power-Save Mode Operation, Efficiency

The TPS6130xx device integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage.

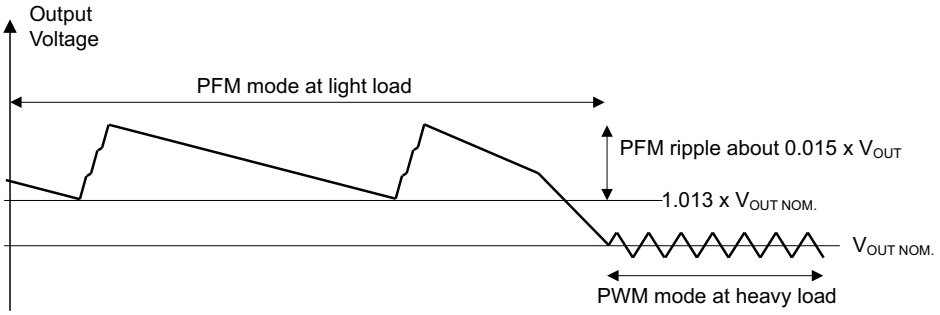

Figure 45. Operation in PFM Mode and Transfer to PWM Mode

The power save mode can be enabled and disabled through the ENPSM bit. In down-conversion mode, power save mode is always active and the device cannot be forced into fixed frequency operation at light loads.

The LED sense voltage has a direct effect on the converter's efficiency. Because the voltage across the low-side current regulator does not contribute to the output power (LED brightness), the lower the sense voltage the higher the efficiency will be.

In direct drive mode (HC_SEL = L), the energy is being directly transferred from the battery to the LEDs. The integrated current control loop automatically selects the minimum boosting ratio to maintain regulation based on the LED forward voltage and current requirements. The low-side current regulators will be dropping the voltage difference between the input voltage and the LEDs forward voltage ($V_{F(LED)} < V_{IN}$). When running in boost mode ($V_{F(LED)} > V_{IN}$), the voltage present at the LED1–3 pins of the low-side current regulators will be typically 400 mV leading to high power conversion efficiency. Depending on the input voltage and the LEDs forward voltage characteristic the converter will show efficiency in the range of about 75% to 90%.

In high-current mode (HC_SEL = H), the device is only supplying a limited amount of energy directly from the battery (DC light, contribution to flash current or voltage regulation mode). During a flash strobe, the bulk of the energy supplied to the LEDs is provided by the reservoir capacitor. The low-side current regulators will be typically operating with 400-mV headroom voltage. This means the power losses in the device increase and special care must be taken for thermal considerations.

8.4.4 Mode of Operation: DC Light and Flashlight

Operation is understood best by referring to the timer block diagram. Depending on the settings of MODE_CTRL[1:0] bits the device can enter 4 different operating modes. Table 8 details the converter's operation for ENVM = 0.

Table 8. Converter Operation for ENVM = 0

MODE_CTRL[1:0]	DESCRIPTION
00	The device is in shutdown mode.
01	The device is regulating the LED current to the DC light current level (DCLC bits) regardless of the FLASH_SYNC input and START_FLASH/TIMER (SFT) bit. To avoid device shutdown by DC light safety timeout, MODE_CTRL[1:0] needs to be refreshed within less than 11.2 s.
10	The flashlight pulse can be either trigger by a hardware signal (FLASH_SYNC) or by a software bit (SFT). LED strobe pulse follows FLASH_SYNC.
11	The device is regulating a constant output voltage according to OV[3:0] bits settings. The low-side LED1–3 current sinks are disabled and the LEDs are disconnected from the output. In this operating mode, the safety timer is disabled.

8.4.5 Flash Strobe is Level Sensitive (STT = 0): LED Strobe Follows FLASH_SYNC Input

FLASH_SYNC and (SFT) = 0: LED operation is set to the DC light current level. To avoid device shutdown by DC light safety timeout, MODE_CTRL[1:0] must be refreshed within less than 11.2 s.

FLASH_SYNC or (SFT) = 1: The LED is driven at the flashlight current level and the safety timer is running. The maximum duration of the flashlight pulse is defined in the STIM[2:0] register.

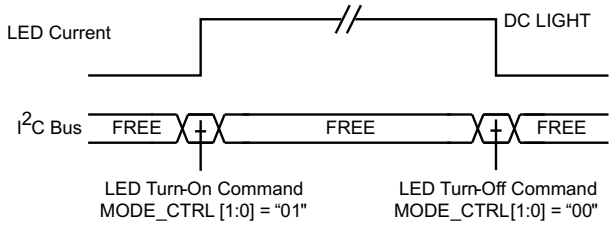

Figure 46. DC Light Operation

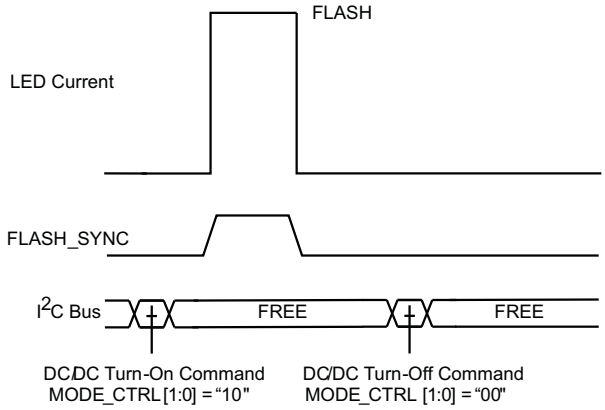

Figure 47. Synchronized Flashlight Strobe

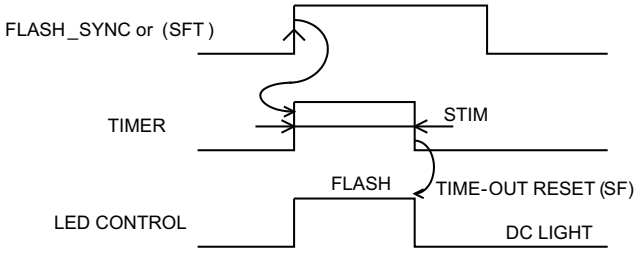

Figure 48. Level Sensitive Safety Timer (Timeout)

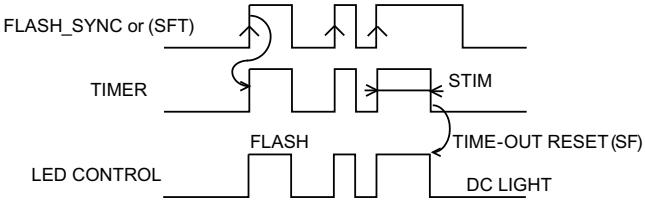

Figure 49. Level Sensitive Safety Timer (Normal Operation + Timeout)

The safety timer is started by:

- a rising edge of FLASH_SYNC signal.
- a rising edge of START_FLASH/TIMER (SFT) bit.

The safety timer is stopped by:

- a low level of FLASH_SYNC signal or START_FLASH/TIMER (SFT) bit.
- a timeout signal (TO).

START-FLASH/TIMER (SFT) bit is being reset by the timeout (TO) signal.

8.4.6 Flash Strobe Is Leading Edge Sensitive (STT = 1): One-Shot LED Strobe

When FLASH_SYNC and START_FLASH/TIMER (SFT) are both low the LED operation is set to the DC Light current level. To avoid device shutdown by DC light safety timeout, MODE_CTRL[1:0] needs to be refreshed within less than 11.2 s.

The duration of the flashlight pulse is defined in the STIM register. The flashlight strobe is started by:

- a rising edge of START_FLASH/TIMER (SFT) bit.
- a rising edge of FLASH_SYNC signal.

Once running, the timer ignores all kind of triggering signal and only stops after a timeout (TO). START-FLASH/TIMER (SFT) bit is being reset by the timeout (TO) signal.

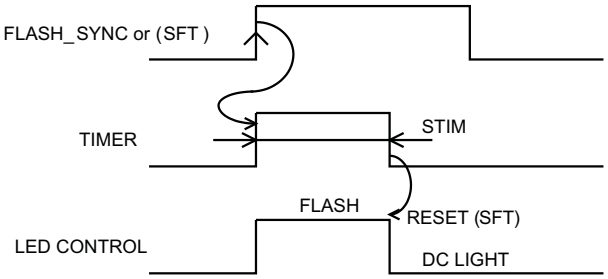

Figure 50. Edge Sensitive Timer (Single Trigger Event)

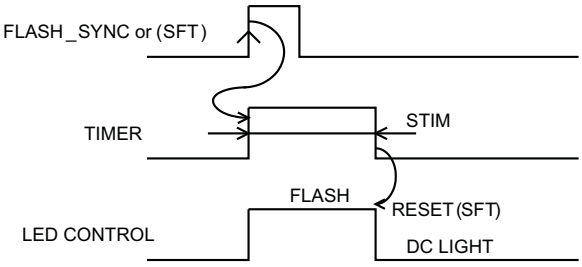

Figure 51. Edge Sensitive Timer (Single Trigger Event)

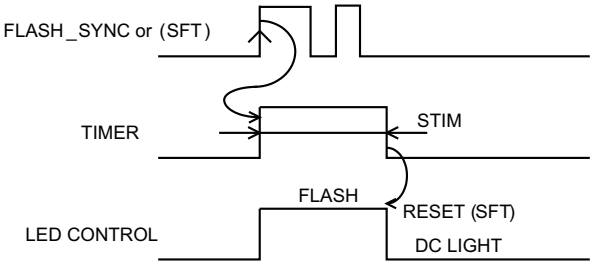

Figure 52. Edge Sensitive Timer (Multiple Trigger Events)

8.4.7 Current Limit Operation

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off time through sensing of the voltage drop across the synchronous rectifier. The detection threshold is user selectable through the ILIM bit. The ILIM bit can only be set before the device enters operation (that is, initial shutdown state).

Figure 53 illustrates the inductor and rectifier current waveforms during current limit operation. The output current, I_{OUT}, is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off time is lengthened to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism).

Both the output voltage and the switching frequency are reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit operation, can be defined with Equation 1.

$$I_{OUT(CL)} = (1 - D) \times \left(I_{VALLEY} + \frac{1}{2} \Delta I_L\right) \text{ with } \Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f} \text{ and } D \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

The TPS6130xx device also provides a negative current limit (≈300 mA) to prevent an excessive reverse inductor current when the power stage sinks current from the output (that is, storage capacitor) in the forced continuous conduction mode.

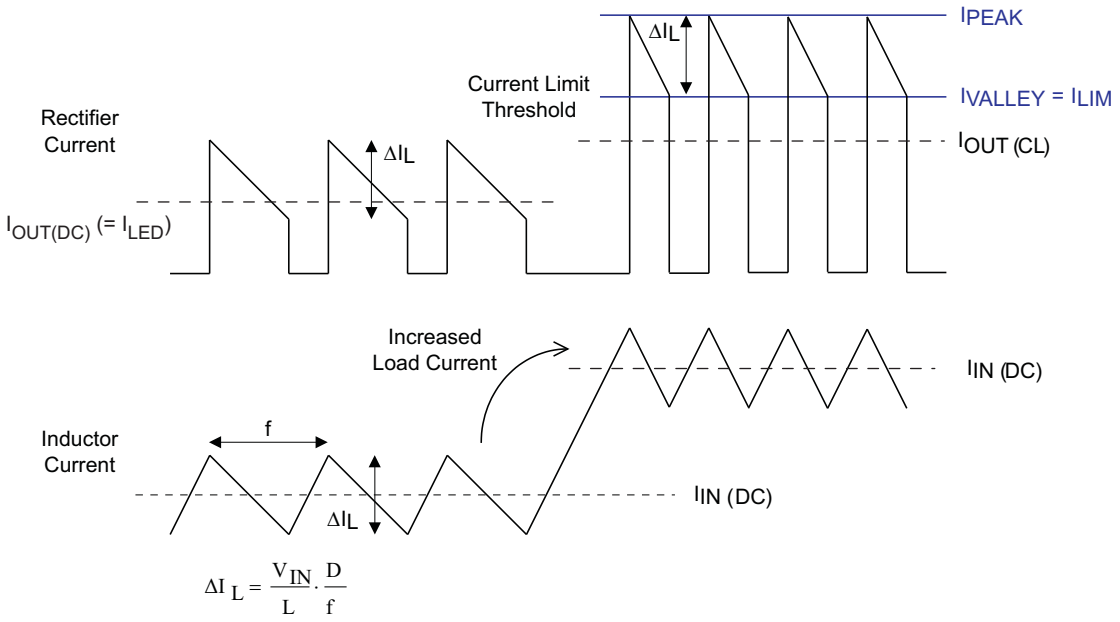

Figure 53. Inductor and Rectifier Currents in Current Limit Operation

To minimize the requirements on the energy storage capacitor present at the output of the driver (HC_SEL = 1), the TPS6130xx device can contribute to a larger extent in supporting directly the high-current LED flash strobe. In fact, the device can dynamically adjust its current limit setting according to the Tx-MASK input.

Table 9. Inductor Current Limit Operation vs HC_SEL and Tx-MASK Inputs

CURRENT LIMIT SETTING	ILIM BIT	HC_SEL INPUT	Tx-MASK INPUT
1250 mA	Low	Low	Low
1750 mA	High	Low	Low
1250 mA	Low	High	Low
1750 mA	High	High	Low
1250 mA	Low	Low	High
1750 mA	High	Low	High
250 mA	Low	High	High
500 mA	High	High	High

8.4.8 Hardware Voltage Mode Selection

The TPS6130xx device integrates a logic input (ENVM) or a software control bit (ENVM bit) that can be used to force the converter to run in voltage mode regulation. Pulling the ENVM pin high forces the device into voltage regulation mode (V_{OUT} is preset to a fixed value, 4.95 V). This additional operating mode can be useful to supply other high power consuming devices in the system, such as hands-free audio power amplifiers, or any other component requiring a regulated supply voltage higher or lower than the battery voltage.

Table 10 gives an overview of the different mode of operation.

Table 10. Operating Mode Description

INTERNAL REGISTER SETTINGS MODE_CTRL[1:0]	ENVM BIT	OPERATING MODES
00	0	The converter is in shutdown mode and the load is disconnected from the battery.
01	0	**LEDs are turned-on for DC light operation (for example, movie-light).** The converter is operating in the current regulation mode (CM). The output voltage is controlled by the forward voltage characteristic of the LED. The energy is being directly transferred from the battery to the output.
		The integrated current control loop automatically selects the minimum boosting ratio to maintain regulation based on the LED forward voltage and current requirements. When running in linear mode ($V_{F(LED)} < V_{IN}$), the DC-DC power stage featuring valley-current limit is not active permitting relatively large currents to circulate from the input to the output of the device.
10	0	The converter is operating in the current regulation mode (CM). The output voltage is controlled by the forward voltage characteristic of the LED. LEDs are ready for flashlight operation and DC light operation is supported directly from the battery.
		The integrated current control loop automatically selects the minimum boosting ratio to maintain regulation based on the LED forward voltage and current requirements. When running in linear mode ($V_{F(LED)} < V_{IN}$), the DC-DC power stage featuring valley-current limit is not active permitting relatively large currents to circulate from the input to the output of the device.
		In high-current mode (HC_SEL = H), the energy is supplied by the output reservoir capacitor and the inductive power stage is turned-off for the flash strobe period of time.
11	0	LEDs are turned-off and the converter is operating in the voltage regulation mode (VM). The output voltage is set through the register OV[3:0].
00	1	LEDs are turned-off and the converter is operating in the voltage regulation mode (VM). The output voltage is set through the register OV[3:0].
01	1	**The converter is operating in the voltage regulation mode (VM) and it's output voltage is set through the register OV[3:0]. The LEDs are turned-on for DC light operation and the energy is being directly transferred from the battery to the output. The LED currents are regulated by the means of the low-side current sinks.**
10	1	The converter is operating in the voltage regulation mode (VM) and it's output voltage is set through the register OV[3:0]. The LED currents are regulated by the means of the low-side current sinks. The LEDs are ready for flashlight operation.
		In direct drive mode (HC_SEL = L), the energy is being directly transferred from the battery to the output.
		In high-current mode (HC_SEL = H), the energy is largely supplied by the output reservoir capacitor. The inductive power stage is turned-on to support DC light operation and to contribute the flash strobe itself.
11	1	LEDs are turned-off and the converter is operating in the voltage regulation mode (VM). The output voltage is set through the register OV[3:0].

8.4.9 Shutdown

MODE_CTRL[1:0] bits low force the device into shutdown. The shutdown state can only be entered when the voltage regulation and DC light modes are both turned-off (ENVM = 0 and ENDCL = 0).

In direct drive mode (HC_SEL = L), the regulator stops switching, the high-side PMOS disconnects the load from the input and the LEDx pins are high impedance thus eliminating any DC conduction path. The TPS6130xx device actively discharges the output capacitor when it turns off.

The integrated discharge resistor has a typical resistance of 2 kΩ equally split-off between VOUT to BAL and BAL to GND outputs. The required time to discharge the output capacitor at V_{OUT} depends on load current and the effective output capacitance. The active balancing circuit is disabled and the device consumes only a shutdown current of 1 µA (typical).

In high-current mode (HC_SEL = H), the device maintains its output biased at the input voltage level. In this mode, the synchronous rectifier is current-limited, allowing external load, such as audio amplifiers, to be powered with a restricted supply. The active balancing circuit is enabled and the device consumes only a standby current of 5 µA (typical).

8.4.10 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 160°C typical, the device goes into thermal shutdown. In this mode, the power stage and the low-side current regulators are turned off, the HOTDIE[1:0] bits are set and can only be reset by a readout.

In the voltage mode operation (MODE_CTRL[1:0] = 11 or ENVM = 1), the device continues its operation when the junction temperature falls below 140°C (typical) again. In the current regulation mode (that is, DC light or flashlight modes) the device operation is suspended.

8.4.11 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 54. All I^2C-compatible devices will recognize a start condition.

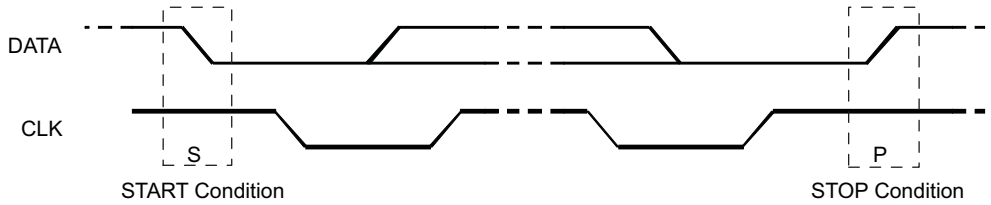

Figure 54. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 55). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 56) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

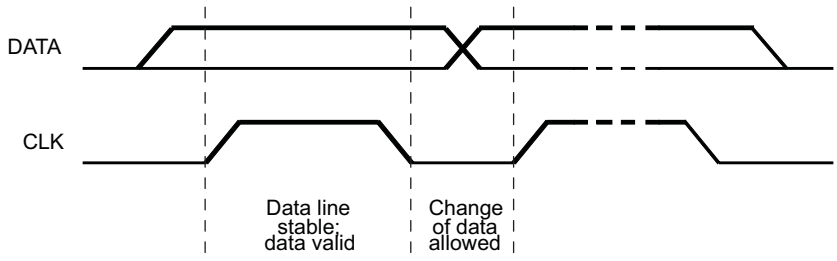

Figure 55. Bit Transfer On the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 54). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

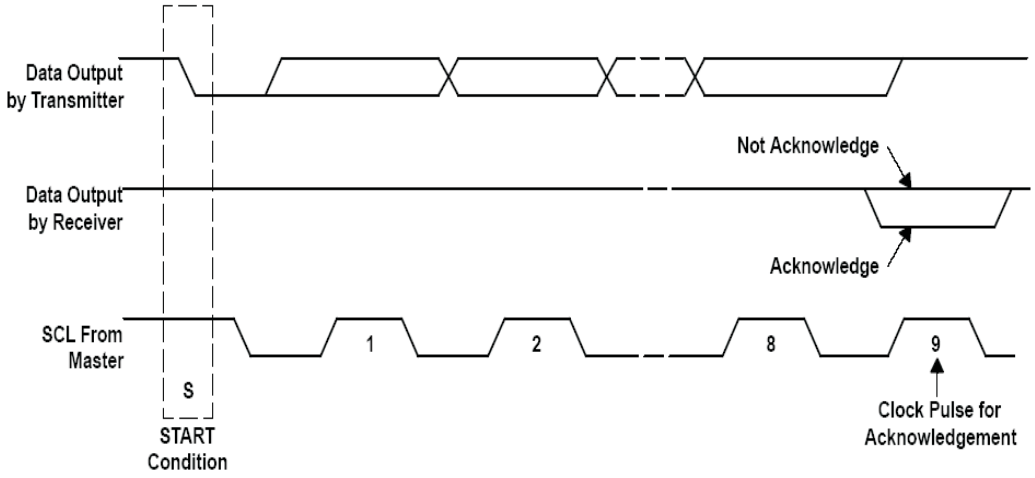

Figure 56. Acknowledge On the I^2C Bus

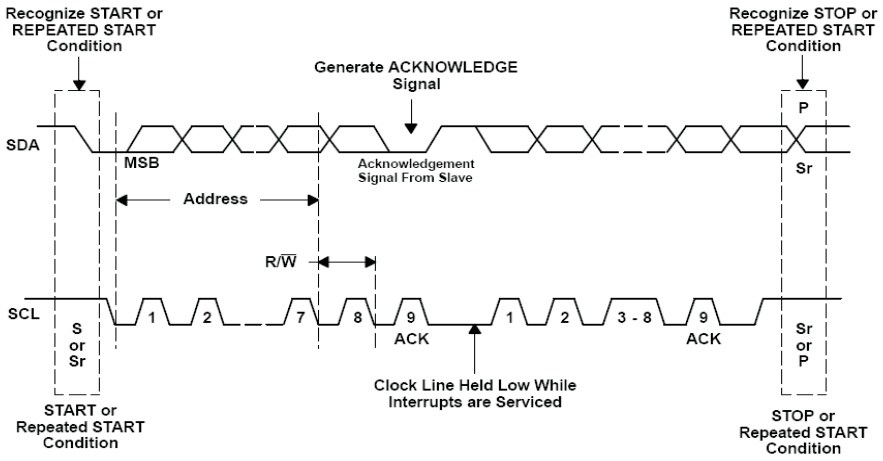

Figure 57. Bus Protocol

8.4.12 HS-Mode Protocol

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions must be used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

8.4.13 TPS6130xx I²C Update Sequence

The TPS6130xx requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS6130xx device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the TPS6130xx. TPS6130xx performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

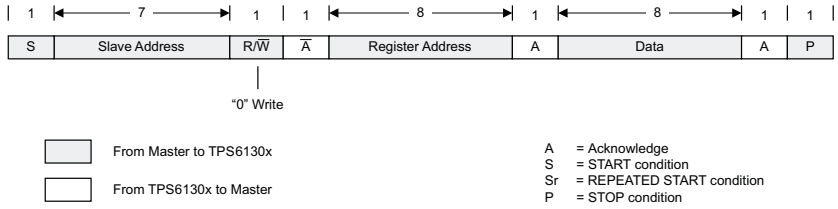

Figure 58. Write Data Transfer Format in F/S-Mode

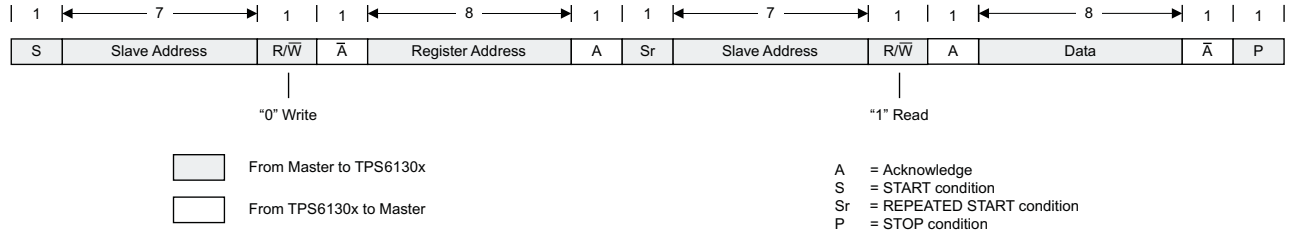

Figure 59. Read Data Transfer Format in F/S-Mode

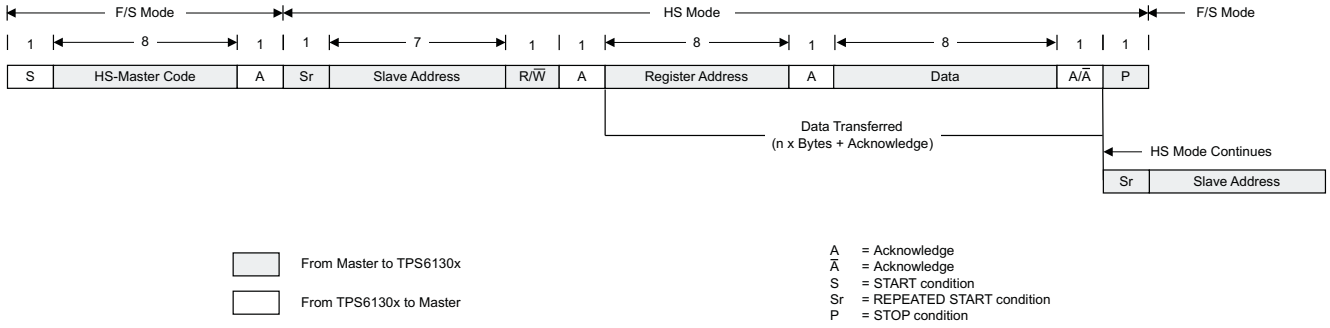

Figure 60. Data Transfer Format in HS-Mode

8.5 Register Maps

8.5.1 Slave Address Byte

Figure 61. Slave Address Byte Description

MSB							LSB
X	X	X	X	X	X	A1	A0

The slave address byte is the first byte received following the START condition from the master device.

8.5.2 Register Address Byte

Figure 62. Register Address Byte Description

MSB							LSB
0	0	0	0	00	D2	D1	D0

Following the successful acknowledgement of the slave address, the bus master will send a byte to the TPS6130xx, which will contain the address of the register to be accessed.

8.5.3 REGISTER1 (TPS61300, TPS61301)

Memory location: 0x01

Figure 63. REGISTER1 Fields

7	6	5	4	3	2	1	0
ENVM	MODE_CTRL[1:0]		DCLC13[1:0]		DCLC2[2:0]		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. (For example, CONTROL_REVISION Register) Field Descriptions

Bit	Field	Type	Reset	Description
7	ENVM	R/W	0	**Enable Voltage Mode bit.** 0: Normal operation. 1: Forces the device into a constant voltage source. In read mode, the ENVM bit is automatically updated to reflect the logic state of the ENVM input pin.
6–5	MODE_CTRL[1:0]	R/W	00	**Mode Control bits.** 00: Device in shutdown mode. 01: Device operates in DC light mode. 10: Device operates in DC light and flash mode. 11: Device operates as constant voltage source. To avoid device shutdown by DC light safety timeout, MODE_CTRL[1:0] bits need to be refreshed within less than 11.2 s. Writing to REGISTER1[6:5] automatically updates REGISTER2[6:5].
4–3	DCLC13[1:0]	R/W	01	**DC Light Current Control bits (LED1/3).** 00: 0 mA. LEDs are off, V_{OUT} set according to OV[3:0].(1)(2) 01: 50 mA 10: 75 mA 11: 100 mA
2–0	DCLC2[2:0]	R/W	001	**DC Light Current Control bits (LED2).** 000: 0 mA. LEDs are off, V_{OUT} set according to OV[3:0].(1)(2) 001: 50 mA 010: 75 mA 011: 100 mA 100: 125 mA 101: 150 mA 110: 200 mA, 350 mA current level can be activated simultaneously with Tx-MASK = 1. 111: 250 mA, 500 mA current level can be activated simultaneously with Tx-MASK = 1.

(1) When DCLC2[2:0] and DCLC13[1:0] are both reset, the device operates in voltage regulation mode. The output voltage is set according to OV[3:0].
(2) To ensure a proper transition into voltage mode operation, TI recommends disabling the LEDs (ENLED[2:0] bits are reset) before clearing DCLC2[2:0] and DCLC13[1:0] bits.

8.5.4 REGISTER1 (TPS61305, TPS61305A, TPS61306)

Memory location: 0x01

Figure 64. REGISTER1 Fields

7	6	5	4	3	2	1	0
ENVM	MODE_CTRL[1:0]		DCLC13[1:0]		DCLC2[2:0]		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. (For example, CONTROL_REVISION Register) Field Descriptions

Bit	Field	Type	Reset	Description
7	ENVM	R/W	0	**Enable Voltage Mode bit.** 0: Normal operation. 1: Forces the device into a constant voltage source. In read mode, the ENVM bit is automatically updated to reflect the logic state of the ENVM input pin.
6–5	MODE_CTRL[1:0]	R/W	00	**Mode Control bits.** 00: Device in shutdown mode. 01: Device operates in DC light mode. 10: Device operates in DC light and flash mode. 11: Device operates as constant voltage source. To avoid device shutdown by DC light safety timeout, MODE_CTRL[1:0] bits need to be refreshed within less than 11.2 s. Writing to REGISTER1[6:5] automatically updates REGISTER2[6:5].
4–3	DCLC13[1:0]	R/W	01	**DC Light Current Control bits (LED1/3).** 00: 0 mA. LEDs are off, V_{OUT} set according to OV[3:0].(1)(2) 01: 55 mA 10: 85 mA 11: 110 mA
2–0	DCLC2[2:0]	R/W	001	**DC Light Current Control bits (LED2).** 000: 0 mA. LEDs are off, V_{OUT} set according to OV[3:0].(1)(2) 001: 55 mA 010: 85 mA 011: 110 mA 100: 140 mA 101: 165 mA 110: 220 mA, 350 mA current level can be activated simultaneously with Tx-MASK = 1. 111: 275 mA, 500 mA current level can be activated simultaneously with Tx-MASK = 1.

(1) When DCLC2[2:0] and DCLC13[1:0] are both reset, the device operates in voltage regulation mode. The output voltage is set according to OV[3:0].
(2) To ensure a proper transition into voltage mode operation, TI recommends disabling the LEDs (ENLED[2:0] bits are reset) before clearing DCLC2[2:0] and DCLC13[1:0] bits.

8.5.5 REGISTER2 (TPS61300, TPS61301)

Memory location: 0x02

Figure 65. REGISTER2 Fields

7	6	5	4	3	2	1	0
ENVM	MODE_CTRL[1:0]		FC13[1:0]		FC2[2:0]		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. REGISTER2 Field Descriptions

Bit	Field	Type	Reset	Description
7	ENVM	R/W	0	Enable Voltage Mode bit. 0: Normal operation. 1: Forces the device into a constant voltage source. In read mode, the ENVM bit is automatically updated to reflect the logic state of the ENVM input pin.
6–5	MODE_CTRL[1:0]	R/W	00	**Mode Control bits.** 00: Device in shutdown mode. 01: Device operates in DC light mode. 10: Device operates in DC light and flash mode. 11: Device operates as constant voltage source. To avoid device shutdown by DC light safety timeout, MODE_CTRL[1:0] bits need to be refreshed within less than 11.2 s. Writing to REGISTER2[6:5] automatically updates REGISTER1[6:5].
4–3	FC13[1:0]	R/W	00	**Flash Current Control bits (LED1/3).** HC_SEL = 0 / HC_SEL = 1 000: 275 mA / 000: 650 mA 001: 300 mA / 001: 700 mA 010: 350 mA / 010: 825 mA 011: 450 mA / 011: 1050 mA 100: 550 mA / 100: 1300 mA 101: 600 mA / 101: 1400 mA 110: 700 mA / 110: 1600 mA 111: 800 mA / 111: 1850 mA
2–0	FC2[2:0]	R/W	011	**Flash Current Control bits (LED2).** HC_SEL = 0 / HC_SEL = 1 00: 250 mA / 00: 600 mA 01: 300 mA / 01: 700 mA 10: 350 mA / 10: 800 mA 11: 400 mA / 11: 925 mA

8.5.6 REGISTER2 (TPS61305, TPS61305A, TPS61306)

Memory location: 0x02

Figure 66. REGISTER2 Fields

7	6	5	4	3	2	1	0
ENVM	MODE_CTRL[1:0]		FC13[1:0]		FC2[2:0]		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. REGISTER2 Field Descriptions

Bit	Field	Type	Reset	Description
7	ENVM	R/W	0	Enable Voltage Mode bit. 0: Normal operation. 1: Forces the device into a constant voltage source. In read mode, the ENVM bit is automatically updated to reflect the logic state of the ENVM input pin.
6–5	MODE_CTRL[1:0]	R/W	00	**Mode Control bits.** 00: Device in shutdown mode. 01: Device operates in DC light mode. 10: Device operates in DC light and flash mode. 11: Device operates as constant voltage source. To avoid device shutdown by DC light safety timeout, MODE_CTRL[1:0] bits need to be refreshed within less than 11.2 s. Writing to REGISTER2[6:5] automatically updates REGISTER1[6:5].
4–3	FC13[1:0]	R/W	00	**Flash Current Control bits (LED1/3).** HC_SEL = 0 / HC_SEL = 1 00: 275 mA / 00: 665 mA 01: 335 mA / 01: 775 mA 10: 385 mA / 10: 890 mA 11: 445 mA / 11: 1025 mA
2–0	FC2[2:0]	R/W	011	**Flash Current Control bits (LED2).** HC_SEL = 0 / HC_SEL = 1 000: 305 mA / 000: 720 mA 001: 335 mA / 001: 775 mA 010: 385 mA / 010: 915 mA 011: 500 mA / 011: 1165 mA 100: 610 mA / 100: 1450 mA 101: 665 mA / 101: 1550 mA 110: 775 mA / 110: 1775 mA 111: 885 mA / 111: 2050 mA

8.5.7 REGISTER3

Memory location: 0x03

Figure 67. REGISTER3 Fields

7	6	5	4	3	2	1	0
STIM[2:0]			HPLF	SELSTIM (W) TO (R)	STT	SFT	Tx-MASK
R/W-1	R/W-1	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. REGISTER3 Field Descriptions

Bit	Field	Type	Reset	Description
7–5	STIM[2:0]	R/W	110	**Safety Timer bits** STIM[2:0]: Range 0, Range 1 000: 68.2 ms, 5.3 ms 001: 102.2 ms, 10.7 ms 010: 136.3 ms, 16.0 ms 011: 170.4 ms, 21.3 ms 100: 204.5 ms, 26.6 ms 101: 340.8 ms, 32.0 ms 110: 579.3 ms, 37.3 ms 111: 852 ms, 207.7 ms
4	HPFL	R	0	**High-Power LED Failure flag.** 0: Proper LED operation. 1: LED failed (open or shorted). High-power LED failure flag is reset after readout
3	SELSTIM	R	0	**Safety Timer Selection Range (Write Only).** 0: Safety timer range 0. 1: Safety timer range 1.
	TO	W		**Time-Out Flag (Read Only).** 0: No time-out event occurred. 1: Time-out event occurred. Time-out flag is reset at re-start of the safety timer.
2	STT	R/W	0	**Safety Timer Trigger bit.** 0: LED safety timer is level sensitive. 1: LED safety timer is rising edge sensitive. This bit is only valid for MODE_CTRL[1:0] = 10.
1	SFT	R/W	0	**Start/Flash Timer bit.** In write mode, this bit initiates a flash strobe sequence. 0: No change in the high-power LED current. 1: High-power LED current ramps to the flash current level. In read mode, this bit indicates the high-power LED status. 0: High-power LEDs are idle. 1: Ongoing high-power LED flash strobe.
0	Tx-MASK	R/W	1	**Flash Blanking Control bit.** In write mode, this bit enables and disables the flash blanking and LED current reduction function. 0: Flash blanking disabled. 1: LED current is reduced to DC light level when Tx-MASK input is high. In read mode, this flag indicates whether or not the flashlight masking input has been activated. Tx-MASK flag is reset after readout of the flag. 0: No flash blanking event occurred. 1: Tx-MASK input triggered.

8.5.8 REGISTER4

Memory location: 0x04

Figure 68. REGISTER4 Fields

7	6	5	4	3	2	1	0
PG	HOTDIE[1:0]		ILIM	INC[3:0]			
R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. REGISTER4 Field Descriptions

Bit	Field	Type	Reset	Description
7	PG	R/W	0	**Power Good bit.** In write mode, this bit selects the functionality of the GPIO/PG output. 0: PG signal is routed to the GPIO port. 1: GPIO PORT VALUE bit is routed to the GPIO port. In read mode, this bit indicates the output voltage conditions. 0: The converter is not operating within the voltage regulation limits. 1: The output voltage is within its nominal value.
6–5	HOTDIE[1:0]	R	00	**Instantaneous Die Temperature bits.** 00: T_J < 55°C 01:55°C < T_J < 70°C 10: T_J > 70°C 11: Thermal shutdown tripped. Indicator flag is reset after readout.
4	ILIM	R/W	0	**Inductor Valley Current Limit bit.** (1) Current Limit setting, ILIM-bit setting, HC_SEL input level, Tx-MASK input level 1250 mA, Low, Low, Low 1750 mA, High, Low, Low 1250 mA, Low, High, Low 1750 mA, High, High, Low 1250 mA, Low, Low, High 1750 mA, High, Low, High 250 mA, Low, High, High 500 mA, High, High, High
3–0	INDC[3:0]	R/W	0000	**Indicator Light Control bits.** INDC[3:0]: Privacy indicator INDLED channel 0000: Privacy indicator turned-off 0001: INDLED current = 2.6 mA 0010: INDLED current = 5.2 mA 0011: INDLED current = 7.9 mA 0100: Privacy indicator turned-off 0101: INDLED current = 2.6 mA (2) 0110: INDLED current = 5.2 mA (2) 0111: INDLED current = 7.9 mA (2) INDC[3:0]: Privacy indicator LED1–3 channels (3) 1000: 0.8% PWM dimming ratio 1001: 1.6% PWM dimming ratio 1010: 2.3% PWM dimming ratio 1011: 3.1% PWM dimming ratio 1100: 3.9% PWM dimming ratio 1101: 4.7% PWM dimming ratio 1110: 6.3% PWM dimming ratio 1111: 8.6% PWM dimming ratio

(1) The ILIM bit can only be set before the device enters operation (initial shutdown state).
(2) The output node is internally pulled to ground. This mode is only possible for HC_SEL = L.
(3) This mode of operation can only be activated for MODE_CTRL[1:0] = 01 and ENDCL = 0.

8.5.9 REGISTER5

Memory location: 0x05

Figure 69. REGISTER5 Fields

7	6	5	4	3	2	1	0
SELFCAL	ENPSM	STENDCL (R) DIR (W)	GPIO	GPIOTYPE	ENLED3	ENLED2	ENLED1
R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. REGISTER5 Field Descriptions

Bit	Field	Type	Reset	Description
7	SELFCAL	R/W	0	**High-Current LED Forward Voltage Self-Calibration Start bit.** In write mode, this bit enables and disables the output voltage vs LED forward voltage and current self-calibration procedure. 0: Self-calibration disabled. 1: Self-calibration enabled. In read mode, this bit returns the status of the self-calibration procedure. 0: Self-calibration ongoing 1: Self-calibration done Notice that this bit is only being reset at the (re-)start of a calibration cycle.
6	ENPSM	R/W	1	**Enable and Disable Power-Save Mode bit.** 0: Power-save mode disabled. 1: Power-save mode enabled.
5	STENDCL	R	1	**ENDCL Input Status bit (Read Only).** This bit indicates the logic state on the ENDCL state. This bit is only active in TPS61300.
	DIR	W		**GPIO Direction bit.** 0: GPIO configured as input. 1: GPIO configured as output.
4	GPIO	R/W	0	**GPIO Port Value.** This bit contains the GPIO port value.
3	GPIOTYPE	R/W	1	**GPIO Port Type.** 0: GPIO is configured as push-pull output. 1: GPIO is configured as open-drain output.
2	ENLED3	R/W	0	**Enable and Disable High-Current LED3 bit.** 0: LED3 input is disabled. 1: LED3 input is enabled.
1	ENLED2	R/W	1	**Enable and Disable High-Current LED2 bit.** 0: LED2 input is disabled. 1: LED2 input is enabled.
0	ENLED1	R/W	0	**Enable and Disable High-Current LED1 bit.** 0: LED1 input is disabled. 1: LED1 input is enabled.

8.5.10 REGISTER6 (TPS61300, TPS61301)

Memory location: 0x06

Figure 70. REGISTER6 Fields

7	6	5	4	3	2	1	0
NOT USED			LEDHDR	OV[3:0]			
R/W-0	R/W-0	R/W-0	R-0	R/W-1	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. REGISTER6 Field Descriptions

Bit	Field	Type	Reset	Description
4	LEDHDR	R	0	**LED High-Current Regulator Headroom Voltage Monitoring bit.** This bit returns the headroom voltage status of the LED high-current regulators. This value is being updated at the end of a flash strobe, before the LED current ramp-down phase. 0: Low headroom voltage. 1: Sufficient headroom voltage.
3–0	OV[3:0]	R/W	1001	**Output Voltage Selection bits.** In read mode, these bits return the result of the high-current LED forward voltage self-calibration procedure. In write mode, these bits are used to set the target output voltage (see *Down-Mode in Voltage Regulation Mode*). In applications requiring dynamic voltage control, care must be take to set the new target code after voltage mode operation has been enabled (MODE_CTRL[1:0] = 11 or ENVM bit = 1). OV[3:0]: Target Output Voltage 0000: 3.825 V 0001: 3.950 V 0010: 4.075 V 0011: 4.200 V 0100: 4.325 V 0101: 4.450 V 0110: 4.575 V 0111: 4.700 V 1000: 4.825 V 1001: 4.950 V 1010: 5.075 V 1011: 5.200 V 1100: 5.325 V 1101: 5.450 V 1110: 5.575 V 1111: 5.700 V

8.5.11 REGISTER6 (TPS61305, TPS61305A)

Memory location: 0x06

Figure 71. REGISTER6 Fields

7	6	5	4	3	2	1	0
ENTS	LEDHOT	LEDWARN	LEDHDR	OV[3:0]			
R/W-0	R/W-0	R-0	R-0	R/W-1	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. REGISTER6 Field Descriptions

Bit	Field	Type	Reset	Description
7	ENTS	R/W	0	**Enable and Disable LED Temperature Monitoring.** 0: LED temperature monitoring disabled. 1: LED temperature monitoring enabled
6	LEDHOT	R/W	0	**LED Excessive Temperature Flag.** This bit can be reset by writing a logic level zero. 0: TS input voltage > 0.345 V. 1: TS input voltage < 0.345 V.
5	LEDWARN	R	0	**LED Temperature Warning Flag (Read Only).** This flag is reset after readout. 0: TS input voltage > 1.05 V. 1: TS input voltage < 1.05 V.
4	LEDHDR	R	0	**LED High-Current Regulator Headroom Voltage Monitoring bit.** This bit returns the headroom voltage status of the LED high-current regulators. This value is being updated at the end of a flash strobe, before the LED current ramp-down phase. 0: Low headroom voltage. 1: Sufficient headroom voltage.
3–0	OV[3:0]	R/W	1001	**Output Voltage Selection bits.** In read mode, these bits return the result of the high-current LED forward voltage self-calibration procedure. In write mode, these bits are used to set the target output voltage (see *Down-Mode in Voltage Regulation Mode*). In applications requiring dynamic voltage control, care must be take to set the new target code after voltage mode operation has been enabled (MODE_CTRL[1:0] = 11 or ENVM bit = 1). OV[3:0]: Target output voltage 0000: 3.825 V 0001: 3.950 V 0010: 4.075 V 0011: 4.200 V 0100: 4.325 V 0101: 4.450 V 0110: 4.575 V 0111: 4.700 V 1000: 4.825 V 1001: 4.950 V 1010: 5.075 V 1011: 5.200 V 1100: 5.325 V 1101: 5.450 V 1110: 5.575 V 1111: 5.700 V

8.5.12 REGISTER7

Memory location: 0x07

Figure 72. REGISTER7 Fields

7	6	5	4	3	2	1	0
					REVID[2:0]		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. REGISTER7 Field Descriptions

Bit	Field	Type	Reset	Description
2–0	REVID[2:0](1)	R	100	Silicon Revision ID.

(1) Bit values may differ depending on the product die revision number.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6130xx can drive up to three white LEDs in parallel (400-mA, 800-mA, and 400-mA maximum flash current). The extended high-current mode (HC_SEL) allows up to 1025-mA, 2050-mA, and 1025-mA flash current. The 2-MHz switching frequency allows the use of small and low profile passive components.

9.2 Typical Applications

9.2.1 4100-mA Two White High-Power LED Flashlight Featuring Storage Capacitor

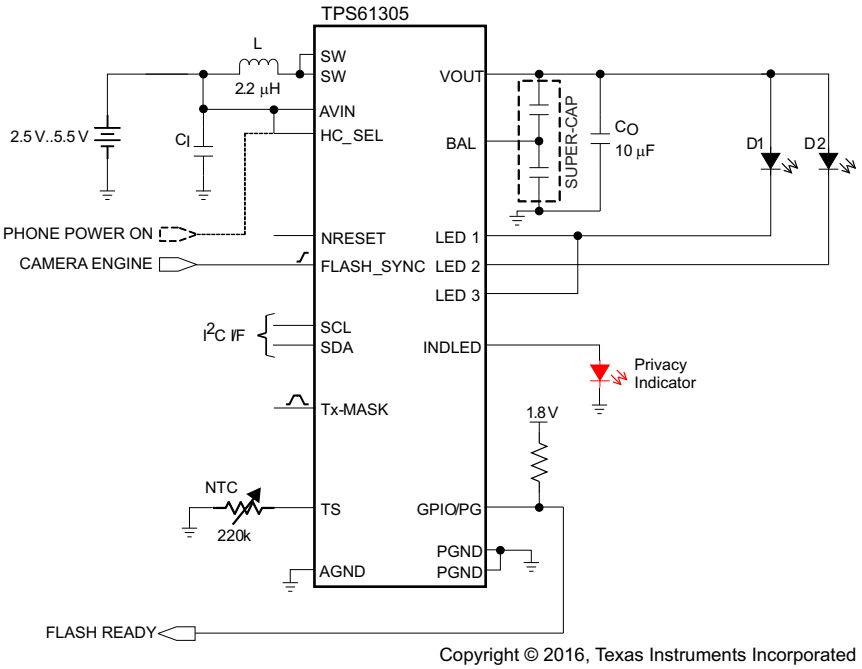

Figure 73. 4100-mA Two White High-Power LED Flashlight Featuring Storage Capacitor

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 21 as the input parameters.

Table 21. TPS61305 Design Requirement

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	2.5 V to 5.5 V
Output Voltage	4.95 V
Operating Freqency	2 MHz

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor Selection

A boost converter requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. The TPS6130xx device integrates a current limit protection circuitry. The valley current of the PMOS rectifier is sensed to limit the maximum current flowing through the synchronous rectifier and the inductor. The valley peak current limit (250 mA, 500 mA, 1250 mA, or 1750 mA) is user selectable through the I^2C interface.

To optimize solution size, the TPS6130xx device has been designed to operate with inductance values between a minimum of 1.3 µH and maximum of 2.9 µH. TI recommends a 2.2-µH inductance in typical high current white LED applications.

The highest peak current through the inductor and the power switch depends on the output load, the input and output voltages. Estimation of the maximum average inductor current and the maximum inductor peak current can be done using Equation 2 and Equation 3:

$$I_L \approx I_{OUT} \times \frac{V_{OUT}}{\eta \times V_{IN}} \tag{2}$$

$$I_{L(PEAK)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1-D) \times \eta} \quad \text{with } D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{3}$$

where

- f = switching frequency (2 MHz)
- L = inductance value (2.2 µH)
- η = estimated efficiency (85%)

The losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

9.2.1.2.2 Input Capacitor

TI recommends low ESR ceramic capacitors for good input voltage filtering. TI recommends a 10-µF input capacitor to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. The input capacitor must be placed as close as possible to the input pin of the converter.

9.2.1.2.3 Output Capacitor

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 4:

$$C_{min} \approx \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}} \tag{4}$$

where

- f is the switching frequency and ΔV is the maximum allowed ripple

With a chosen ripple voltage of 10 mV, a minimum capacitance of 10 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 5:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \tag{5}$$

The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. Additional ripple is caused by load transients. This means that the output capacitor has to completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change.

For the standard current white LED application (HC_SEL = 0, TPS6130xx), a minimum of 3-µF effective output capacitance is usually required when operating with 2.2-µH (typical) inductors. For solution size reasons, this is usually one or more X5R or X7R ceramic capacitors.

Depending on the material, size and therefore margin to the rated voltage of the used output capacitor, degradation on the effective capacitance can be observed. This loss of capacitance is related to the DC bias voltage applied. TI recommends ensuring the selected capacitors are showing enough effective capacitance under real operating conditions.

To support high-current camera flash application (HC_SEL = 1), the converter is designed to work with a low voltage super-capacitor on the output to take advantage of the benefits they offer. A low-voltage super-capacitor in the 0.1-F to 1.5-F range, and with ESR larger than 40 mΩ, is suitable in the TPS6130xx application circuit. For this device the output capacitor must be connected between the VOUT pin and a good ground connection.

9.2.1.2.4 NTC Selection (TPS61305, TPS61305A, TPS61306)

The TPS61305, TPS61305A, and TPS61306 require a negative thermistor (NTC) for sensing the LED temperature. Once the temperature monitoring feature is activated, a regulated bias current (≈24 µA) will be driven out of the TS port and produce a voltage across the thermistor.

If the temperature of the NTC-thermistor rises due to the heat dissipated by the LED, the voltage on the TS input pin decreases. When this voltage goes below the warning threshold, the LEDWARN bit in REGISTER6 is set. This flag is cleared by reading the register.

If the voltage on the TS input decreases further and falls below *hot threshold*, the LEDHOT bit in REGISTER6 is set and the device goes automatically in shutdown mode to avoid damaging the LED. This status is latched until the LEDHOT flag gets cleared by software.

The selection of the NTC-thermistor value strongly depends on the power dissipated by the LED and all components surrounding the temperature sensor and on the cooling capabilities of each specific application. With a 220-kΩ (at 25°C) thermistor, the valid temperature window is set between 60°C to 90°C. The temperature window can be enlarged by adding external resistors to the TS pin application circuit. To ensure proper triggering of the LEDWARN and LEDHOT flags in noisy environments, the TS signal may require additional filtering capacitance.

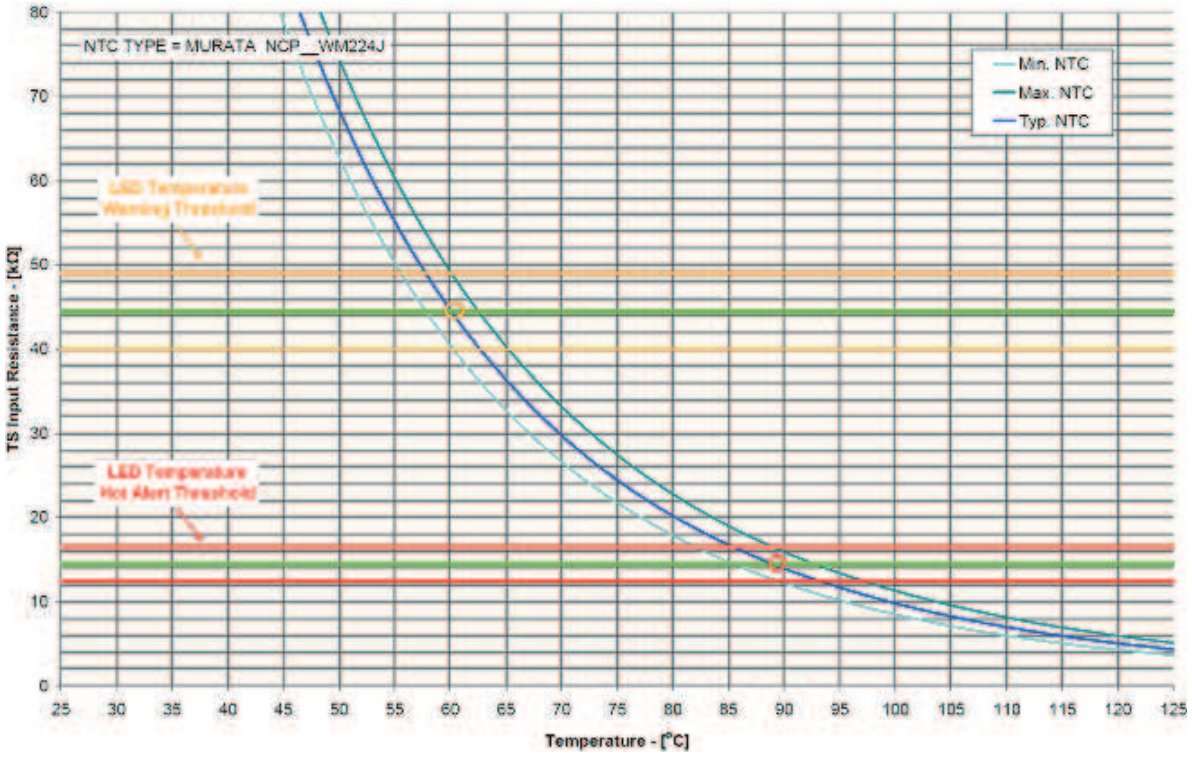

Figure 74. Temperature Monitoring Characteristic

9.2.1.2.5 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations the regulation loop may be unstable. This is often a result of improper board layout or L-C combination.

As a next step in the evaluation of the regulation loop the load transient response needs to be tested. VOUT can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters, such as MOSFET $r_{DS(on)}$, that are temperature dependant, the loop stability analysis has to be done over the input voltage range, output current range, and temperature range.

9.2.1.3 Application Curves

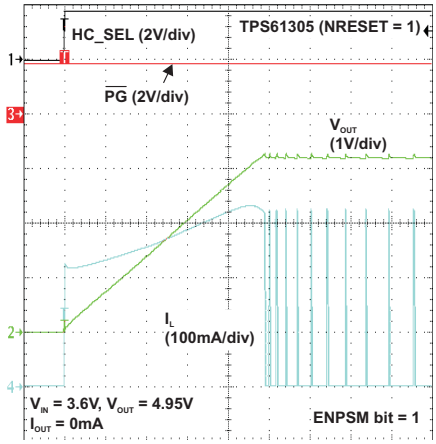

Figure 75. Storage Capacitor Precharge (HC_SEL = 1)

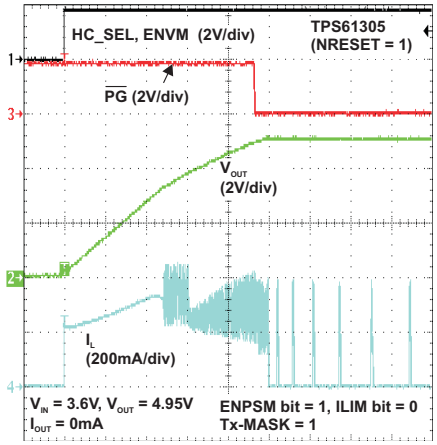

Figure 76. Storage Capacitor Charge-Up (HC_SEL = 1)

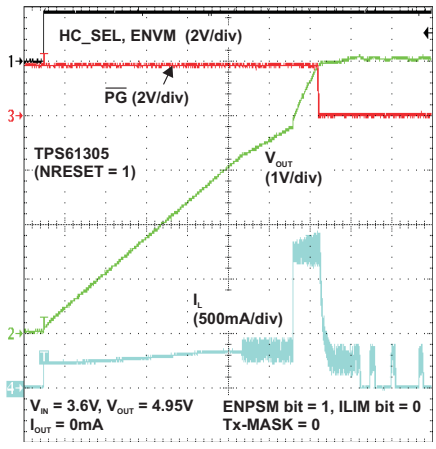

Figure 77. Storage Capacitor Charge-Up (HC_SEL = 1)

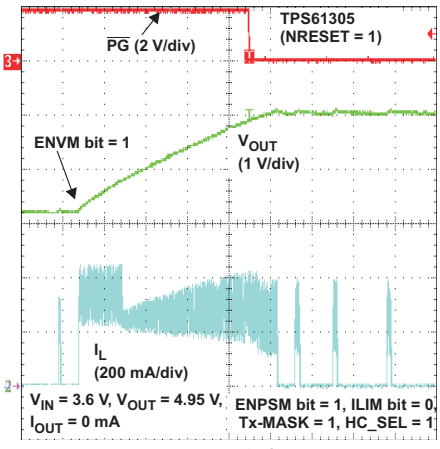

Figure 78. Storage Capacitor Charge-Up (HC_SEL = 1)

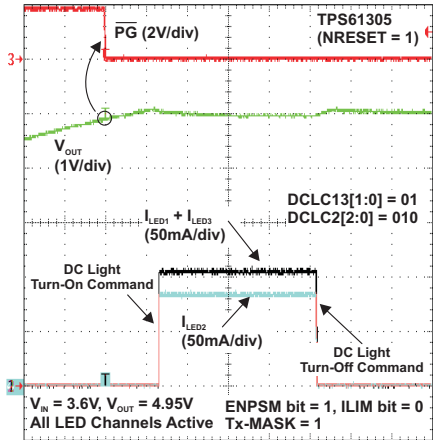

Figure 79. DC Light Operation (HC_SEL = 1)

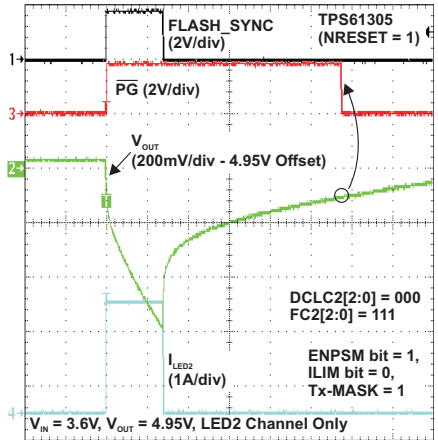

Figure 80. Flash Sequence (HC_SEL = 1)

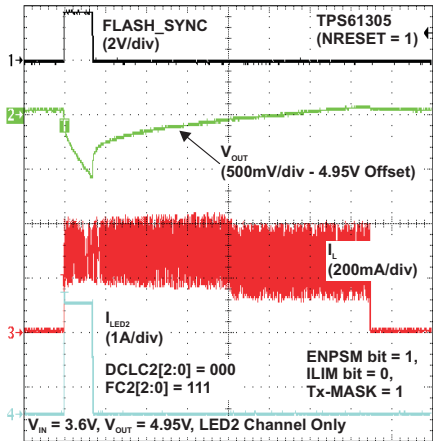

Figure 81. Flash Sequence (HC_SEL = 1)

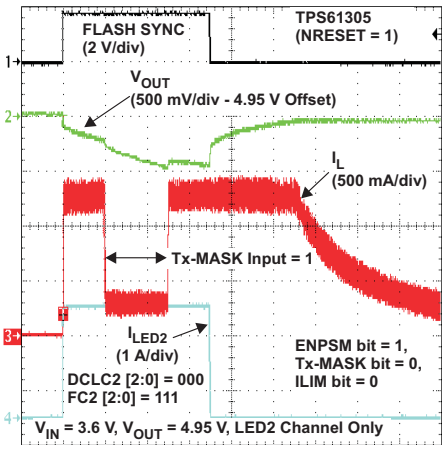

Figure 82. Flash Sequence (HC_SEL = 1)

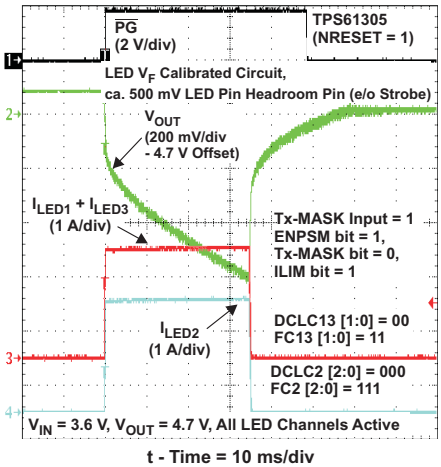

Figure 83. Flash Sequence (HC_SEL = 1)

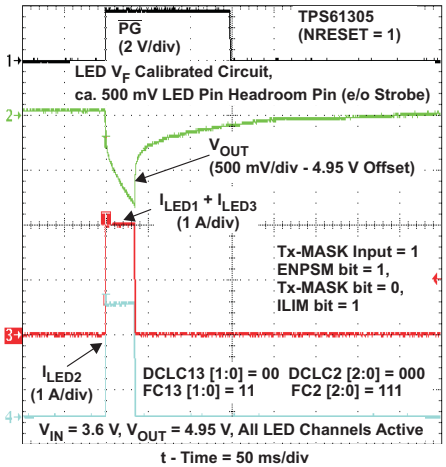

Figure 84. Flash Sequence (HC_SEL = 1)

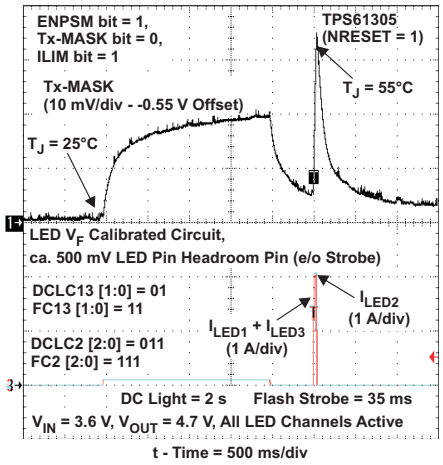

Figure 85. Junction Temperature Monitoring (HC_SEL = 1)

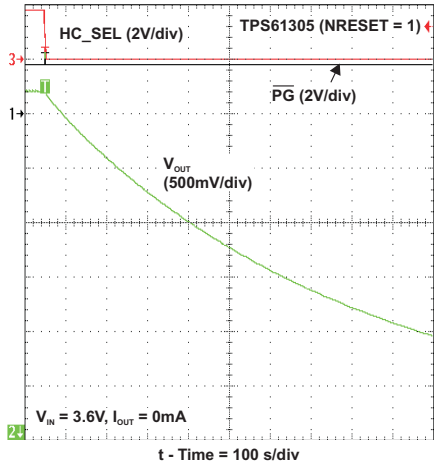

Figure 86. Shutdown (HC_SEL = 1)

9.2.2 TPS61300 Typical Application

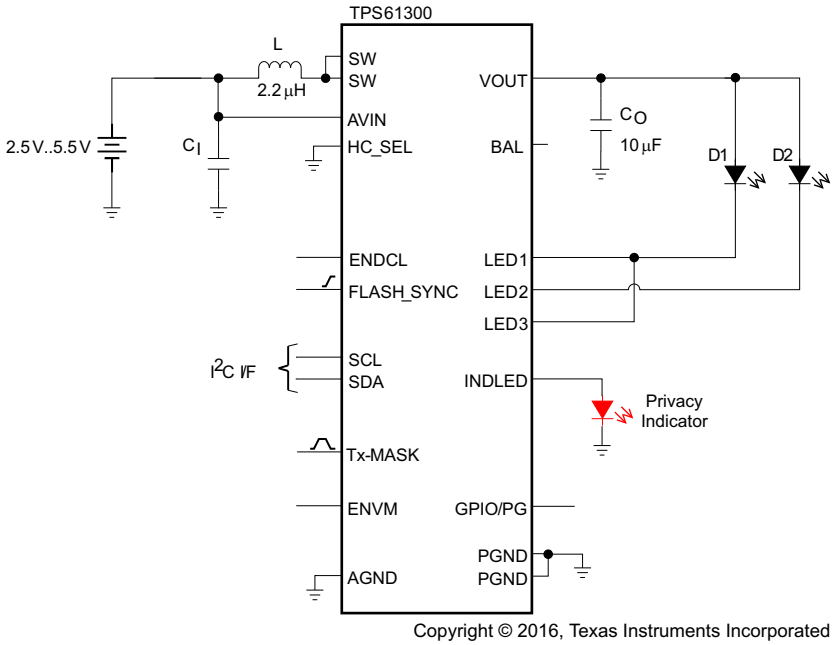

Figure 87. TPS61300 Typical Application Circuit

9.2.2.1 Design Requirement

For this design example, use the parameters listed in Table 22 as the input parameters.

Table 22. TPS61300 Design Requirement

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	2.5 V to 5.5 V
Output Voltage	4.95 V
Operating Freqency	2 MHz

9.2.2.2 Application Curves

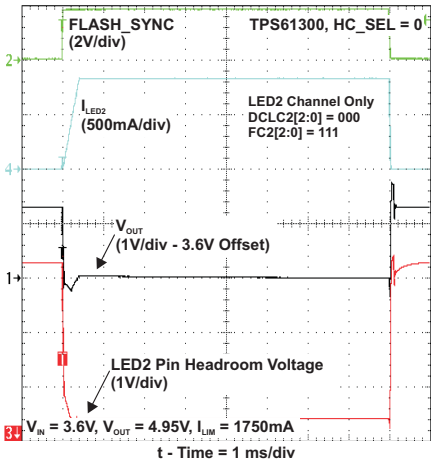

Figure 88. Flash Sequence (HC_SEL = 0)

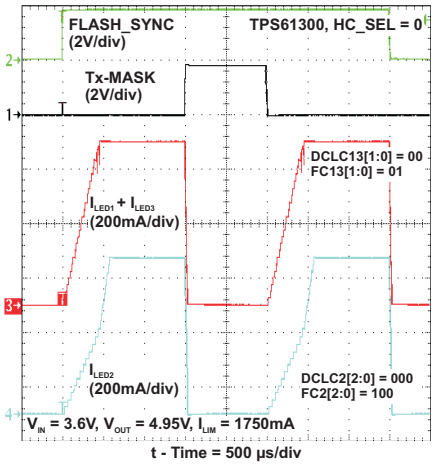

Figure 89. Tx-Masking Operation (HC_SEL = 0)

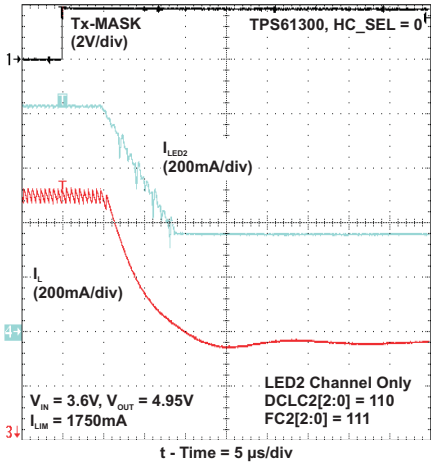

Figure 90. Tx-Masking Operation (HC_SEL = 0)

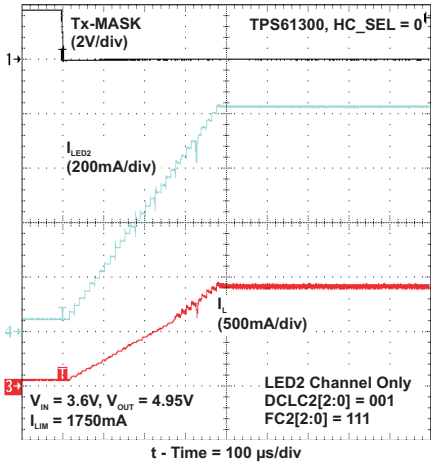

Figure 91. Tx-Masking Operation (HC_SEL = 0)

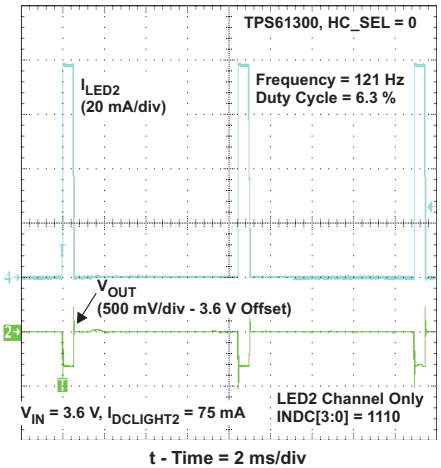

Figure 92. Low-Light Dimming Mode Operation

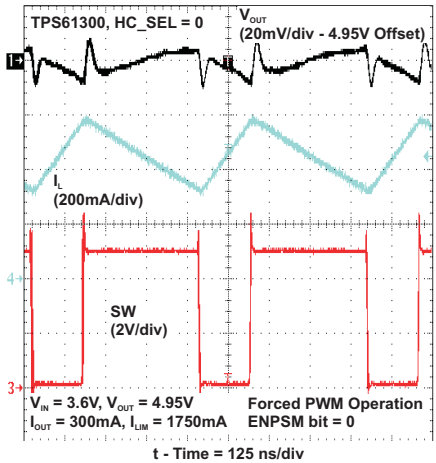

Figure 93. PWM Operation

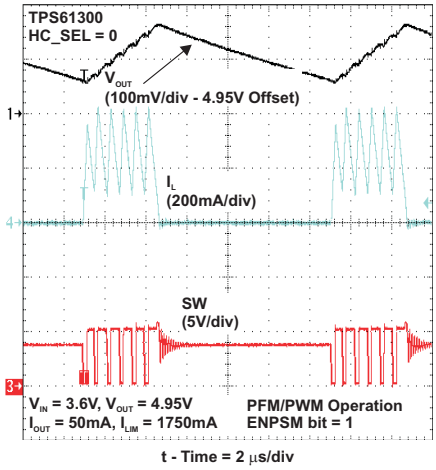

Figure 94. PFM Operation

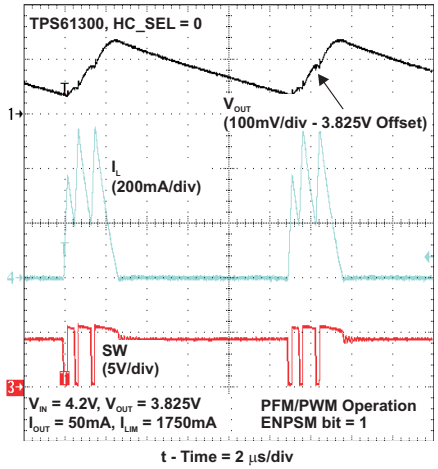

Figure 95. Down-Mode Operation (Voltage Mode)

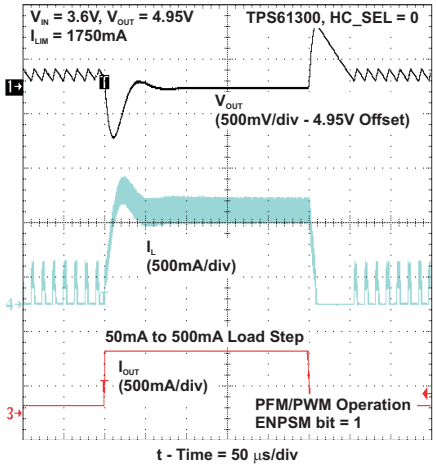

Figure 96. Voltage Mode Load Transient Response

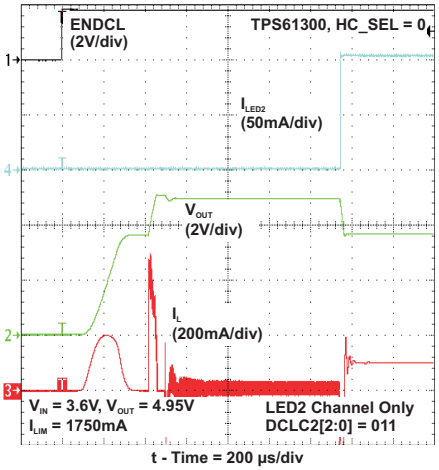

Figure 97. Start-Up Into DC Light Operation

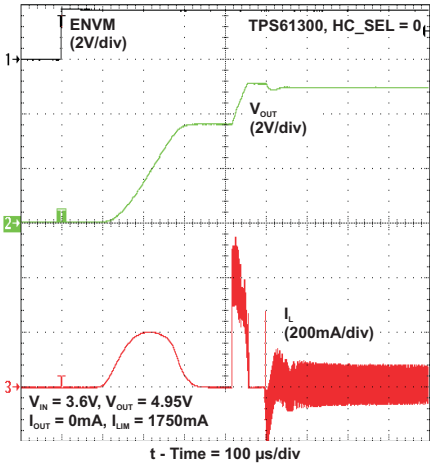

Figure 98. Start-Up Into Voltage Mode Operation

9.3 System Examples

9.3.1 2x 600-mA High-Power White LED Solution Featuring Privacy Indicator

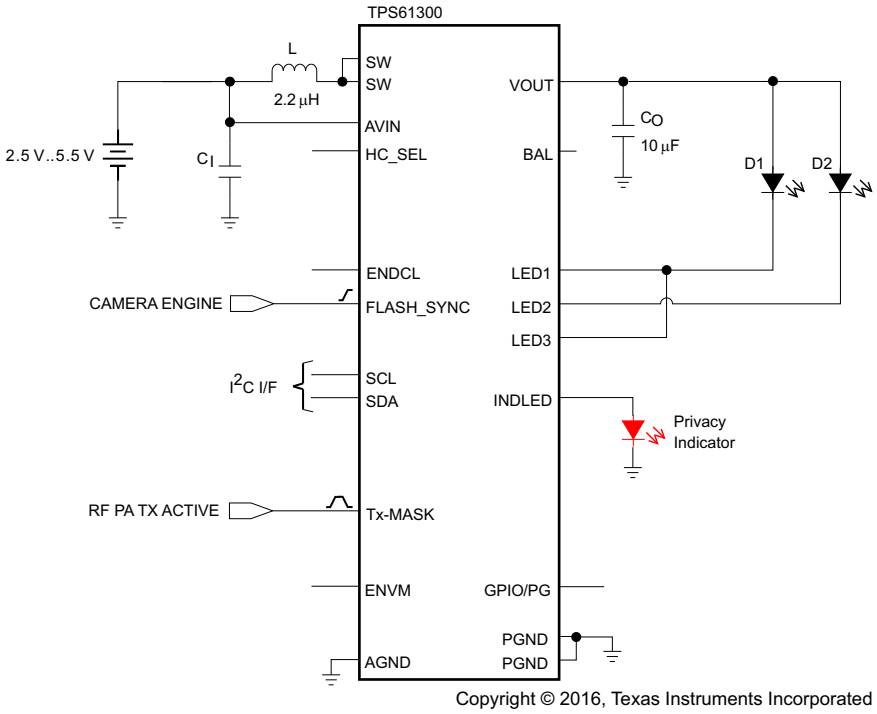

Figure 99. 2× 600-mA High-Power White LED Solution Featuring Privacy Indicator

9.3.2 White LED Flashlight Driver and Audio Amplifier Power Supply Operating Simultaneously

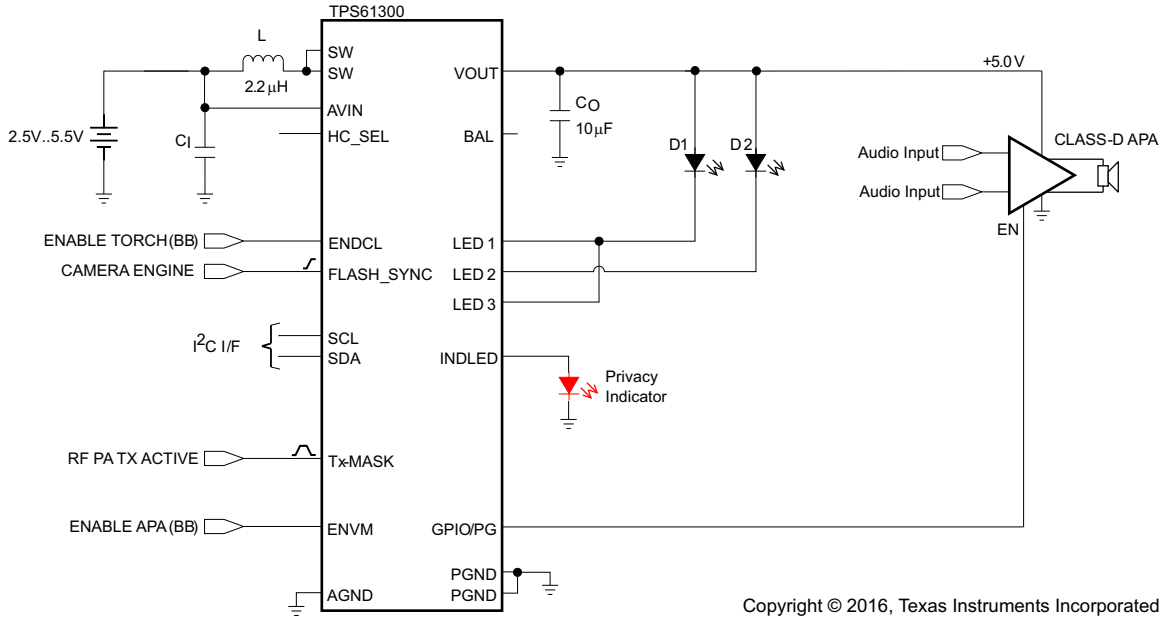

Figure 100. White LED Flashlight Driver and Audio Amplifier Power Supply Operating Simultaneously

System Examples (continued)

9.3.3 White LED Flashlight Driver and Audio Amplifier Power Supply Operating Simultaneously

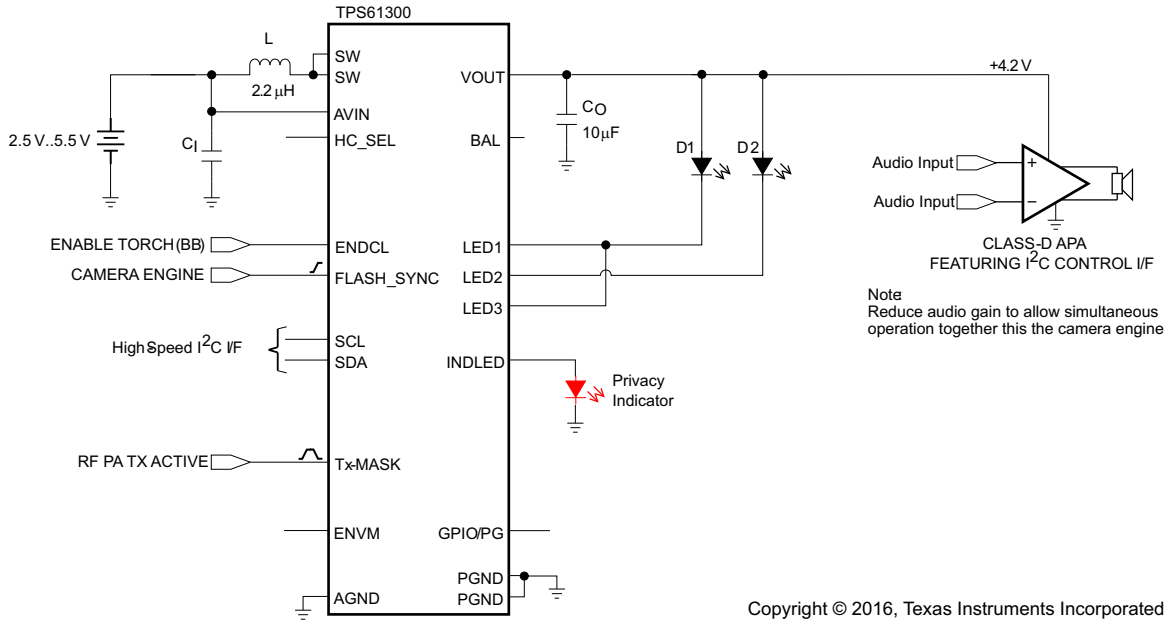

Figure 101. White LED Flashlight Driver and Audio Amplifier Power Supply Operating Simultaneously

9.3.4 White LED Flashlight Driver and Audio Amplifier Power Supply Exclusive Operation

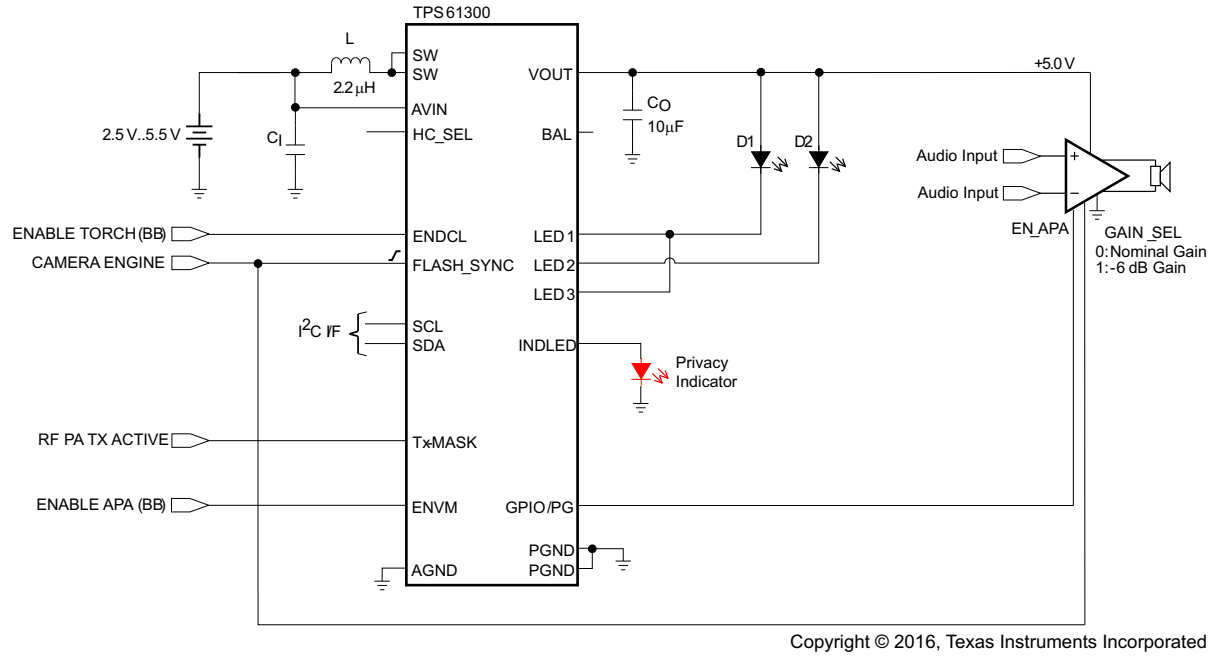

Figure 102. White LED Flashlight Driver and Audio Amplifier Power Supply Exclusive Operation

System Examples (continued)

9.3.5 White LED Flashlight Driver and Auxiliary Lighting Zone Power Supply

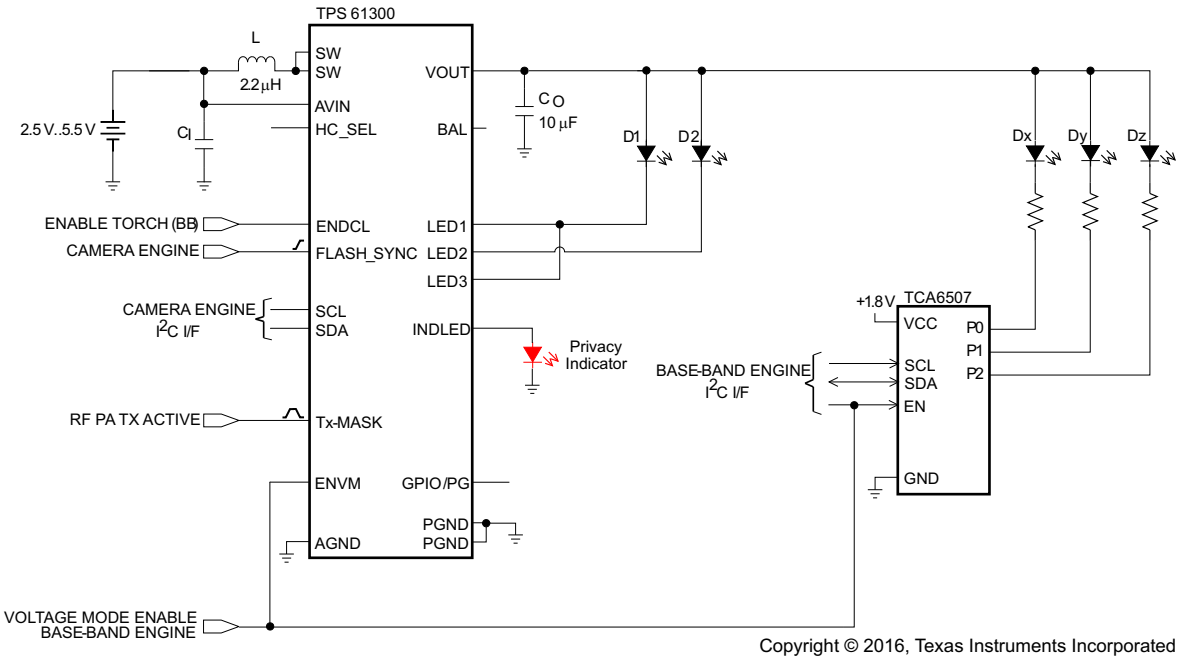

Figure 103. White LED Flashlight Driver and Auxiliary Lighting Zone Power Supply

9.3.6 TPS61300, Typical Application

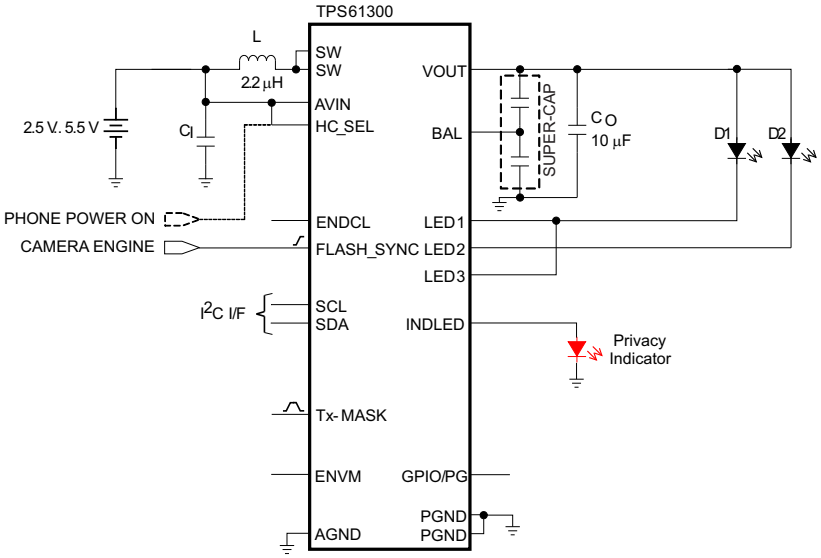

Figure 104. TPS61300, Typical Application

System Examples (continued)

9.3.7 TPS61301, Typical Application

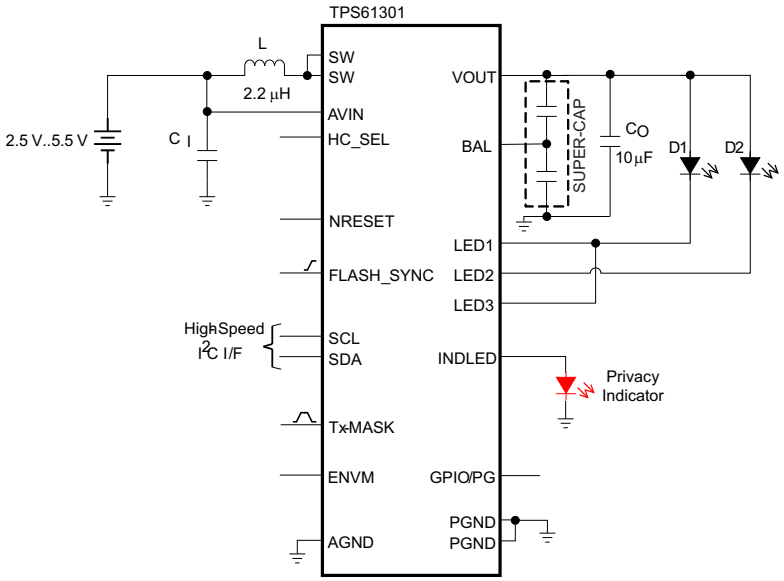

Figure 105. TPS61301, Typical Application

9.3.8 TPS61305 Typical Application

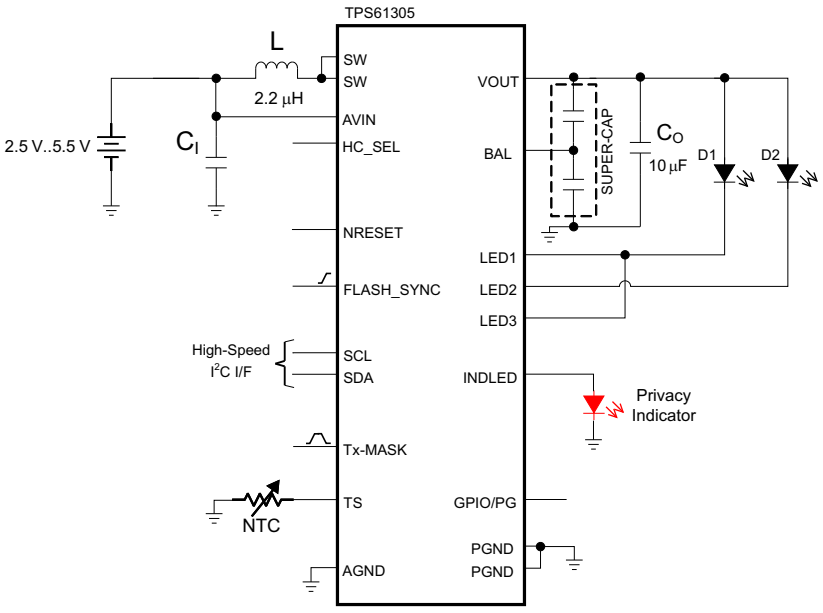

Figure 106. TPS61305, Typical Application

System Examples (continued)

9.3.9 TPS61306, Typical Application

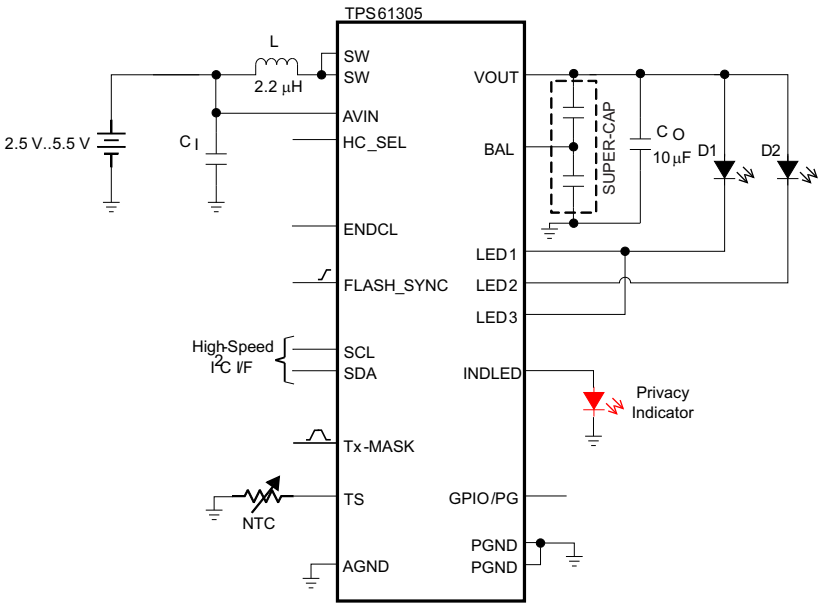

Figure 107. TPS61306, Typical Application

10 Power Supply Recommendations

The TPS6130xx is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the TPS6130xx, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks.

The input capacitor, output capacitor, and the inductor must be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

To lay out the control ground, TI recommends using short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

11.2 Layout Example

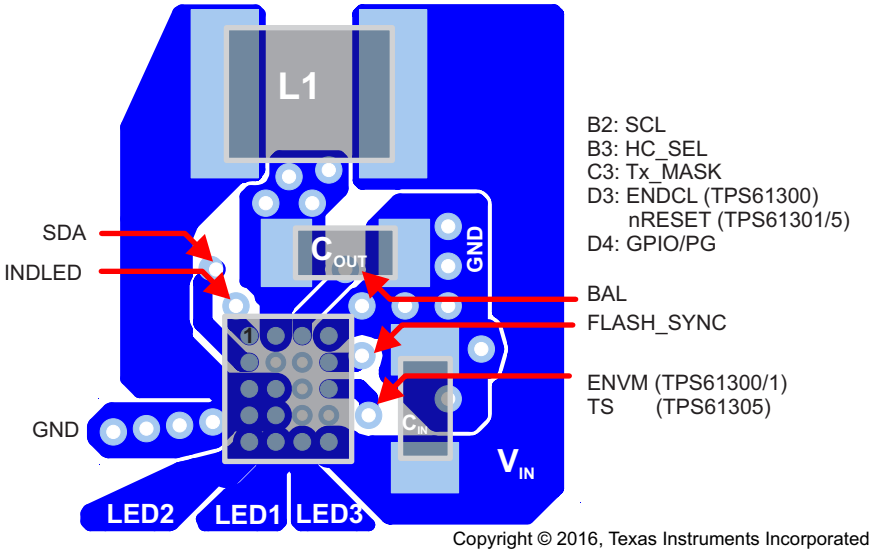

Figure 108. Suggested Layout (Top)

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The maximum junction temperature (T_J) of the TPS6130xx is 150°C.

The maximum power dissipation is especially critical when the device operates in the linear down mode at high LED current. For single pulse power thermal analysis (for example, flashlight strobe), the allowable power dissipation for the device is given by Figure 109. These values are derived using the reference design.

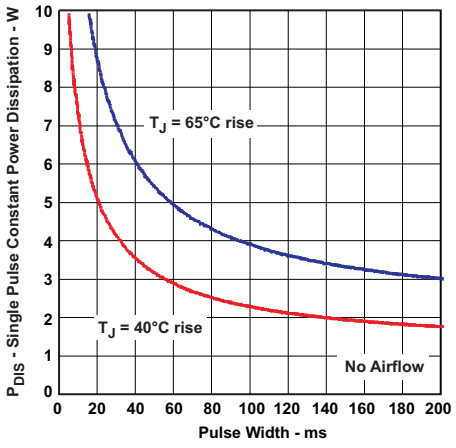

Figure 109. Single Pulse Power Capability

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 23. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61300	Click here	Click here	Click here	Click here	Click here
TPS61301	Click here	Click here	Click here	Click here	Click here
TPS61305	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61300YFFR	ACTIVE	DSBGA	YFF	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61300	Samples
TPS61300YFFT	ACTIVE	DSBGA	YFF	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61300	Samples
TPS61301YFFR	ACTIVE	DSBGA	YFF	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61301	Samples
TPS61301YFFT	ACTIVE	DSBGA	YFF	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61301	Samples
TPS61305YFFR	ACTIVE	DSBGA	YFF	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61305	Samples
TPS61305YFFT	ACTIVE	DSBGA	YFF	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61305	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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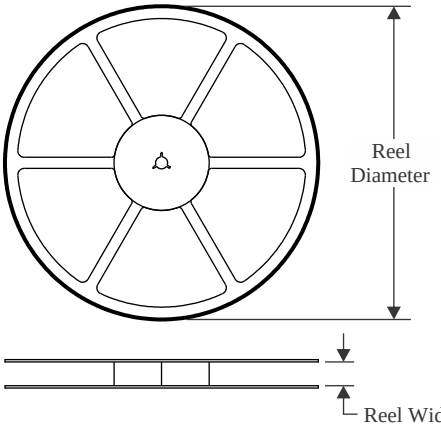
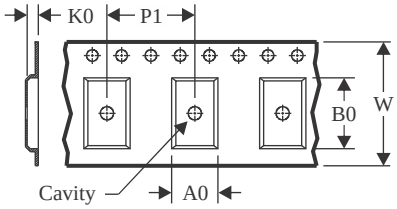
TAPE AND REEL INFORMATION

REEL DIMENSIONS

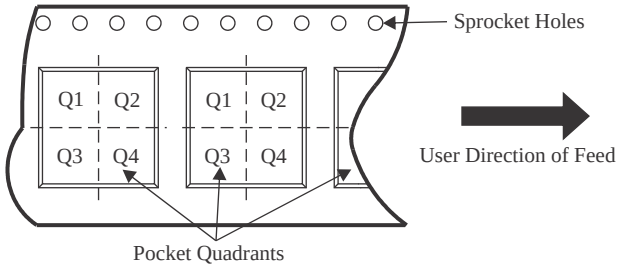


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

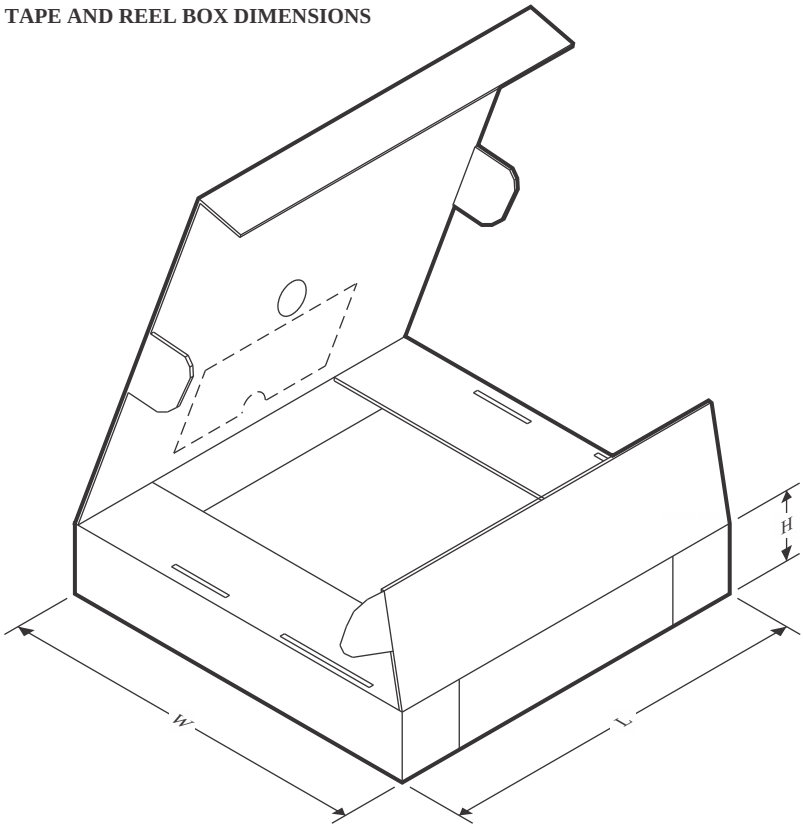
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61300YFFT	DSBGA	YFF	20	250	180.0	8.4	2.2	2.35	0.8	4.0	8.0	Q1
TPS61301YFFR	DSBGA	YFF	20	3000	180.0	8.4	2.13	2.33	0.69	4.0	8.0	Q1
TPS61301YFFT	DSBGA	YFF	20	250	180.0	8.4	2.13	2.33	0.69	4.0	8.0	Q1
TPS61305YFFR	DSBGA	YFF	20	3000	180.0	8.4	2.2	2.35	0.8	4.0	8.0	Q1
TPS61305YFFT	DSBGA	YFF	20	250	180.0	8.4	2.2	2.35	0.8	4.0	8.0	Q1

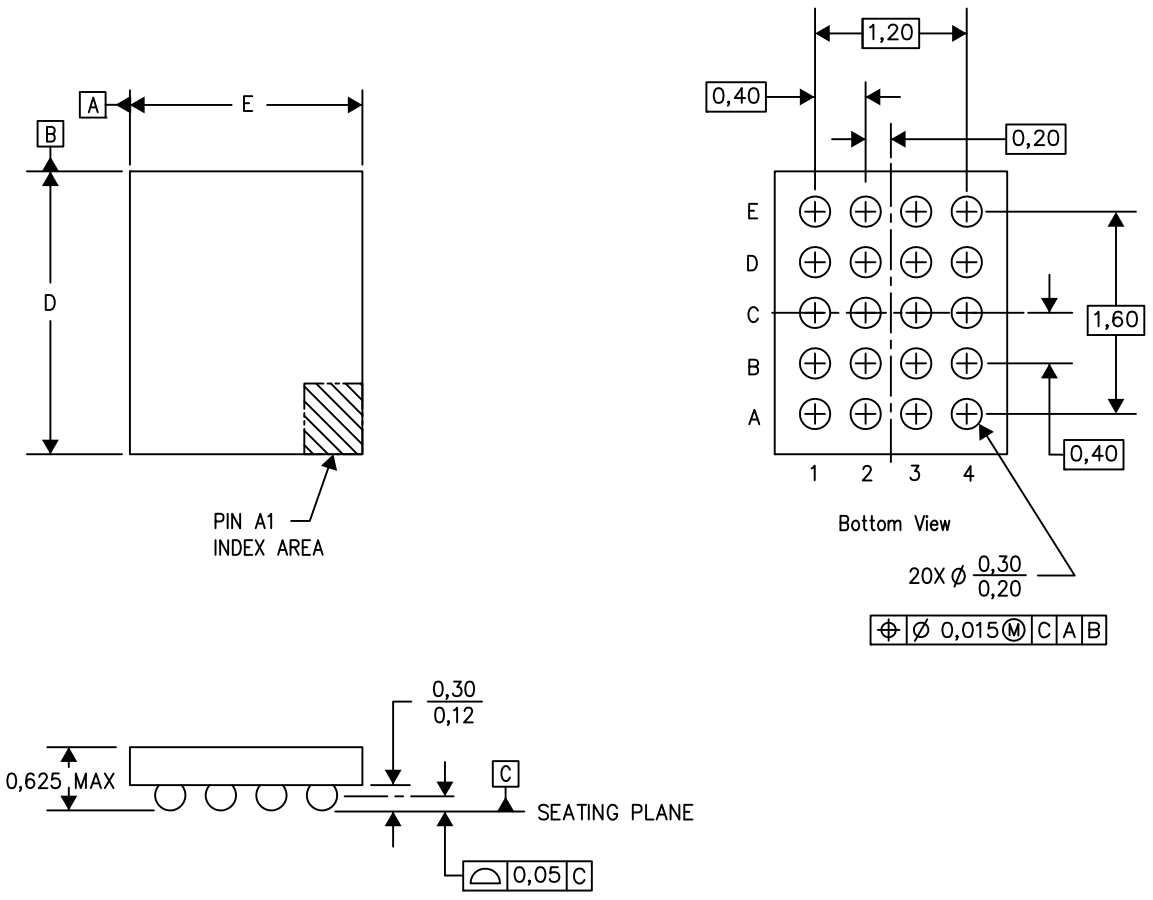
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61300YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0
TPS61301YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0
TPS61301YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0
TPS61305YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0
TPS61305YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0

YFF (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



4207625–9/AO 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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