

U_B12 B12.SchDoc
U_B13 B13.SchDoc
U_B14 B14.SchDoc
U_B15 B15.SchDoc
U_B16 B16.SchDoc
U_B34 B34.SchDoc

U_FPGA-MGT FPGA-MGT.SchDoc
U_FPGA-CFG FPGA-CFG.SchDoc
U_FPGA-MISC FPGA-MISC.SchDoc
U_FPGA-PWR FPGA-PWR.SchDoc

U_PWR1 PWR1.SchDoc
U_PWR2 PWR2.SchDoc

U_Clock Clock.SchDoc

U_B2B-Connectors B2B-Connectors.SchDoc

U_B33 B33.SchDoc

A

A

B

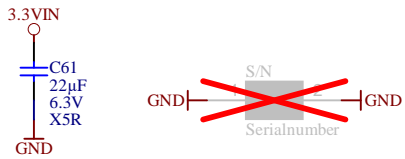
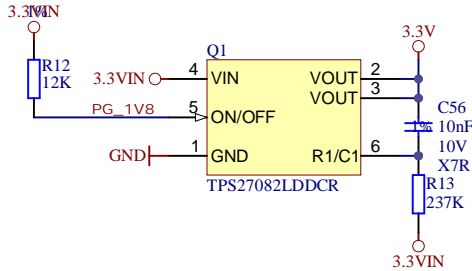
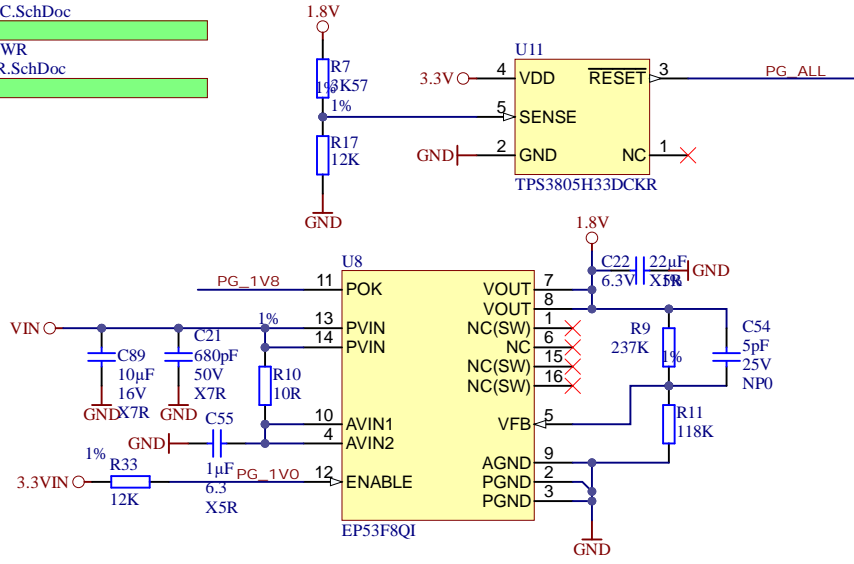
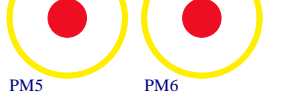
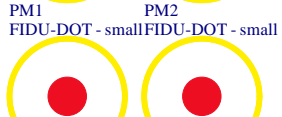
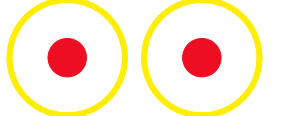
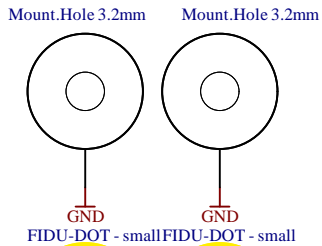
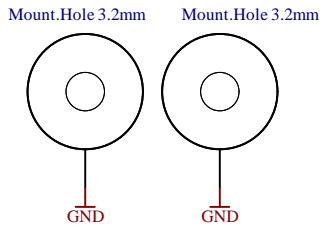
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C

C

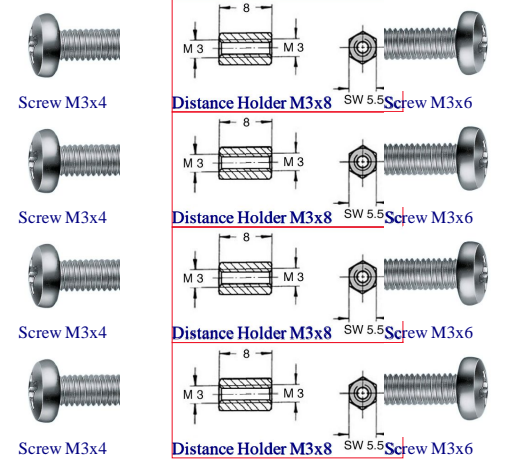
D

D



Serial
Serial
Serialnumber 6,3 x 6,3mm

Top of Board



Assembly variant	070-2CF
Created by	VT
Modified by	VT
Modified at	2017-01-23
SVN Revision	8679

	Title: TE0741		
	A4	Number: TE0741 070-2CF	Rev. 03
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	Filename: TE0741.SchDoc		

1

2

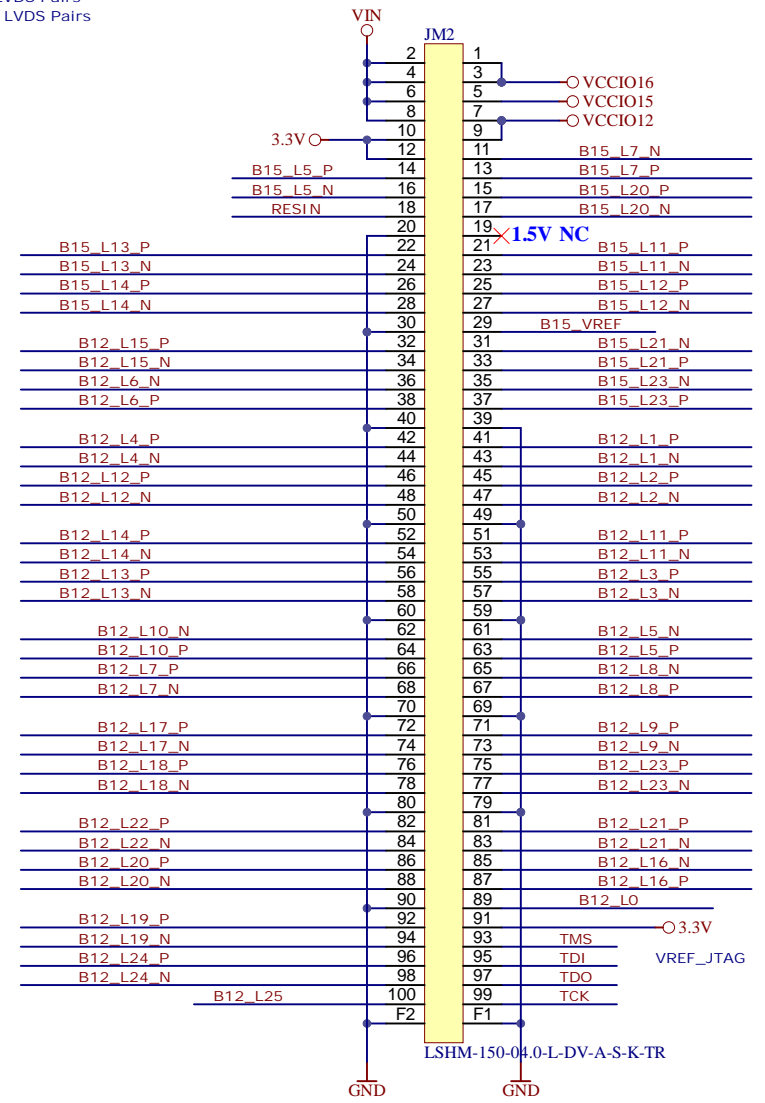
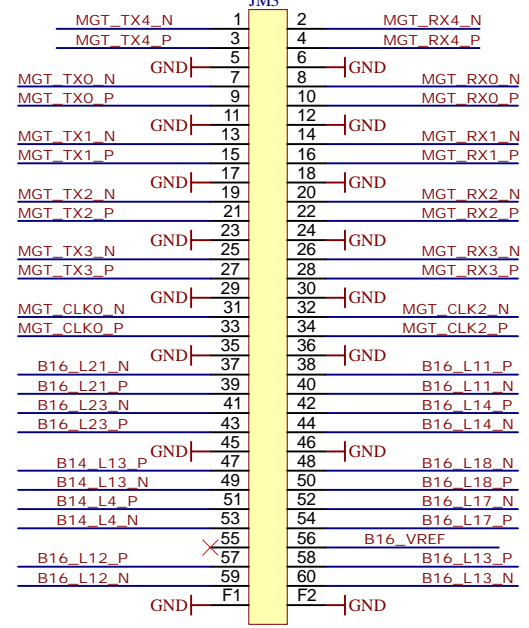
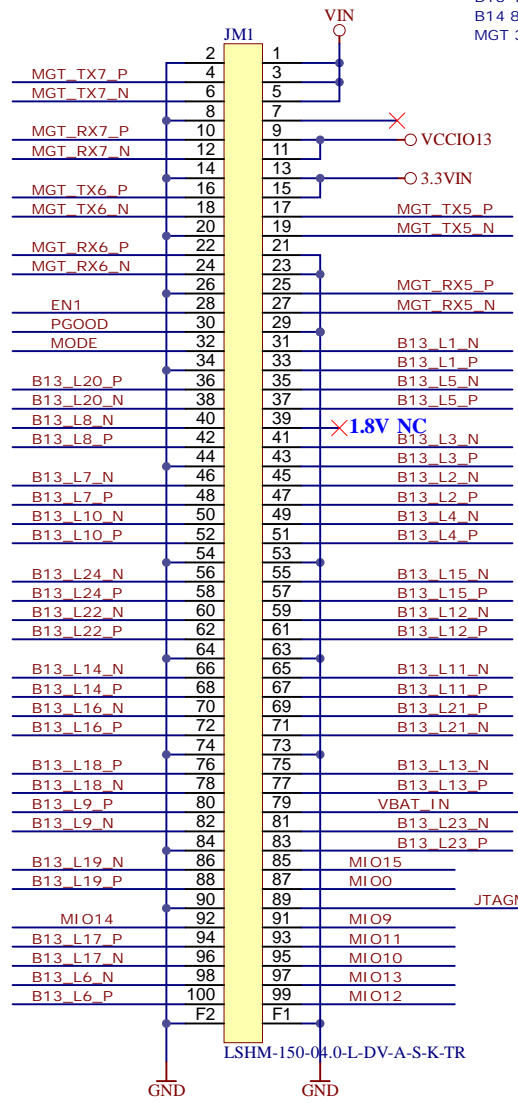
3

4

B13 48 IO, 24 LVDS Pairs
 B14 8 IO, 3.3V
 MGT 3 Lanes

B16 16 IO, 8 LVDS Pairs
 MGT 4 + 1 Lanes
 B14 4 IO, 3.3V

B15 18 IO, 9 LVDS Pairs
 B12 48 IO, 24 LVDS Pairs
 B12 2 IO



TE0720 Compatibility

MIO0 8 pins => 8 IO B14
 USB D+,D-, vbusen,otg_id => 4 IO B14
 SGMII => MGT
 MIO1(SDCARD) => MGT
 ETH MD1 => MGT
 B34 => B16, MGT
 B35 => B13
 B13 => B12
 B33 => B15

Clock Capable I/O
 All pins named
 Bxx_11_X
 Bxx_12_X
 Bxx_13_X
 Bxx_14_X
 Are Clock Capable I/O's



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1

2

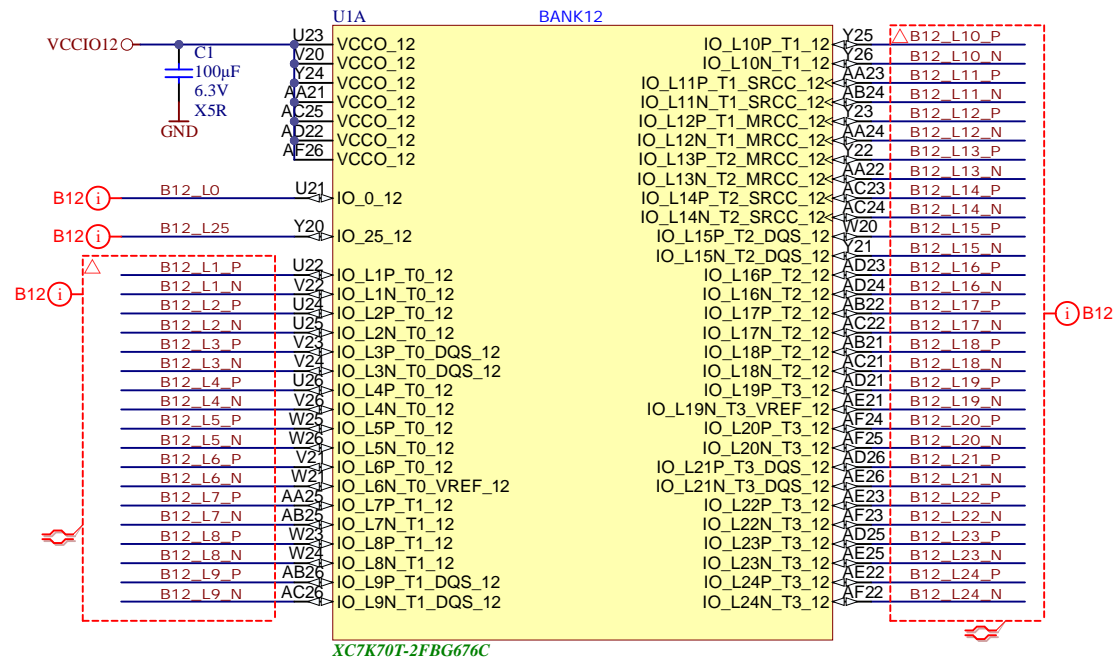
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4

B12_FIXED (i) △

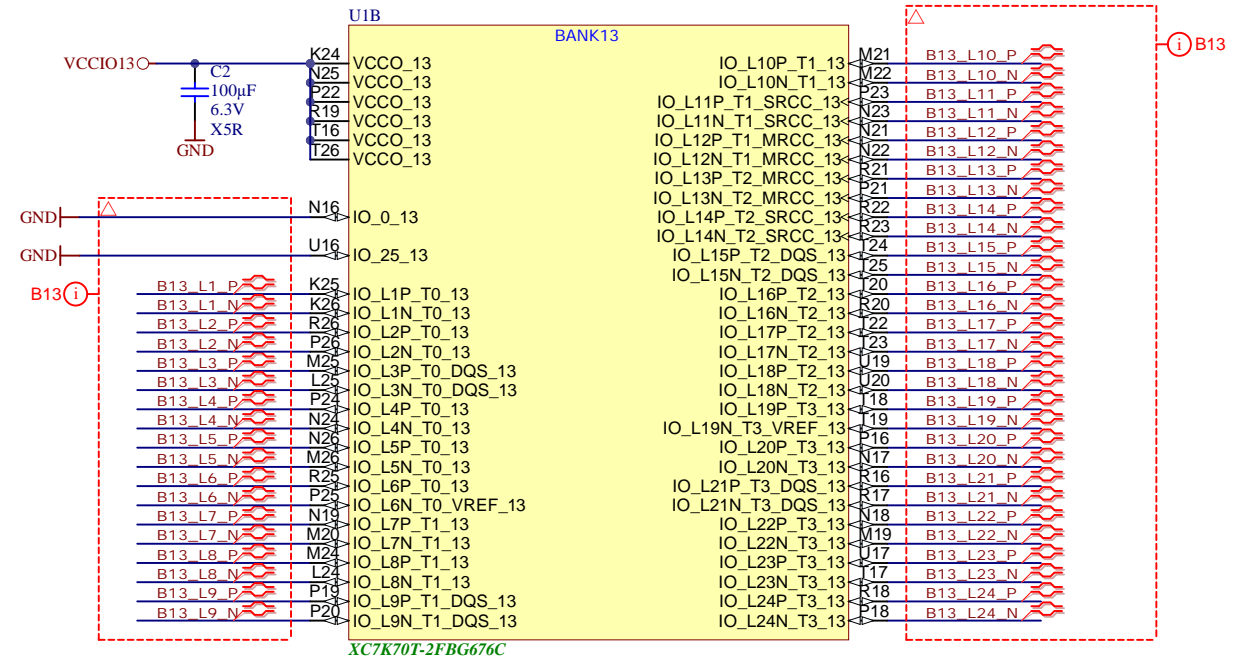
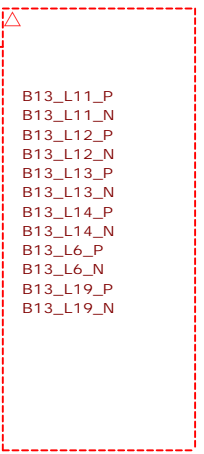
B12_L11_P
B12_L11_N
B12_L12_P
B12_L12_N
B12_L13_P
B12_L13_N
B12_L14_P
B12_L14_N
B12_L19_P
B12_L19_N
B12_L6_P
B12_L6_N

K70T version does not have this bank!



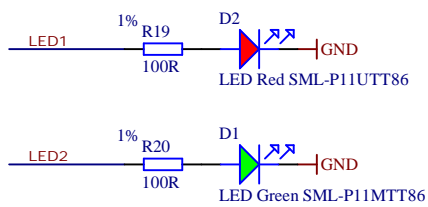
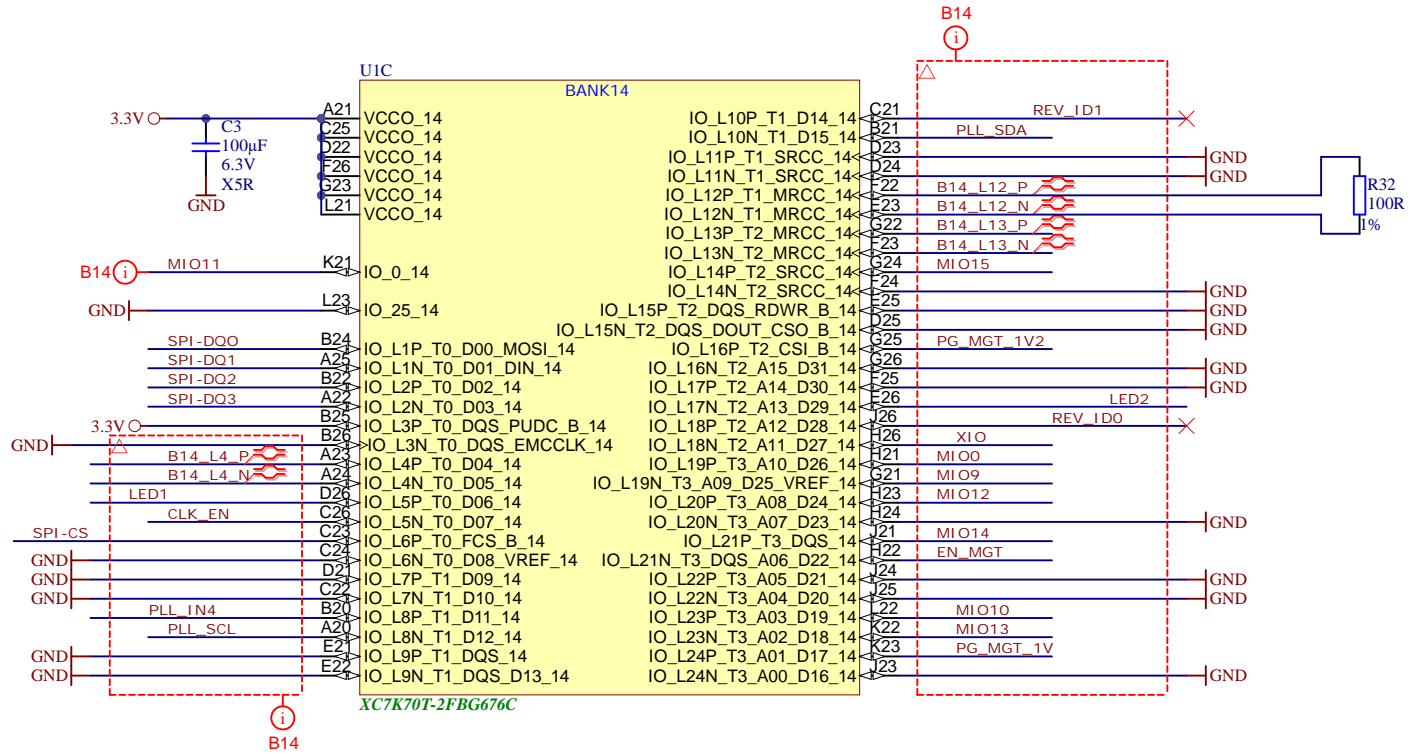
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	A4	Number: TE0741 070-2CF
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	Rev. 03	Page3 of 17
Filename: B12.SchDoc		


B13_FIXED (i)

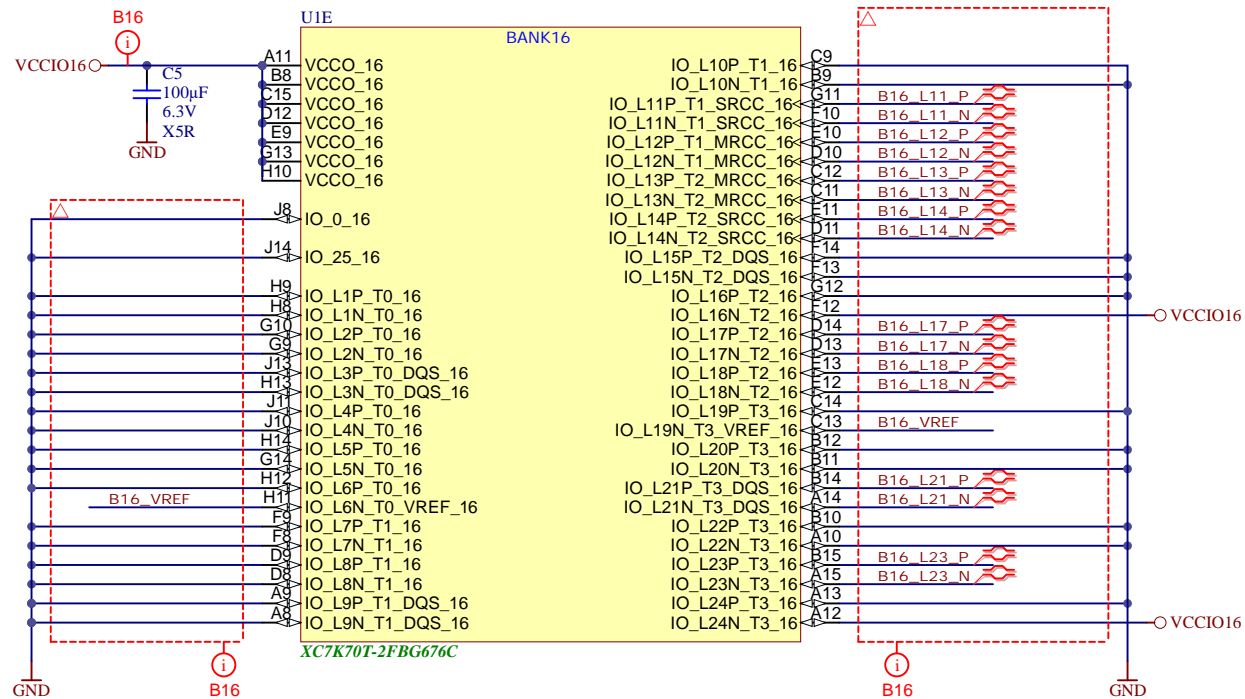



XC7K70T-2FBG676C

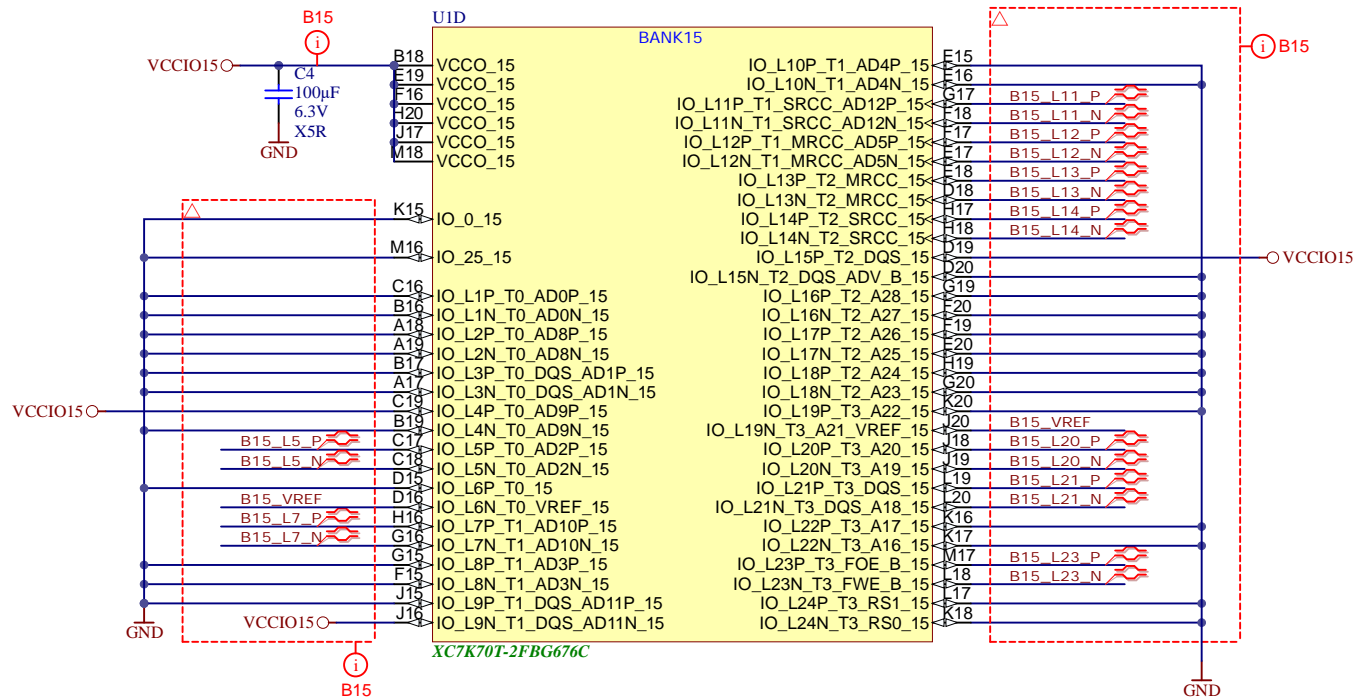
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	Filename: B13.SchDoc		



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A

A

B

B

C

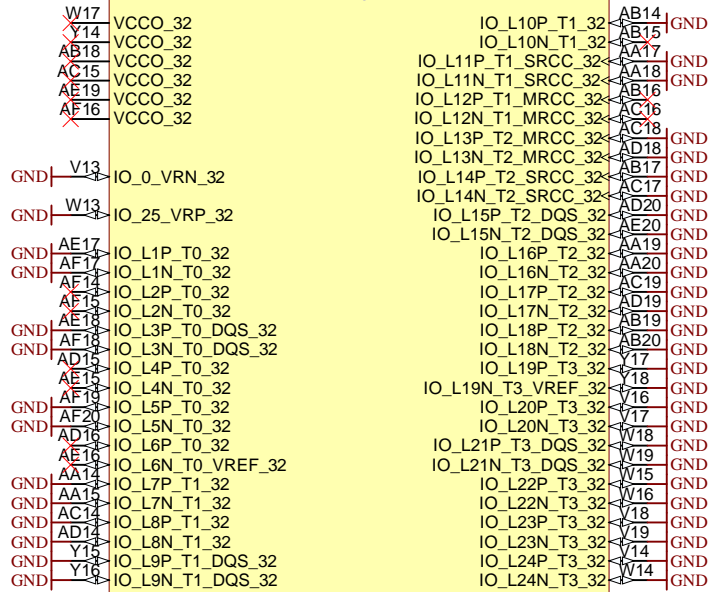
C

D

D

UIF

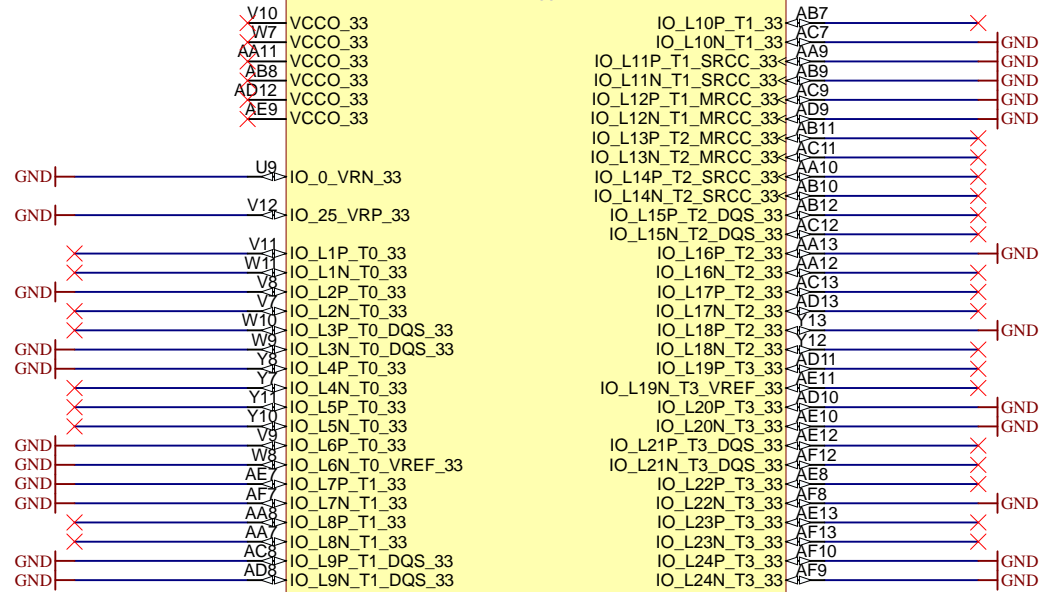
BANK32



XC7K70T-2FBG676C

UIG

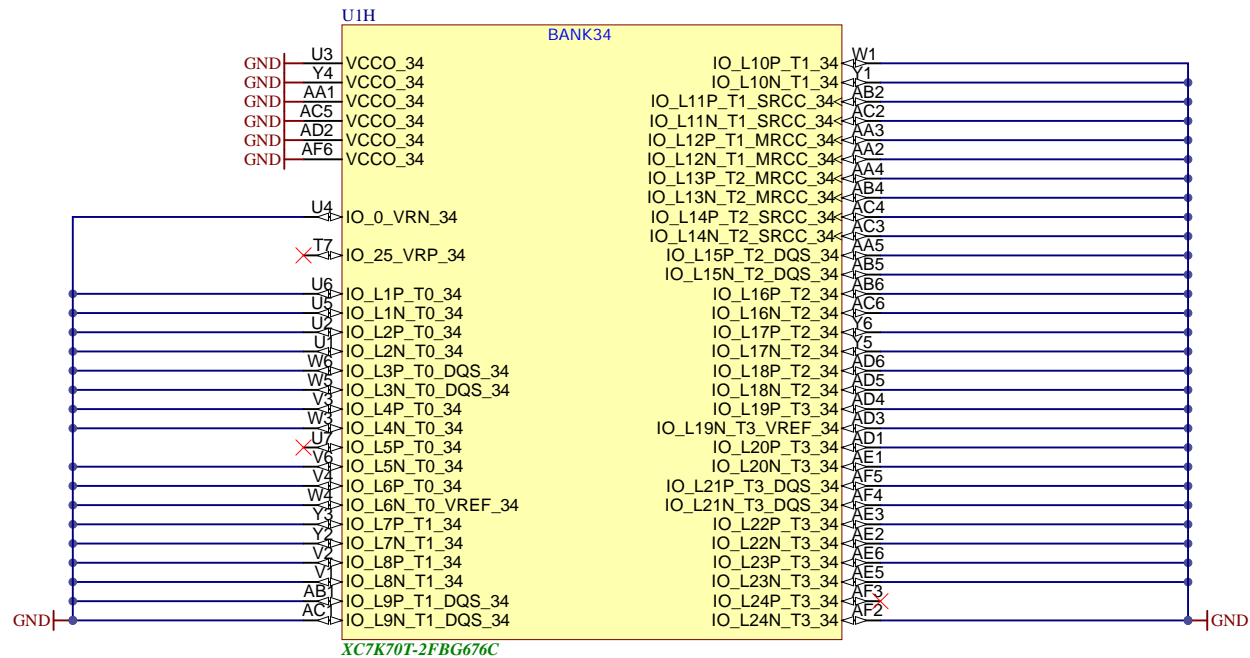
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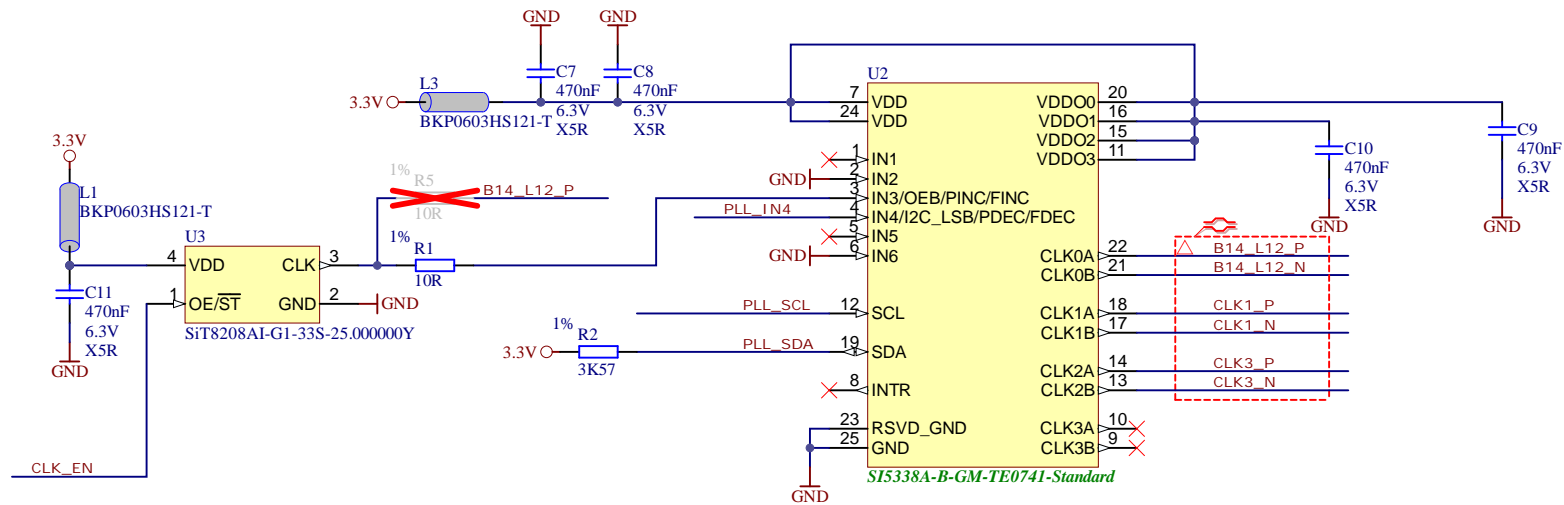
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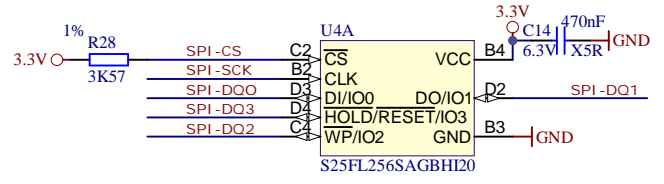
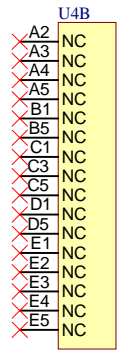
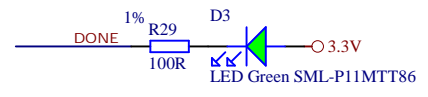
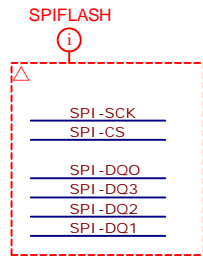
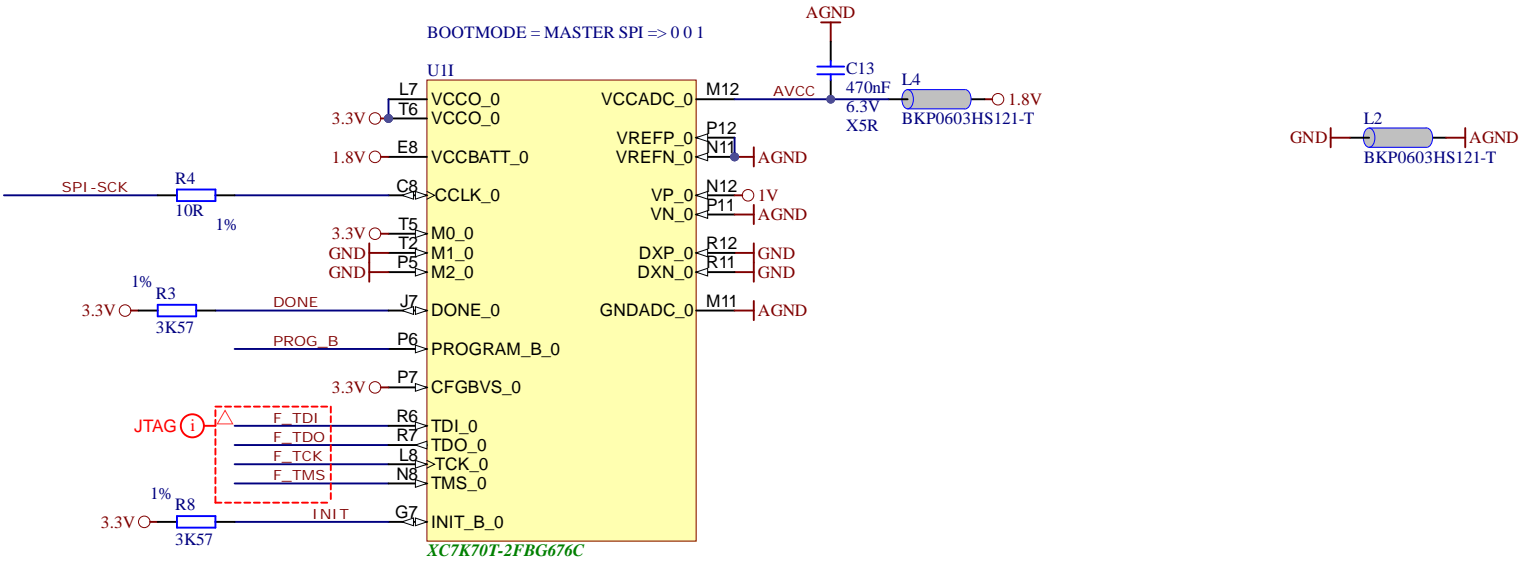


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Filename: B34.SchDoc		Page9 of 17	

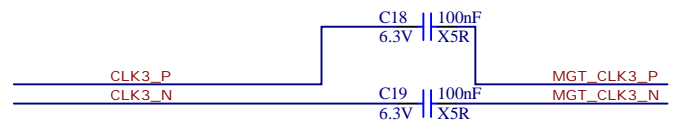
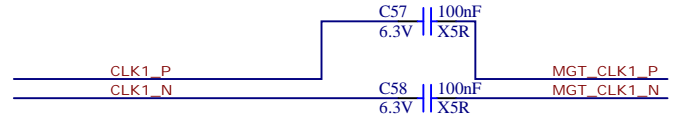
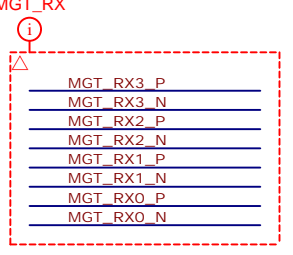
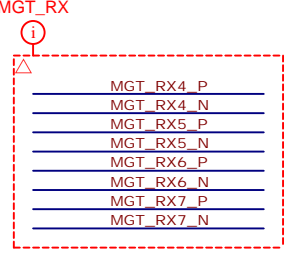
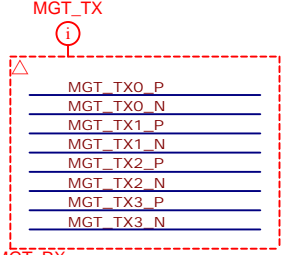
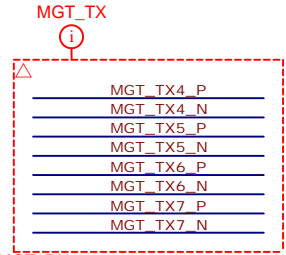
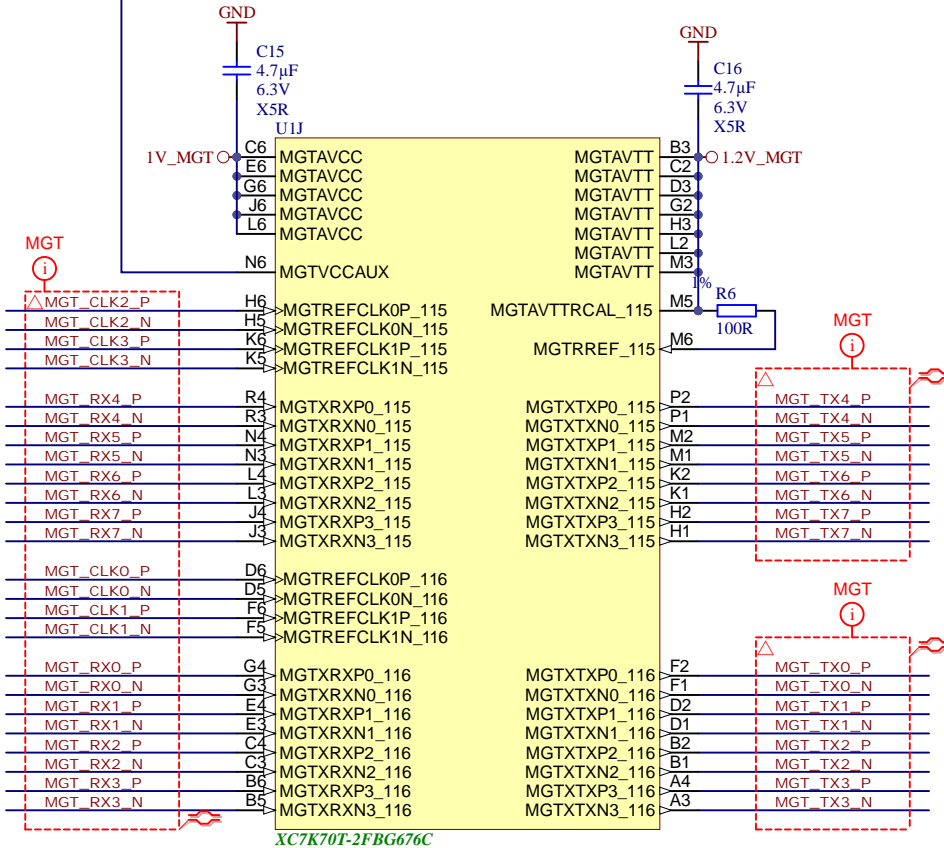
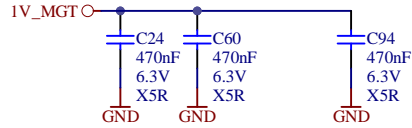
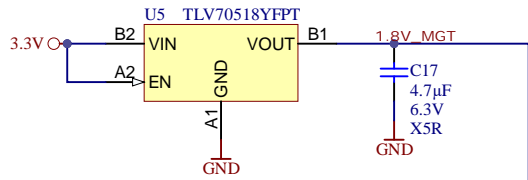


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	Filename: Clock.SchDoc		

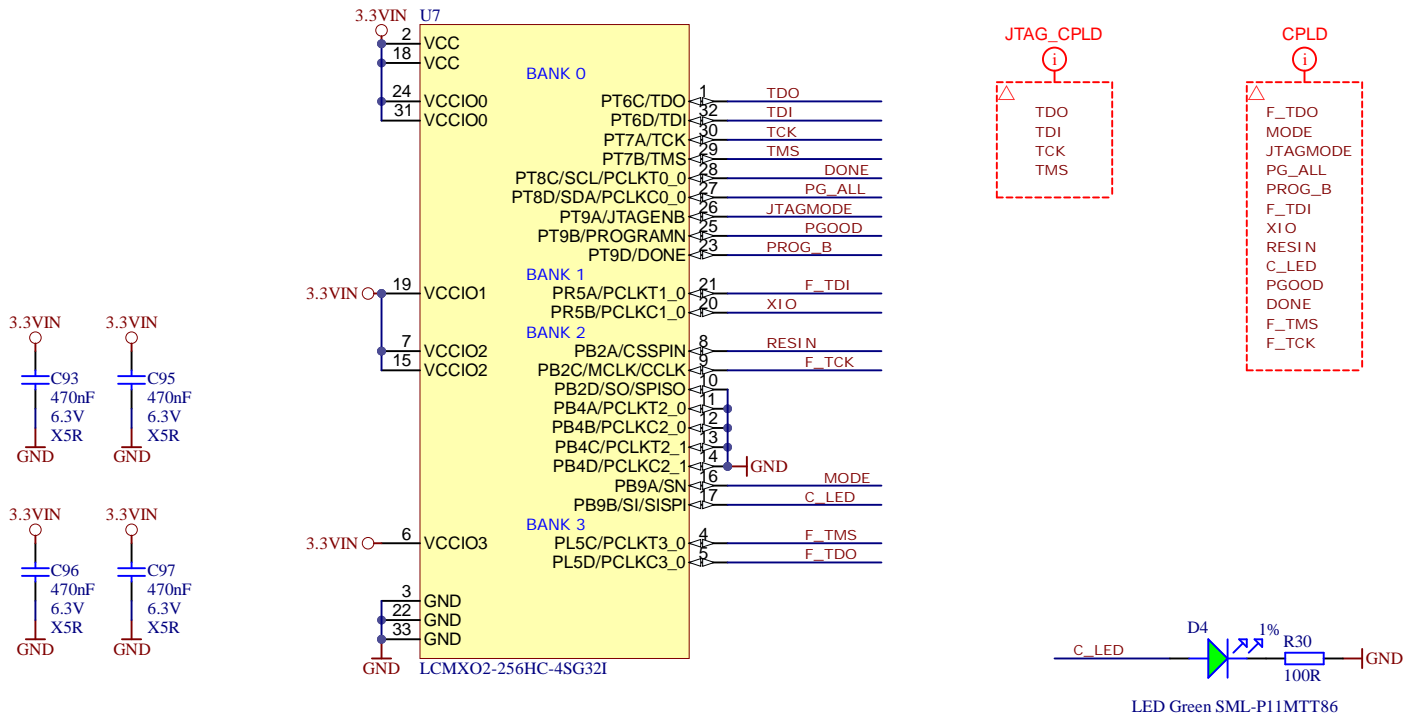
BOOTMODE = MASTER SPI => 0 0 1



Title: TE0741		
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	Title: TE0741	
	A4	Number: TE0741 070-2CF
	Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH
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Filename: FPGA-MISC.SchDoc		

1

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A

A

B

B

C

C

D

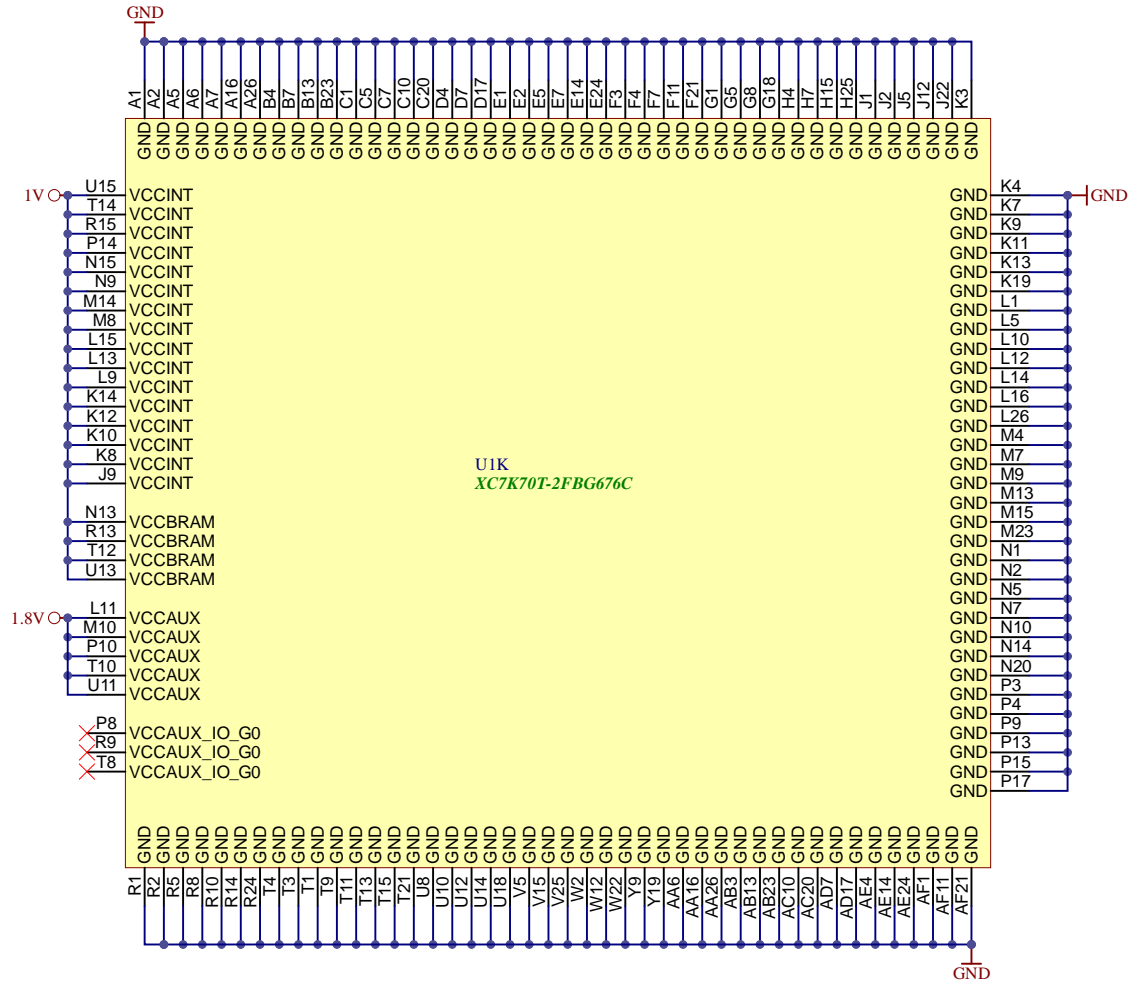
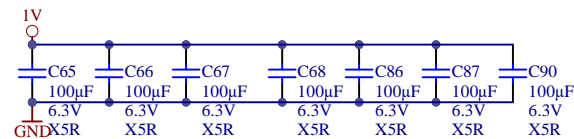
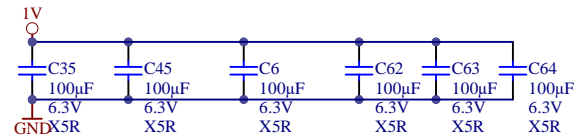
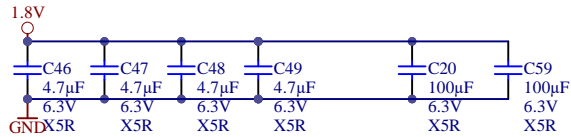
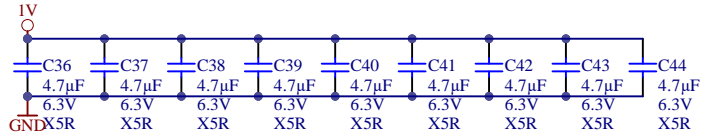
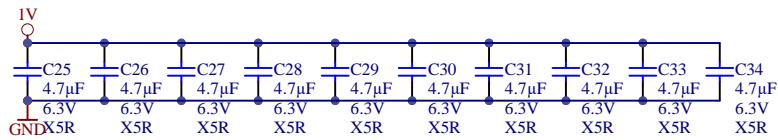
D

1

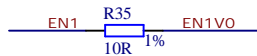
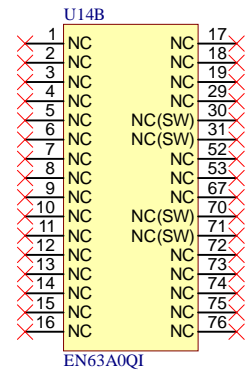
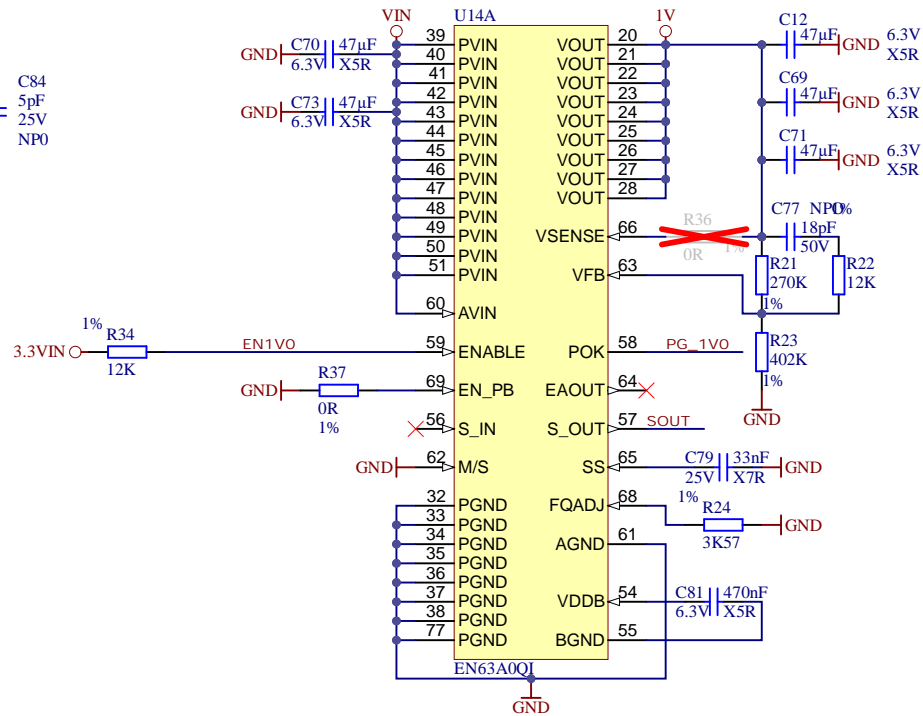
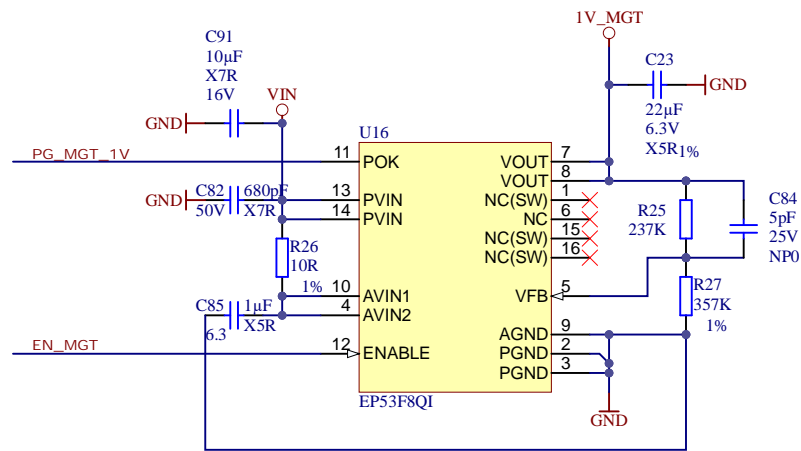
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3

4



Title: TE0741		
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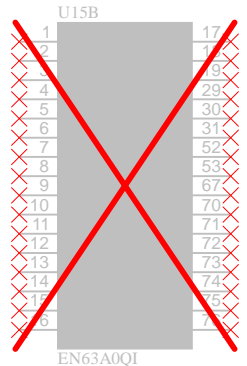
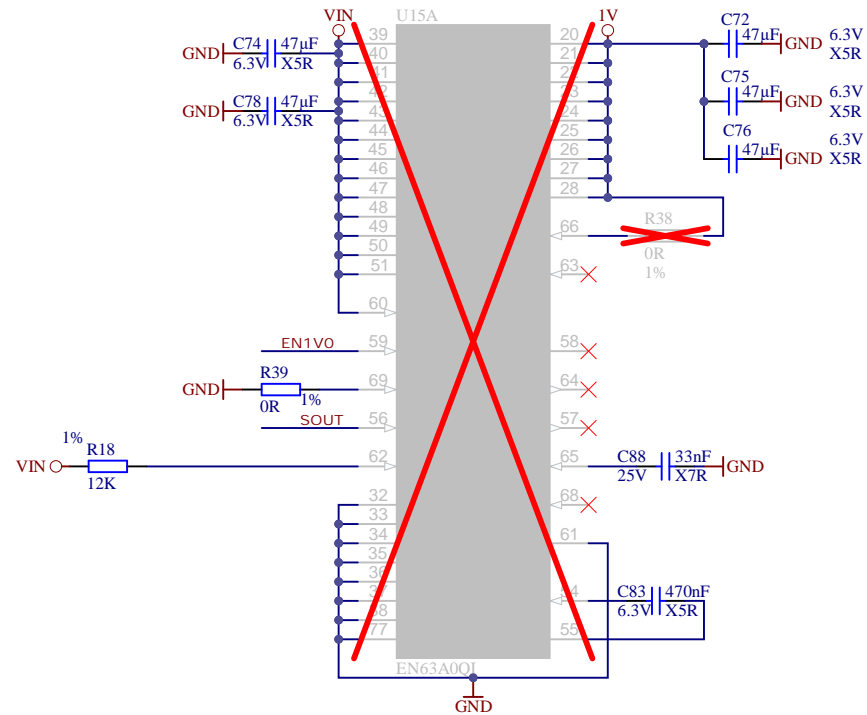
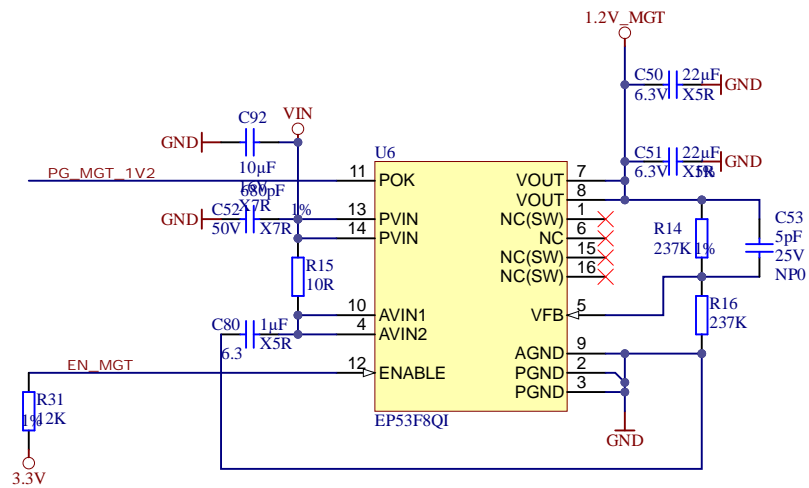
Not mount if baseboard EN1 circuit cause problems

Pre-bias feature is not available for parallel operations

R36 R37 MODE EN63A0QI

OK X | enable pre-bias start-up (available when U14 or U15 as DNP)
 X OK | disable pre-bias start-up

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Pre-bias feature is not available for parallel operations

R38 R39 MODE EN63A0QI

 OK X | enable pre-bias start-up (available when U14 or U15 as DNP)
 X OK | disable pre-bias start-up



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1

2

3

4

CHANGES REV02 to REV03

- 1) fixed connection DCDC for parallel operations
- 2) update Razorbeam Connectors, full update lib
- 3) added serial number (traceability pad)
- 4) changed ferrite beads L1..L4 size 0402 on BKP0603HS121-T
- 5) added thermal vias to mounting holes

A

A

B


B

C

C

D

D

	Title: TE0741 - Changes list		
	A4	Number: TE0741 070-2CF	Rev. 03
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	Filename: Revision_Changes.SchDoc		

1

2

3

4