Keywords: T1,E1,template

APPLICATION NOTE 3718

DS26528 and DS26524 Transmit Pulse Control

Dec 22, 2005

Abstract: With the addition of network protection components and/or the need to route signals through connectors and other PC board requirements, sometimes it is necessary to manipulate the transmit waveform. The DS26528 and DS26524 contain precise methods for making minor or major changes to the output pulse. This application note provides the information required to access factory test registers that allow the transmit waveform to be modified to meet a wide variety of application requirements.

T1 and E1 Transmit Waveform Programmable Sections

The DS26528 and DS26524 contain registers that provide control for the transmit pulse in two major areas: amplitude and timing. T1 and E1 transmit pulses are divided into sections, each of which may be manipulated to provide the desired waveform. **Figure 1** shows how the T1 pulse is divided and the registers that control each section. **Figure 2** provides the same information for the E1 pulse.

T1 and E1 Transmit Waveform Amplitude Control

The amplitude of the DS26528 and DS26524 transmit pulse may be controlled in two ways:

- **Adjusting the DAC Gain**
  The L1TXLAE register bits DAC[3:0] provide positive and negative adjustment of all the T1 or E1 levels simultaneously.
- **Partial Waveform Level Adjustment**
  The WLA[3:0] bits of the Level Adjustment registers provide fine tuning of specific sections of the waveform. The step size of the voltage level will change in proportion to the programmed DAC gain. If the DAC gain is increased by 10%, then the step sizes will also increase by 10%.

T1 and E1 Transmit Waveform Timing Control

The timing of the DS26528 and DS26524 transmit pulse levels are controlled by the CEA[2:0] bits of the Level Adjustment registers. Each edge may be moved in both positive and negative directions in increments of 1/32 of TCLK.

General Recommendations

Modifying the DAC gain is the easiest method of controlling the amplitude of the transmit pulse, because it will control the entire waveform with only one register change. Using the DAC gain first will allow for minimal, if any, modifications of the individual Level Adjustment registers.

The maximum output of the DAC will be affected by V_{DD}. At lower levels of V_{DD}, the maximum DAC gain setting may be unattainable. Changing V will also affect the maximum voltage attainable by the

DD

line driver's output stage.

Negative values do not use signed integer representation. The MSB is the sign bit and the LSBs represent magnitude irrespective of sign. For example, a -3 in a WLA[3:0] register would be 1011b (bit 3 set to 1 means negative, 011 in the next 3 bits is magnitude 3), not 1101b (4-bit signed integer representation).

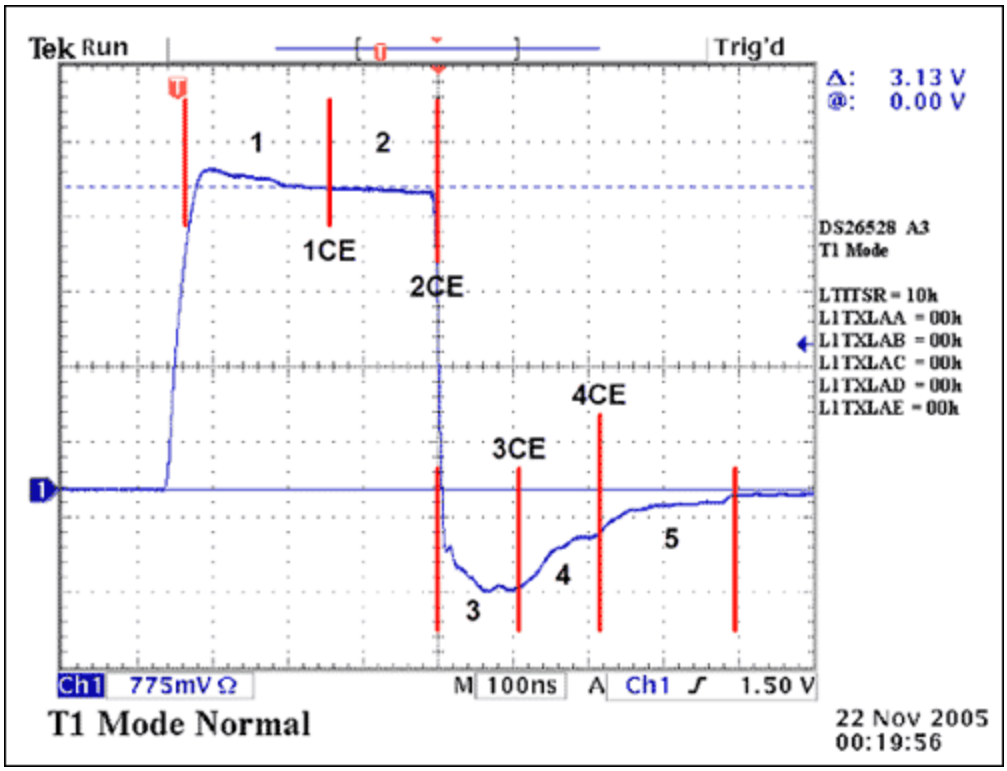


Figure 1. T1 Pulse control sections.

T1 Pulse Control Sections

- Overshoot (1) -- Register L1TXLAA WLA[4:0]
- Clock Edge (1CE) -- Register L1TXLAA CEA[2:0]
  (1CE) = Clock Edge transition from Overshoot to Plateau
- Plateau (2) -- Register L1TXLAB WLA[4:0]
- Clock Edge (2CE) -- Register L1TXLAB CEA[2:0]
  (2CE) = Clock Edge transition from Plateau to Falling Edge
- Undershoot (3) -- Register L1TXLAC WLA[4:0]
- Clock Edge (3CE) -- Register L1TXLAC CEA[2:0]
  (3CE) = Clock Edge transition from Falling Edge to End of Undershoot (3)
- Undershoot (4) -- Register L1TXLAD WLA[4:0]
- Clock Edge (4CE) -- Register L1TXLAD CEA[2:0]
  (4CE) = Clock Edge transition from End of Undershoot (3) to End of Undershoot (4)
- Undershoot (5) -- Register L1TXLAC WLA[4:0]

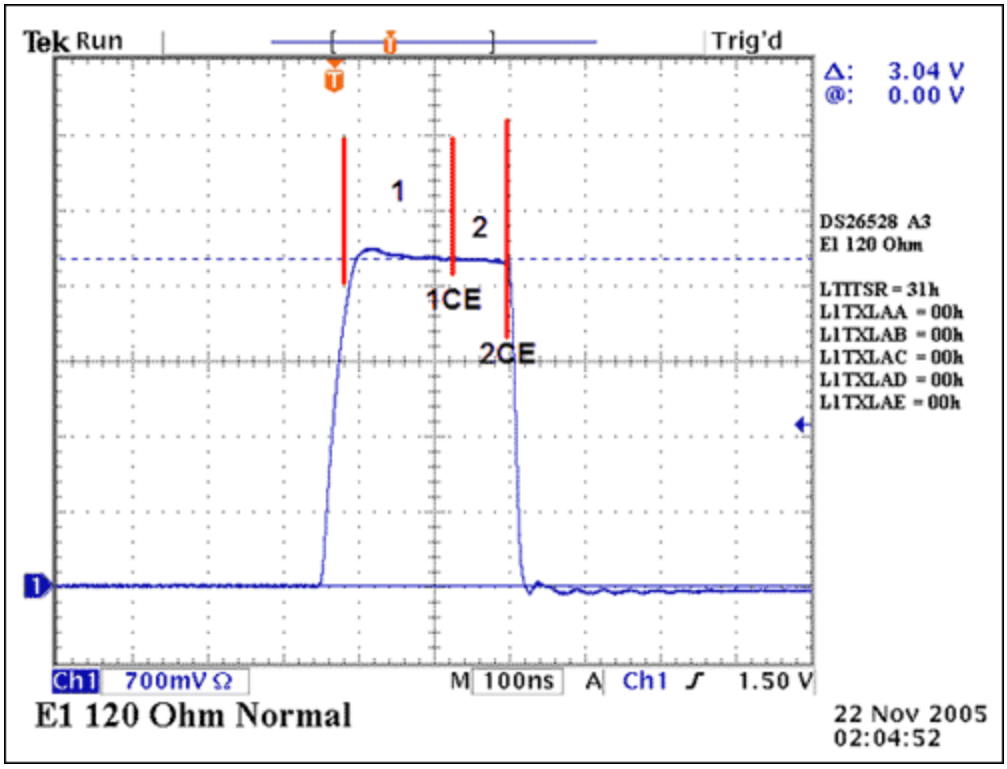


Figure 2. E1 Pulse control sections.

E1 Pulse Control Sections

- Overshoot (1) -- Register L1TXLAA WLA[4:0]
- Clock Edge (1CE) -- Register L1TXLAA CEA[2:0]
  (1CE) = Clock Edge transition from Overshoot to Plateau
- Plateau (2) -- Register L1TXLAB WLA[4:0]
- Clock Edge (2CE) -- Register L1TXLAB CEA[2:0]
  (2CE) = Clock Edge transition from Plateau to Falling Edge

NOTE:

Registers L1TXAC, L1TXAD, and L1TXAE are not used in E1 mode.

LIU Test Register Descriptions for the DS26528 and DS26524

Table 1 provides the register address and description for LIU 1. These registers are duplicated for LIUs 2 through 8. **Table 2** provides the addresses for all of the LIU test registers. The DS26524 does not contain LIU 5 through 8.

Table 1. LIU 1 Test Registers

Address	Abbr	Description
1008h	L1TXLAA	LIU 1 Tx Level Adjust A (Test Register)
1009h	L1TXLAB	LIU 1 Tx Level Adjust B (Test Register)
100Ah	L1TXLAC	LIU 1 Tx Level Adjust C (Test Register)
100Bh	L1TXLAD	LIU 1 Tx Level Adjust D (Test Register)

100Ch	L1TXLAE	LIU 1 Tx Level Adjust E (Test Register)

Table 2. LIU Test Register Address Range

LIU	Address Range
1	1008 - 100Ch
2	1028 - 102Ch
3	1048 - 104Ch
4	1068 - 106Ch
DS26528 Only	
5	1080 - 108Ch
6	10A8 - 10ACh
7	10C8 - 10DCh
8	10E8 - 10ECh

Detailed LIU Test Register Documentation

The following provides the register address and description for LIU 1. These registers are duplicated for LIUs 2 through 8. See Table 2 for the addresses for all of the LIU test registers.

Register Name:	**L1TXLAA**
Register Description:	**LIU Tx Level Adjust A (Overshoot Voltage)**
Register Address:	**1008H**
Read/Write Function:	**R/W**

Bit #	7	6	5	4	3	2	1	0
Name	WLA4	WLA3	WLA2	WLA1	WLA0	CEA2	CEA1	CEA0
Default	0	0	0	0	0	0	0	0

Bits 7 to 3: Transmit Waveform Levels Adjust for Output Level 1 (WLA[4:0]). Moves magnitude from default ±360mV.

Bit 7 = sign bit ('1' means negative)
Bits 6 to 3 = magnitude (unsigned)
i.e., 24mV is LSB step size

Bits 2 to 0: Clock Edge Adjust (CEA[2:0]). Moves clock edge ±3 32x-clks from default.

<2> = sign bit ('1' means negative)
<1:0> = number of 32x-clks to move (unsigned)

Register Name:	**L1TXLAB**
Register Description:	**LIU Tx Level Adjust B (Plateau Voltage)**
Register Address:	**1009H**
Read/Write Function:	**R/W**

Bit #	7	6	5	4	3	2	1	0
Name	WLA4	WLA3	WLA2	WLA1	WLA0	CEA2	CEA1	CEA0
Default	0	0	0	0	0	0	0	0

Bits 7 to 3: Transmit Waveform Levels Adjust for Output Level 2 (WLA[4:0]). Moves magnitude from default ±360mV.

Bit 7 = sign bit ('1' means negative)
Bits 6 to 3 = magnitude (unsigned)
i.e., 24mV is LSB step size

Bits 2 to 0: Clock Edge Adjust (CEA[2:0]). Moves clock edge ±3 32x-clks from default.

<2> = sign bit ('1' means negative)
<1:0> = number of 32x-clks to move (unsigned)

Register Name:	**L1TXLAC**
Register Description:	**LIU Tx Level Adjust C (Undershoot Voltage #1)**
Register Address:	**100AH**
Read/Write Function:	**R/W**

Bit #	7	6	5	4	3	2	1	0
Name	WLA4	WLA3	WLA2	WLA1	WLA0	CEA2	CEA1	CEA0
Default	0	0	0	0	0	0	0	0

Bits 7 to 3: Transmit Waveform Levels Adjust for Output Level 3 (WLA[4:0]). Moves magnitude from default ±360mV.

Bit 7 = sign bit ('1' means negative)
Bits 6 to 3 = magnitude (unsigned)
i.e., 24mV is LSB step size

Bits 2 to 0: Clock Edge Adjust (CEA[2:0]). Moves clock edge ±3 32x-clks from default.

<2> = sign bit ('1' means negative)
<1:0> = number of 32x-clks to move (unsigned)

Register Name:	**L1TXLAD**
Register Description:	**LIU Tx Level Adjust D (Undershoot Voltage #2)**
Register Address:	**100BH**
Read/Write Function:	**R/W**

Bit #	7	6	5	4	3	2	1	0
Name	WLA4	WLA3	WLA2	WLA1	WLA0	CEA2	CEA1	CEA0

Default	0	0	0	0	0	0	0	0

Bits 7 to 3: Transmit Waveform Levels Adjust for Output Level 4 (WLA[4:0]). Moves magnitude from default ±360mV.

Bit 7 = sign bit ('1' means negative)
Bits 6 to 3 = magnitude (unsigned)
i.e., 24mV is LSB step size

Bits 2 to 0: Clock Edge Adjust (CEA[2:0]). Moves clock edge ±3 32x-clks from default.

<2> = sign bit ('1' means negative)
<1:0> = number of 32x-clks to move (unsigned)

Register Name:	**L1TXLAE**
Register Description:	**LIU Tx Level Adjust E (Undershoot Voltage #3)**
Register Address:	**100CH**
Read/Write Function:	**R/W**

Bit #	7	6	5	4	3	2	1	0
Name	WLA4	WLA3	WLA2	WLA1	WLA0	CEA2	CEA1	CEA0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Transmit Waveform Levels Adjust for Output Level 5 (WLA[3:0]). Moves magnitude from default ±180mV.

Bit 7 = sign bit ('1' means negative)
Bits 6 to 4 = magnitude (unsigned)
i.e., 24mV is LSB step size

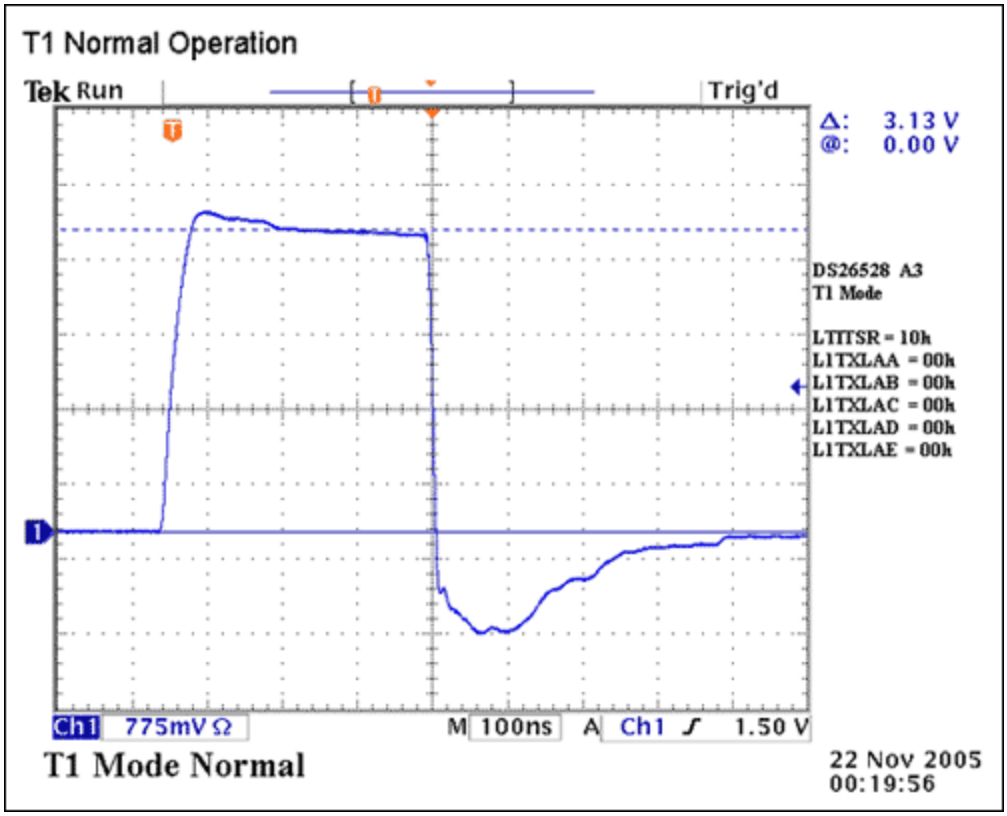
Bits 3 to 0: DAC Gain Adjust (DAC[3:0]). The following settings change the gain of the DAC.

0000 - nominal DAC gain (default)
0001 - DAC gain +2.6%
0010 - DAC gain +5.3%
0011 - DAC gain +8%
0100 - DAC gain +11.1%
0101 - DAC gain +14.2%
0110 - DAC gain +17.7%
0111 - DAC gain +21.3%
1000 - DAC gain -2.2%
1001 - DAC gain -4.88%
1010 - DAC gain -7.11%
1011 - DAC gain -8.88%
1100 - DAC gain -11.11%

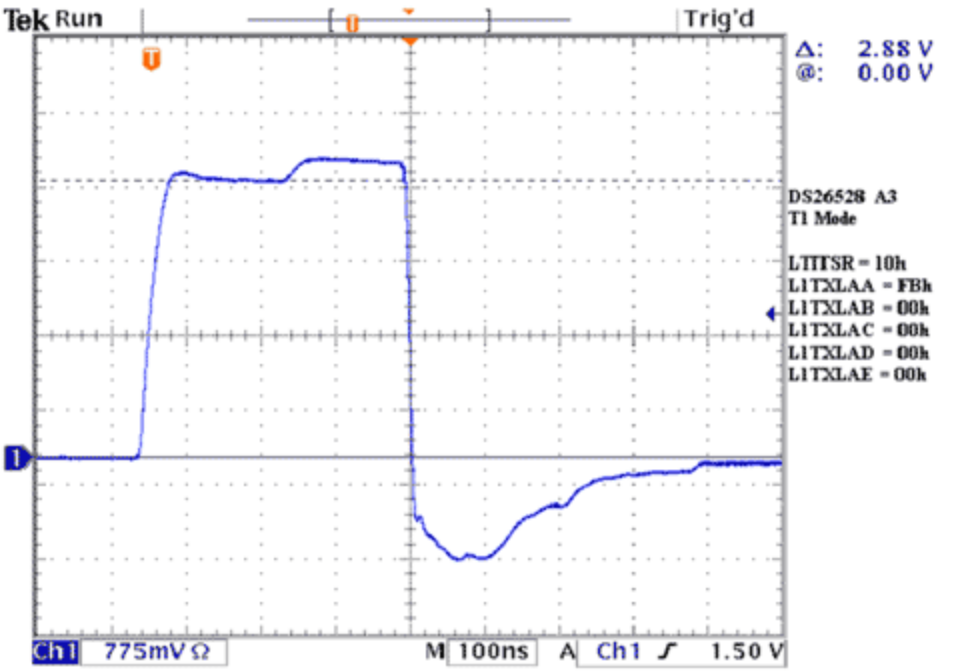
1101 - DAC gain -12%
1110 - DAC gain -15.1%
1111 - DAC gain -16.4%

T1 and E1 Transmit Waveform Data

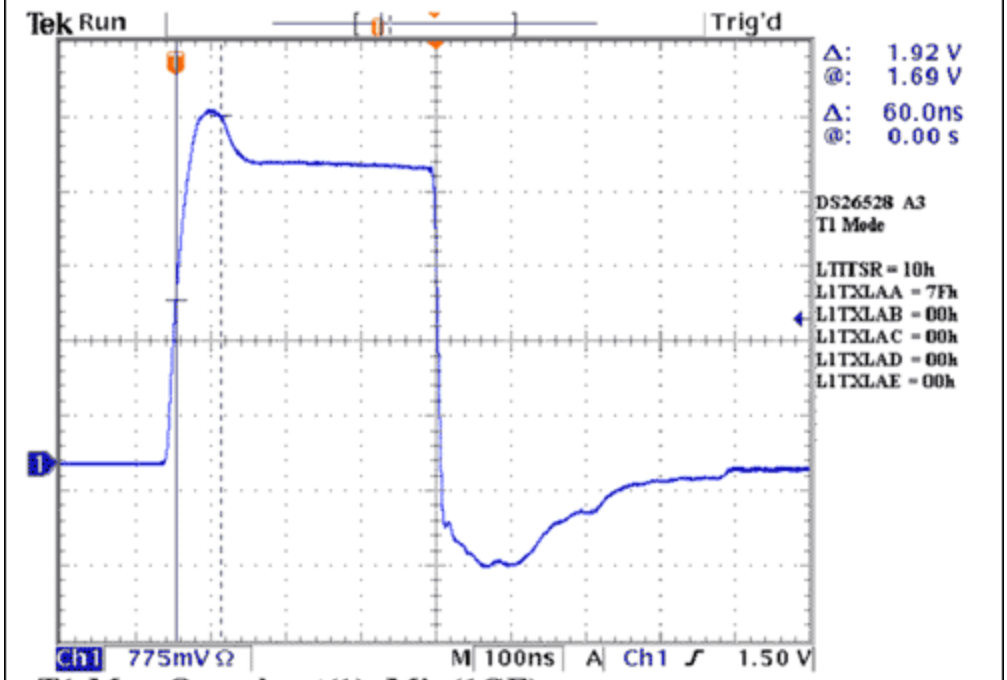
The following data is representative of the expected results for both the DS26528 and DS26524. The data is provided as a guideline for determining the range and method of using the Level Adjustment registers for controlling the amplitude and timing of the T1 and E1 transmit pulses. The data was taken at room temperature with 3.3V V_{DD}.



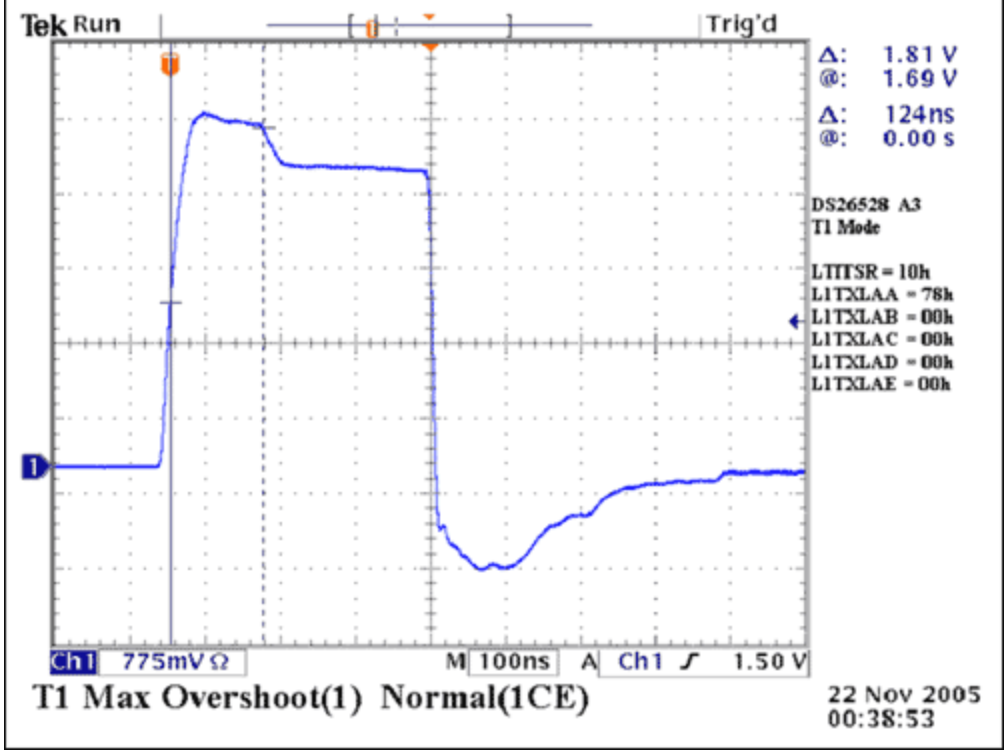
T1 Mode
Min Overshoot (1) = 2.88V
Max Clock Edge (1CE) = 178nS



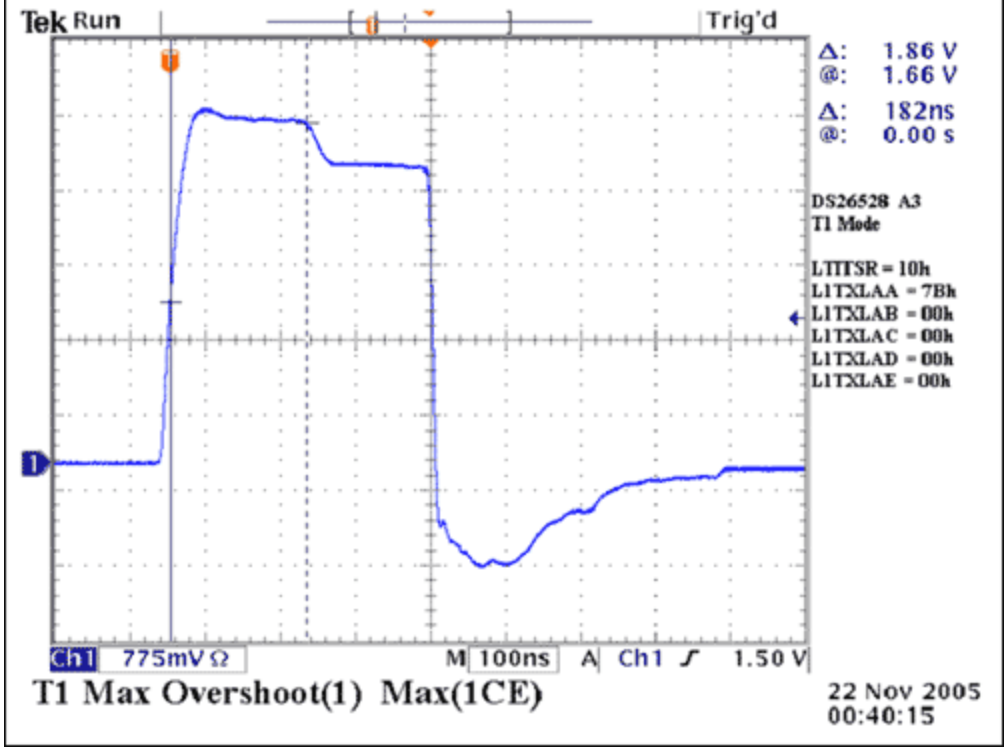
T1 Mode
Max Overshoot (1) = 3.64V
Min Clock Edge (1CE) = 60nS



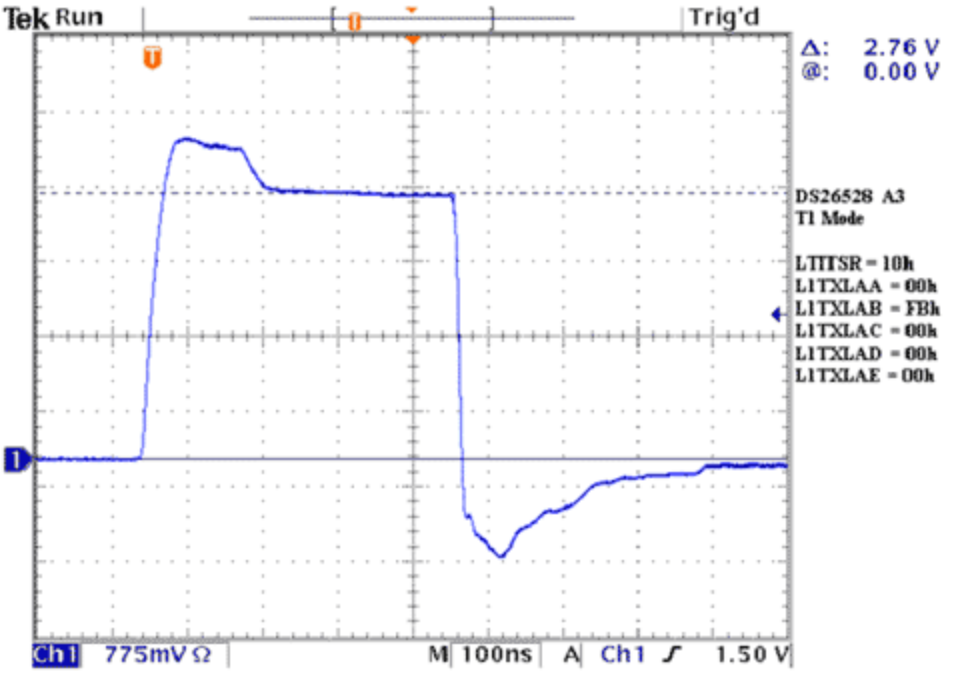
T1 Mode
Max Overshoot (1) = 3.64V
Normal Clock Edge (1CE) = 124nS



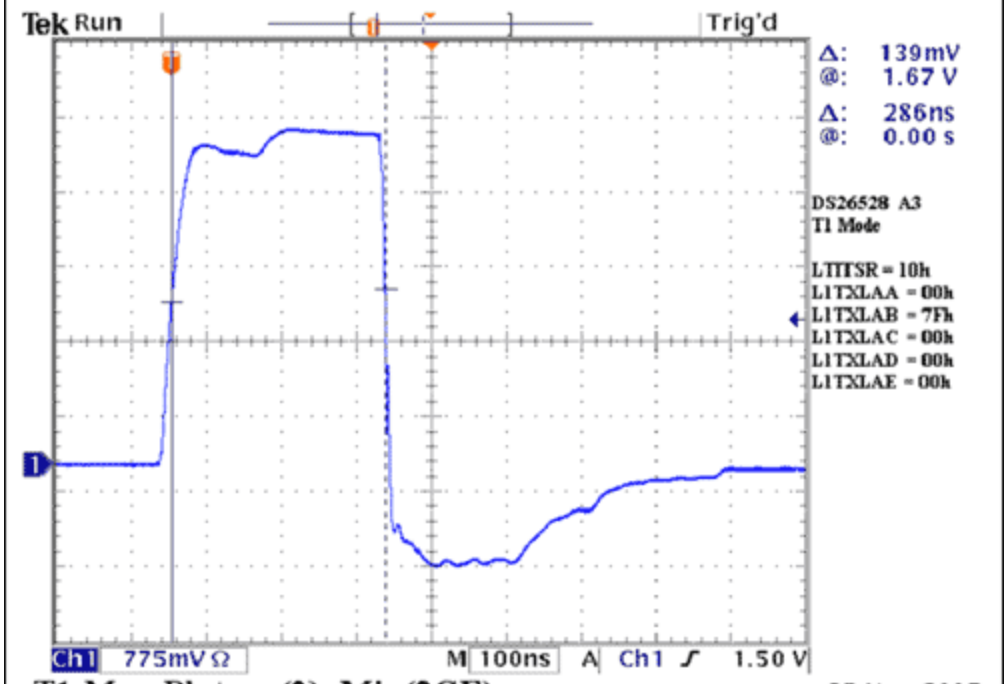
T1 Mode
Max Overshoot (1) = 3.64V
Max Clock Edge (1CE) = 182nS



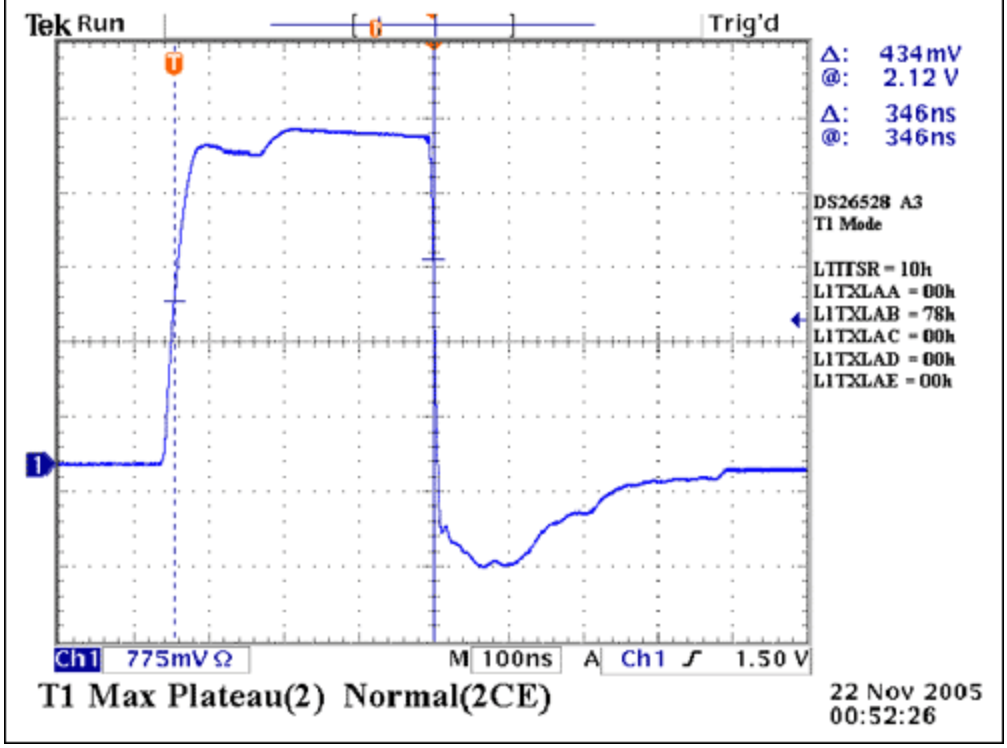
T1 Mode
Min Plateau (2) = 2.76V
Max Clock Edge (2CE) = 406nS



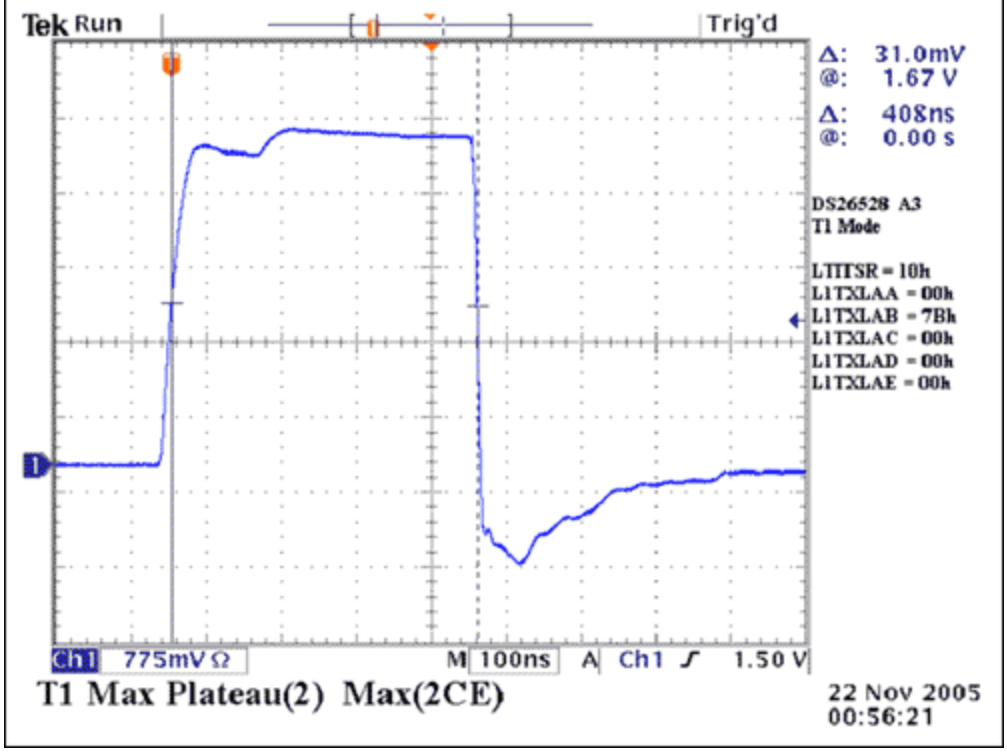
T1 Mode
Max Plateau (2) = 3.43V
Min Clock Edge (2CE) = 286nS



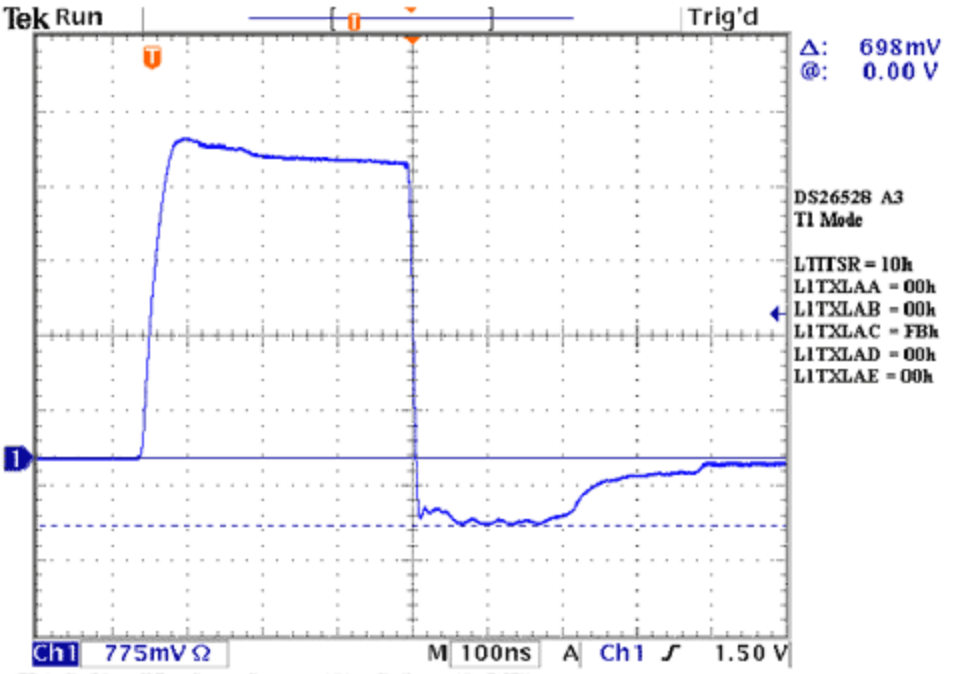
T1 Mode
Max Plateau (2) = 3.43V
Normal Clock Edge (2CE) = 346nS



T1 Mode
Max Plateau (2) = 3.43V
Max Clock Edge (2CE) = 408nS



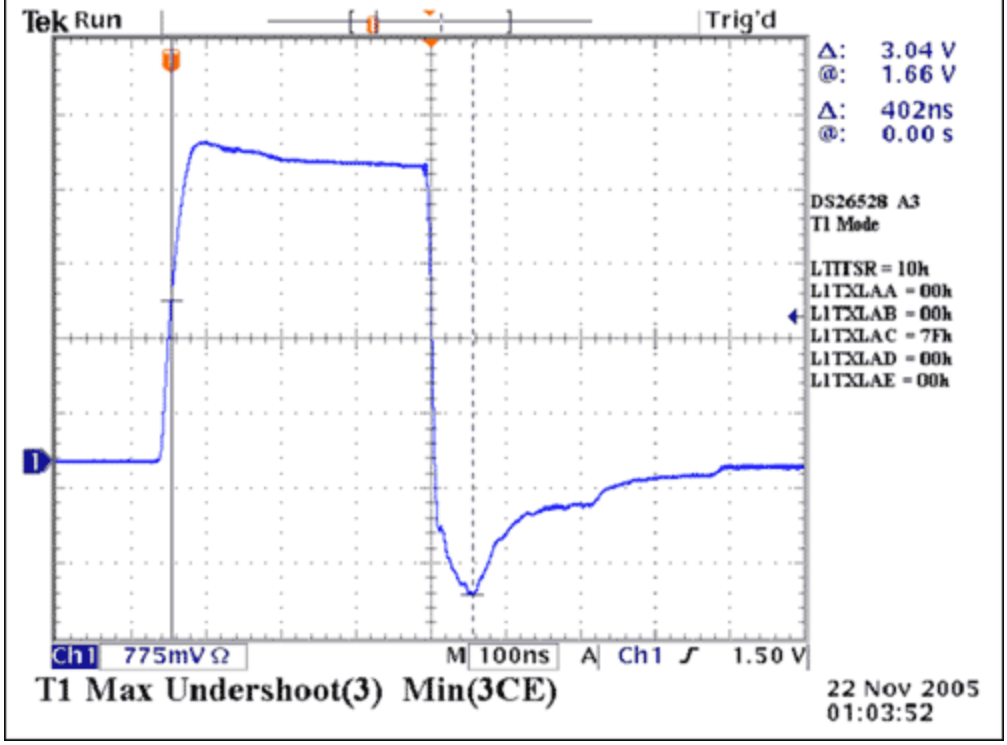
T1 Mode
Min Undershoot (3) = -698mV
Max Clock Edge (3CE) = 554nS



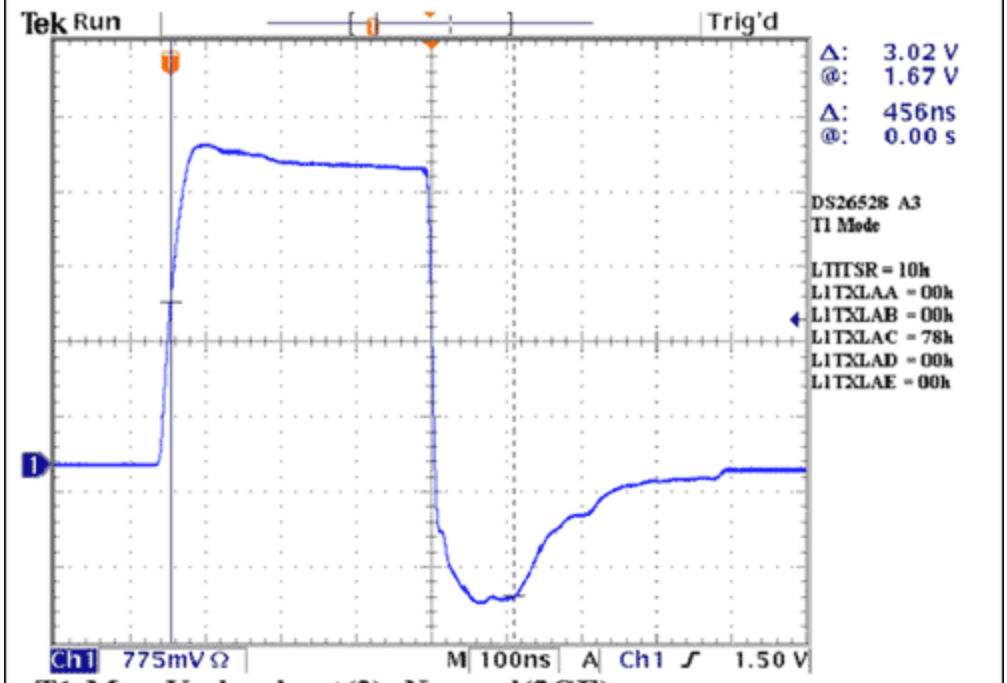
T1 Min Undershoot(3) Max(3CE)

22 Nov 2005
00:59:51

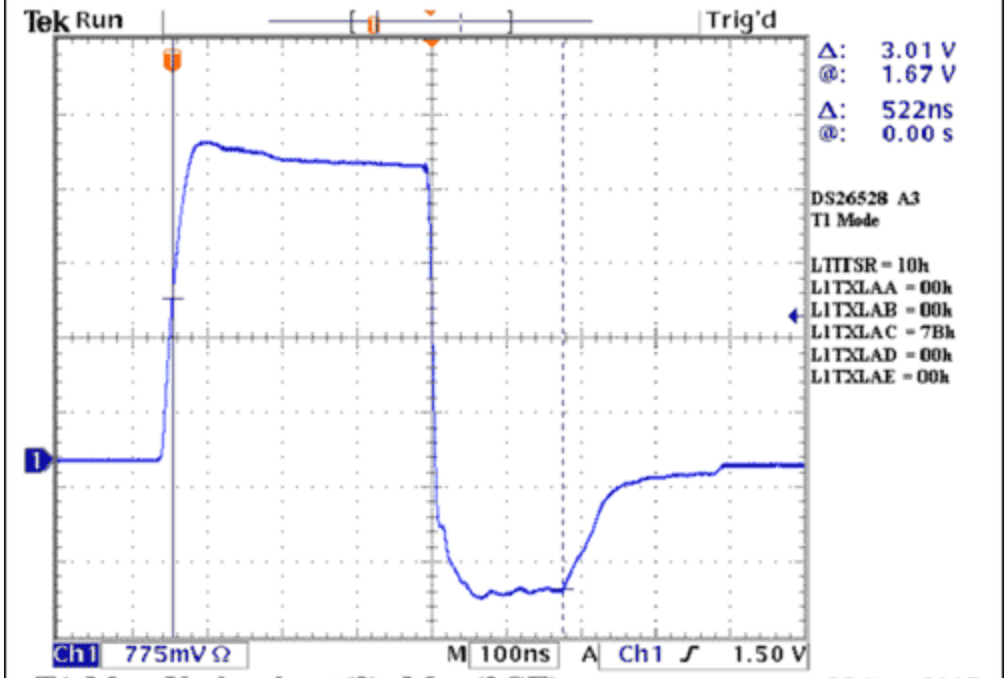
T1 Mode
Max Undershoot (3) = -1.38V
Min Clock Edge (3CE) = 402nS



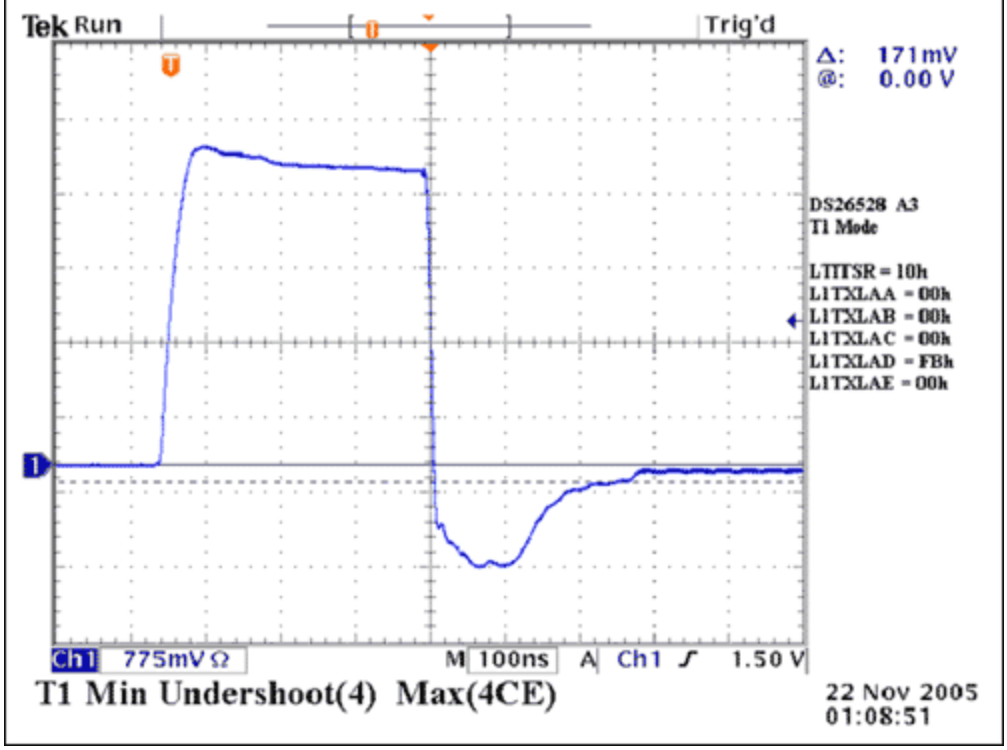
T1 Mode
Max Undershoot (3) = -1.38mV
Normal Clock Edge (3CE) = 456nS

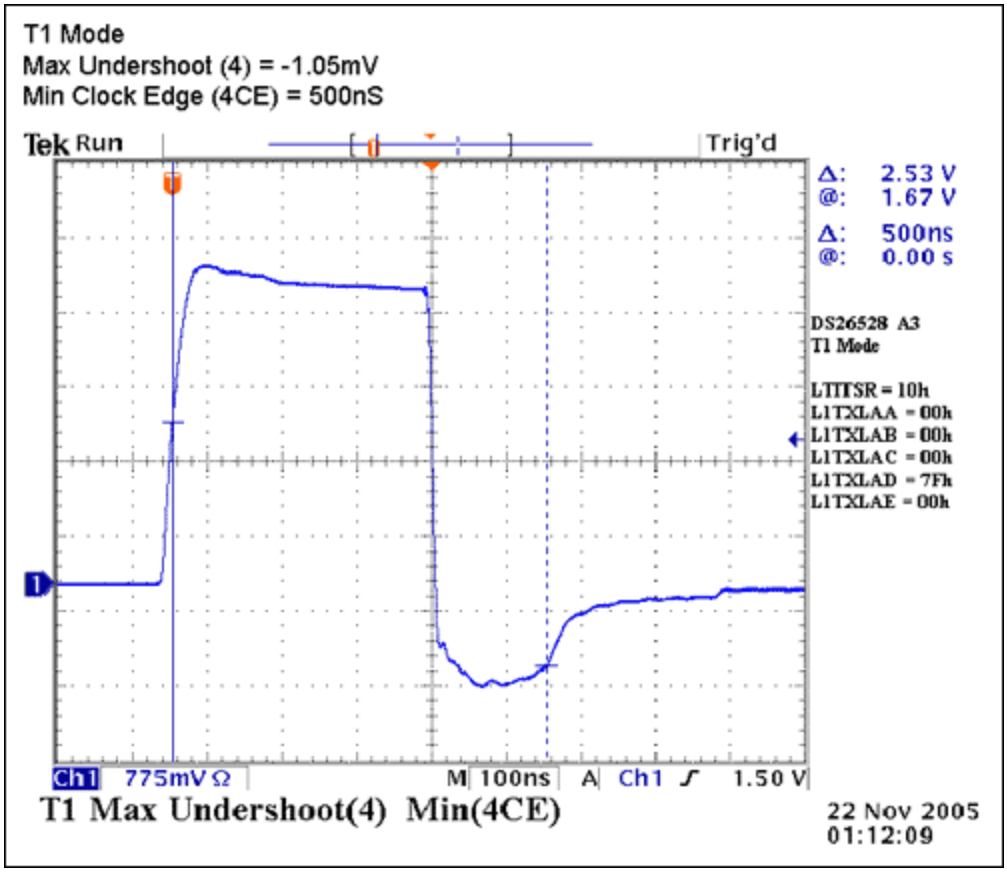


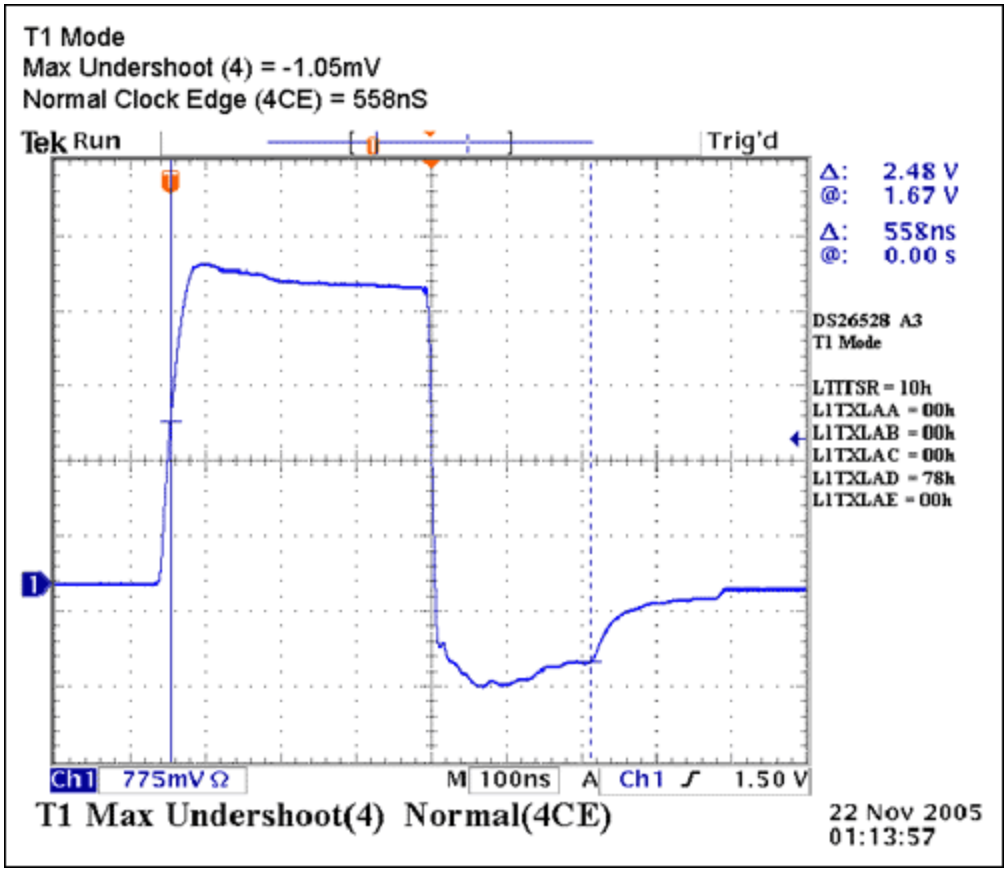
T1 Mode
Max Undershoot (3) = -1.38V
Max Clock Edge (3CE) = 522nS



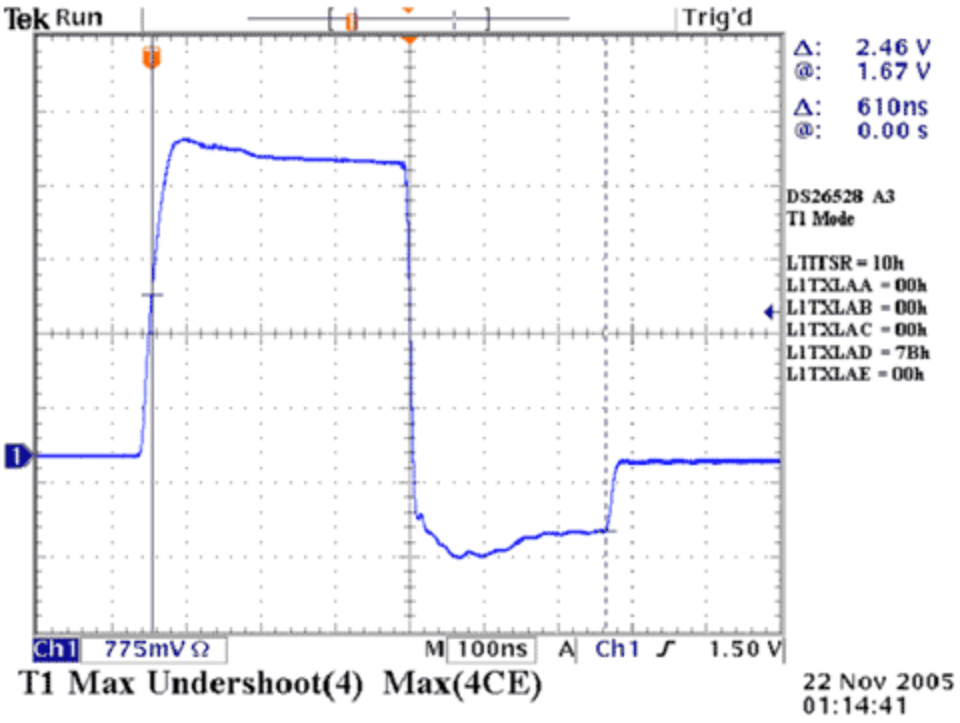
T1 Mode
Min Undershoot (4) = -171mV
Max Clock Edge (4CE) = 610nS

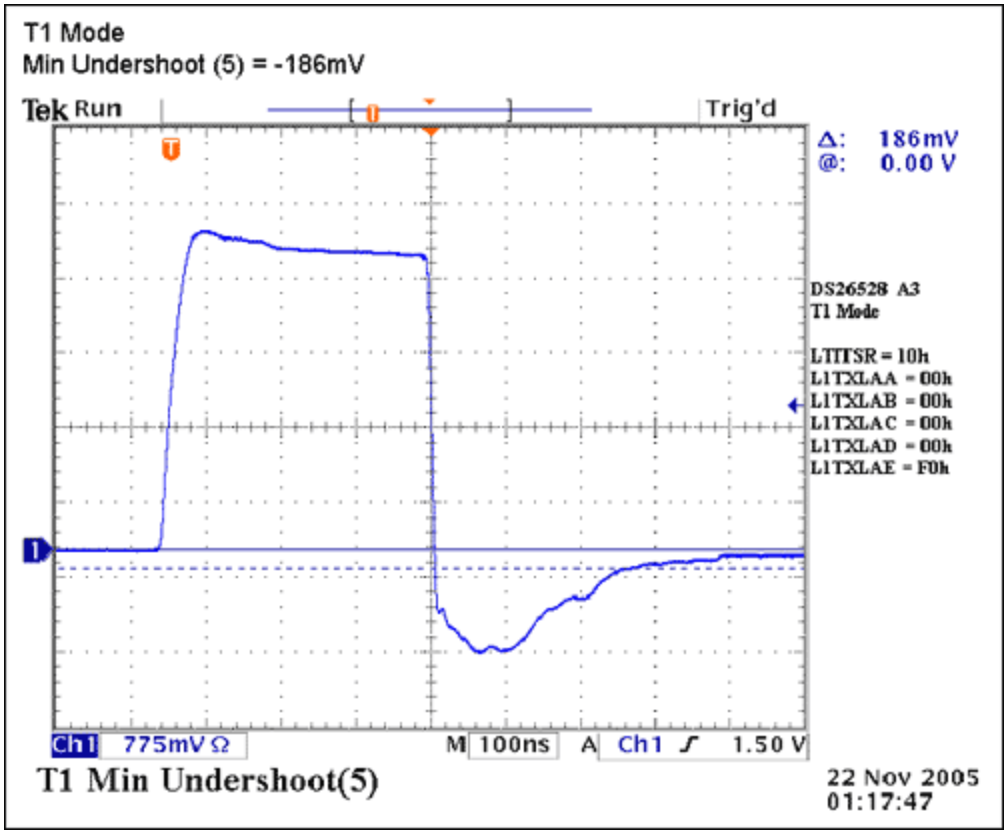



T1 Mode
Max Undershoot (4) = -1.05mV
Min Clock Edge (4CE) = 500nS
Tek Run
Trig'd
Δ: 2.53 V
@: 1.67 V
Δ: 500ns
@: 0.00 s
DS26528 A3
T1 Mode
LTITSR = 10h
L1TXLAA = 00h
L1TXLAB = 00h
L1TXLAC = 00h
L1TXLAD = 7Fh
L1TXLAE = 00h
Ch1 775mV Ω
M 100ns A Ch1 1.50 V
T1 Max Undershoot(4) Min(4CE)
22 Nov 2005
01:12:09

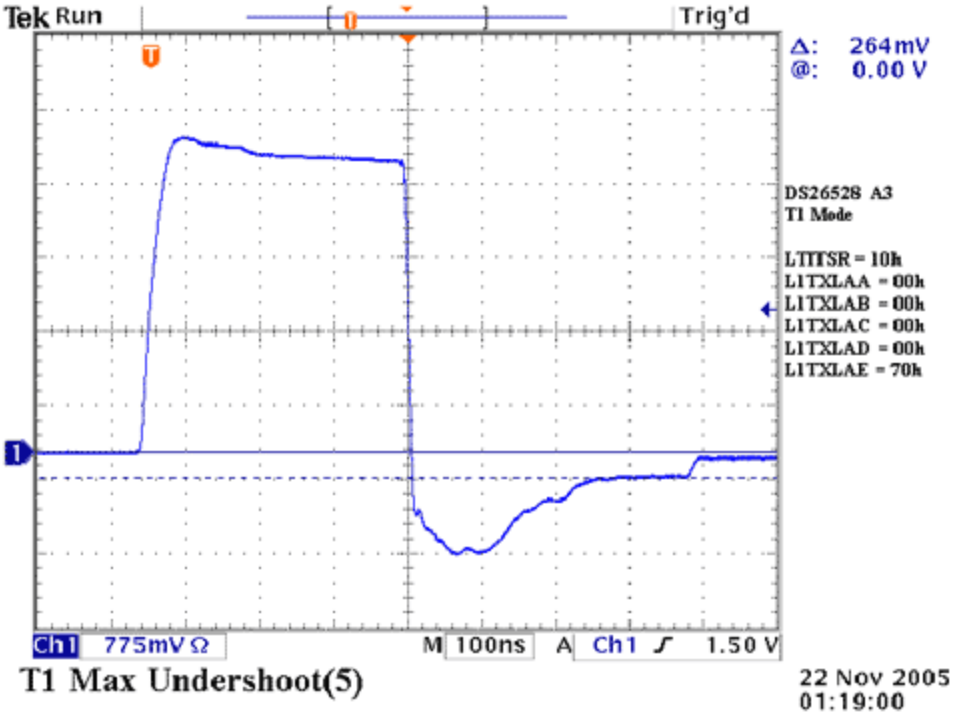

T1 Mode
Max Undershoot (4) = -1.05mV
Normal Clock Edge (4CE) = 558nS
Tek Run
Trig'd
Δ: 2.48 V
@: 1.67 V
Δ: 558ns
@: 0.00 s
DS26528 A3
T1 Mode
LIITSR = 10h
L1TXLAA = 00h
L1TXLAB = 00h
L1TXLAC = 00h
L1TXLAD = 78h
L1TXLAE = 00h
Ch1 775mV Ω
M 100ns A Ch1 1.50 V
T1 Max Undershoot(4) Normal(4CE)
22 Nov 2005
01:13:57

T1 Mode
Max Undershoot (4) = -1.05mV
Max Clock Edge (4CE) = 610nS



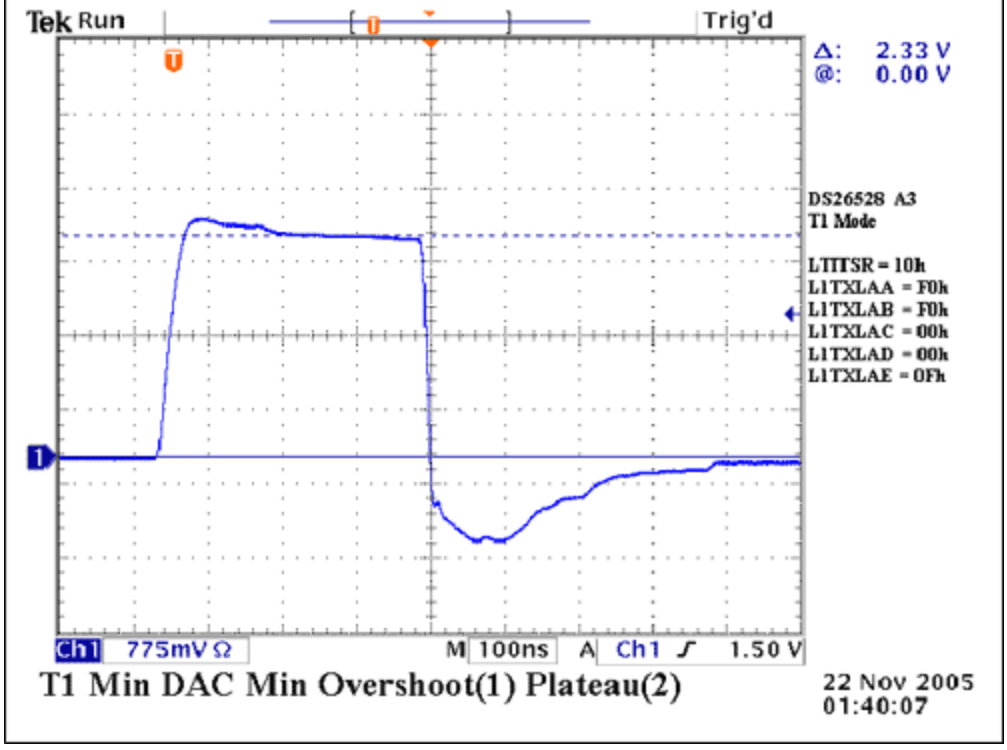

T1 Mode
Min Undershoot (5) = -186mV
Tek Run
Trig'd
Δ: 186mV
@: 0.00 V
DS26528 A3
T1 Mode
LTITSR = 10h
L1TXLAA = 00h
L1TXLAB = 00h
L1TXLAC = 00h
L1TXLAD = 00h
L1TXLAE = F0h
Ch1 775mV Ω
M 100ns A Ch1 1.50 V
T1 Min Undershoot(5)
22 Nov 2005
01:17:47

T1 Mode
Max Undershoot (5) = -264V

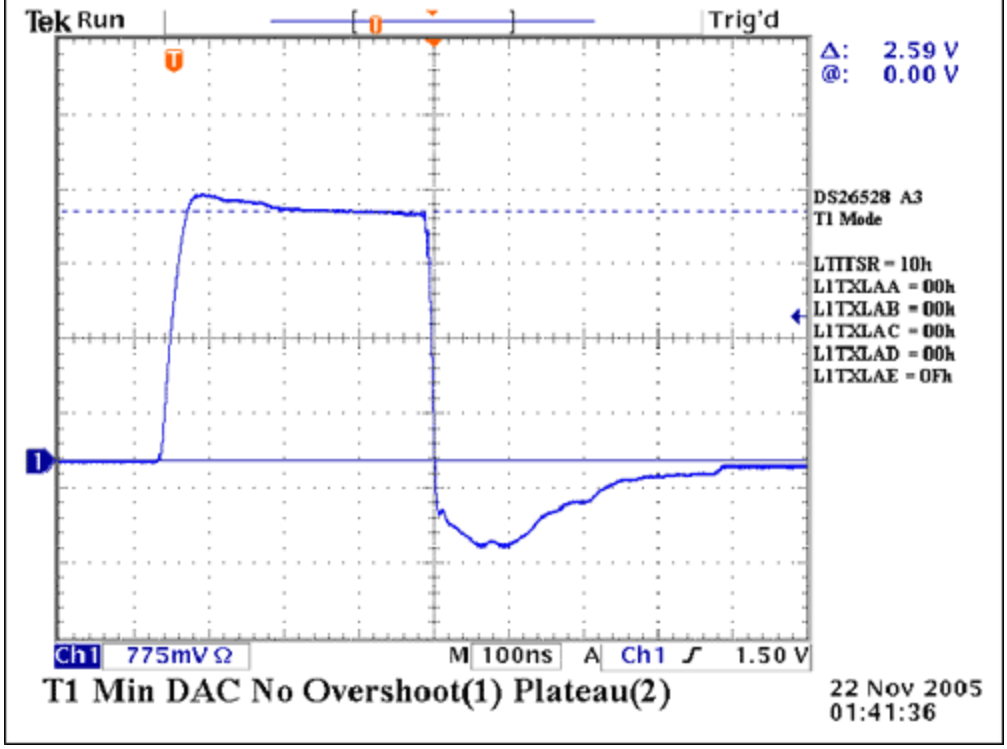


T1 Max Undershoot(5)

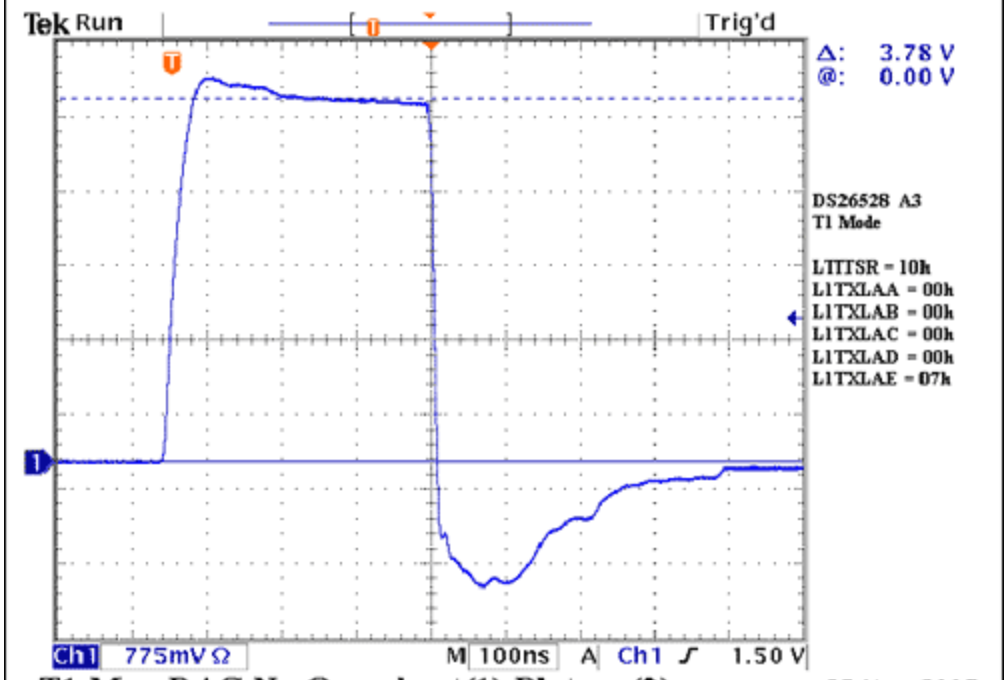
T1 Mode
Entire Pulse
Min DAC Level
Min Overshoot (1), Plateau (2)



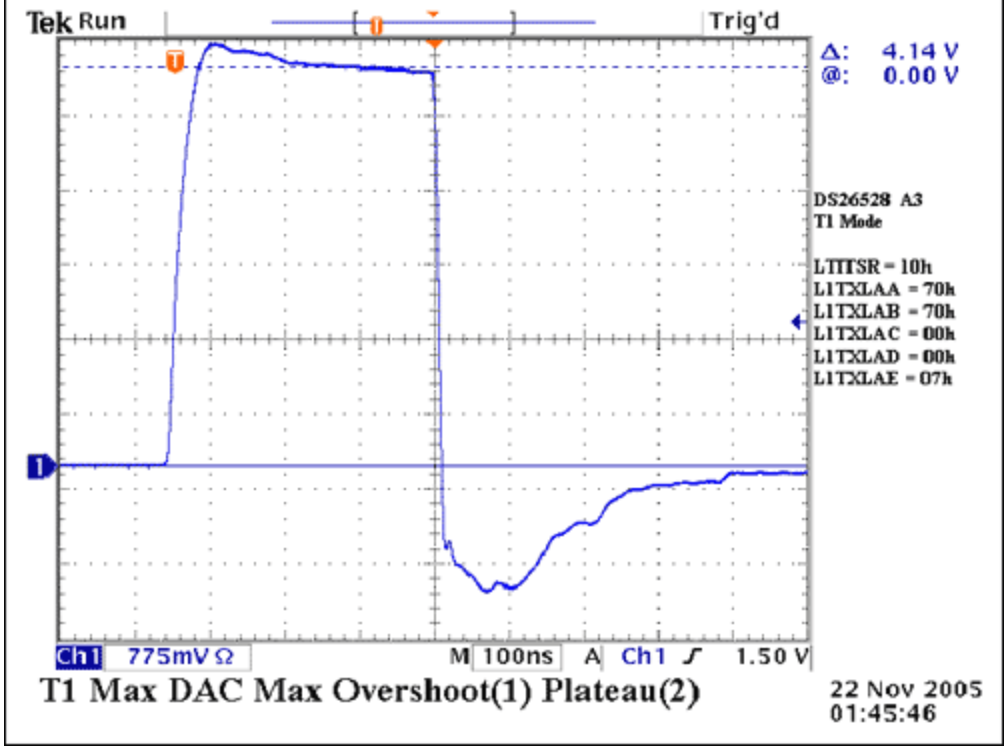
T1 Mode
Entire Pulse
Min DAC Level
No Overshoot (1), Plateau (2)

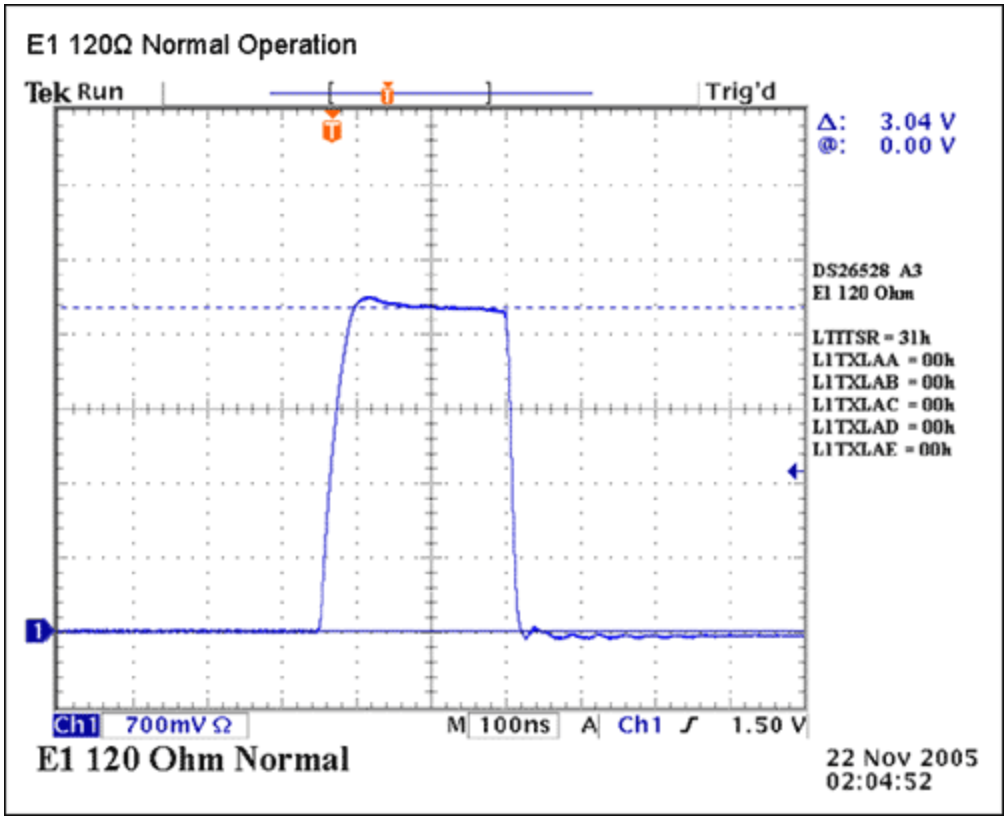


T1 Mode
Entire Pulse
Max DAC Level
No Overshoot (1), Plateau (2)

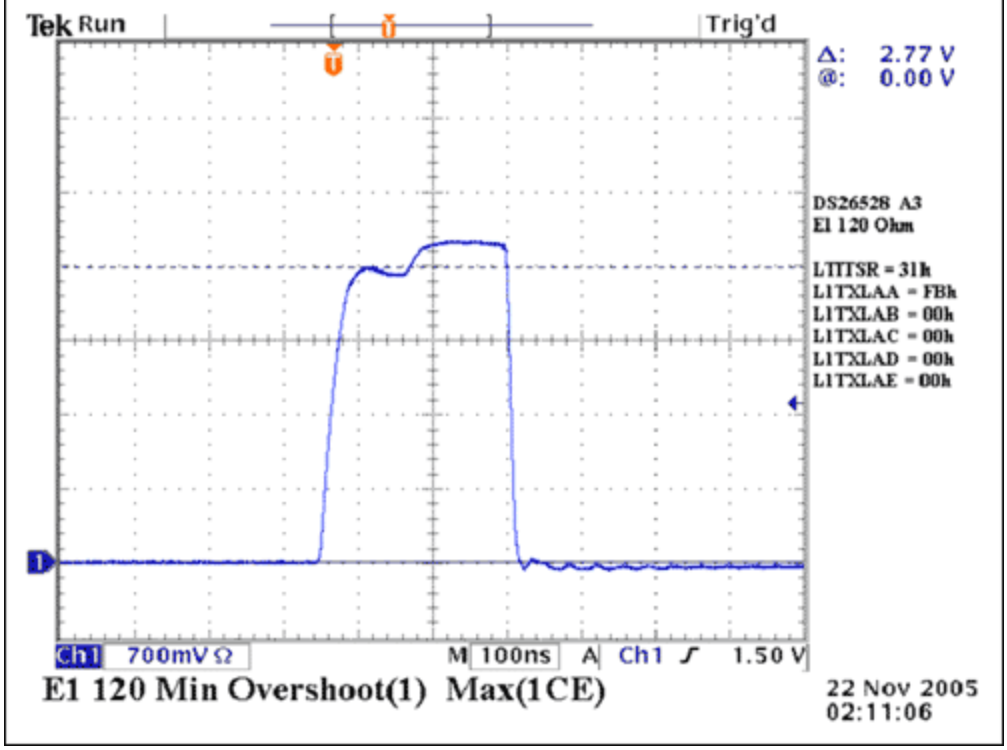


T1 Mode
Entire Pulse
Max DAC Level
Max Overshoot (1), Plateau (2)

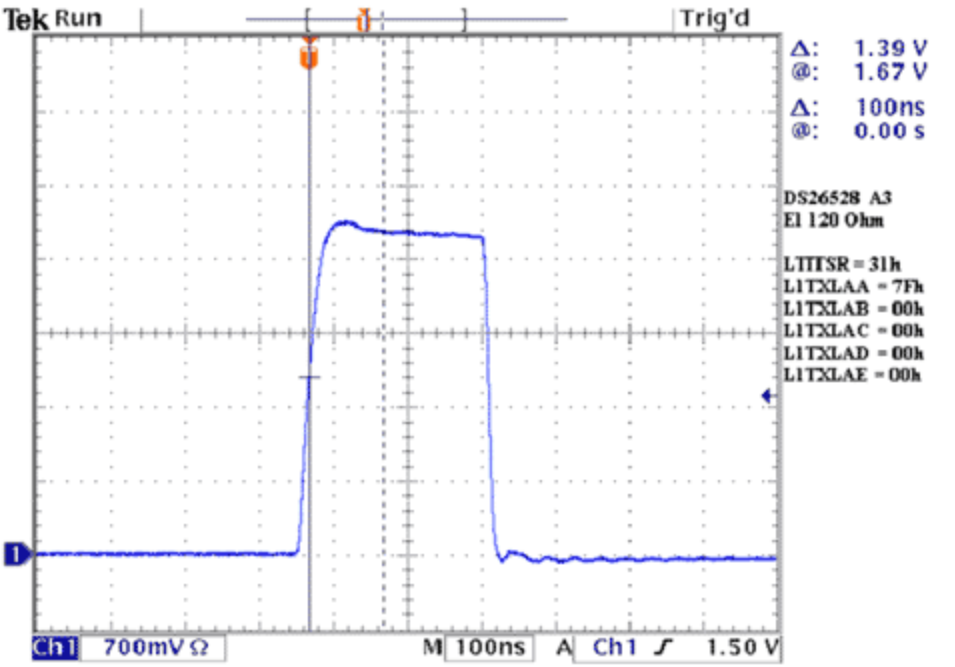



E1 120Ω Normal Operation
Tek Run
Trig'd
Δ: 3.04 V
@: 0.00 V
DS26528 A3
E1 120 Ohm
LTITSR = 31h
L1TXLAA = 00h
L1TXLAB = 00h
L1TXLAC = 00h
L1TXLAD = 00h
L1TXLAE = 00h
Ch1 700mV Ω
M 100ns A Ch1 1.50 V
E1 120 Ohm Normal
22 Nov 2005
02:04:52

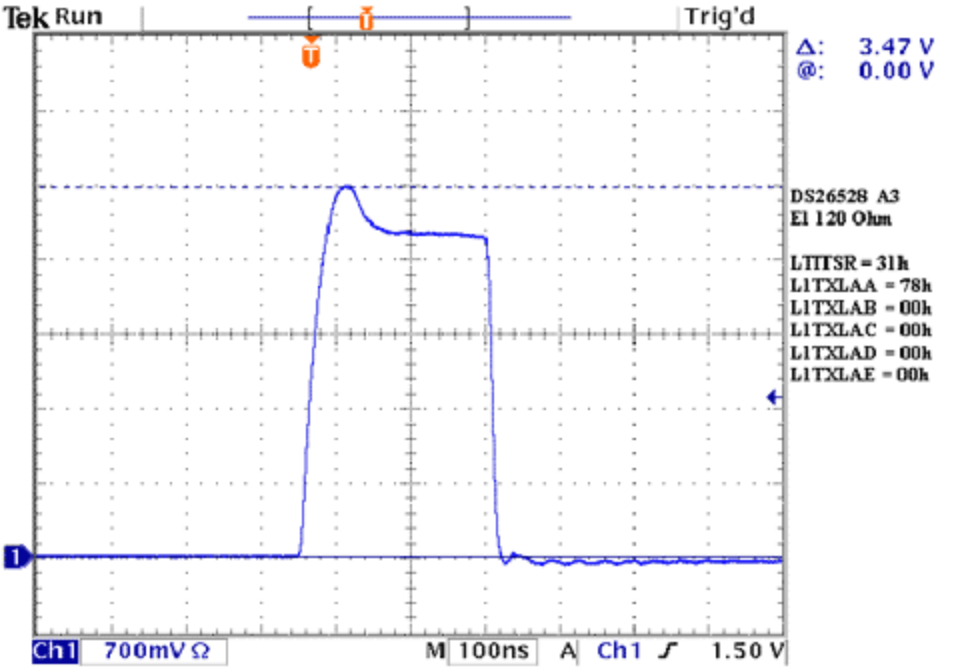
E1 120Ω Mode
Min Overshoot (1) = 2.77V
Max Clock Edge (1CE) = 130nS



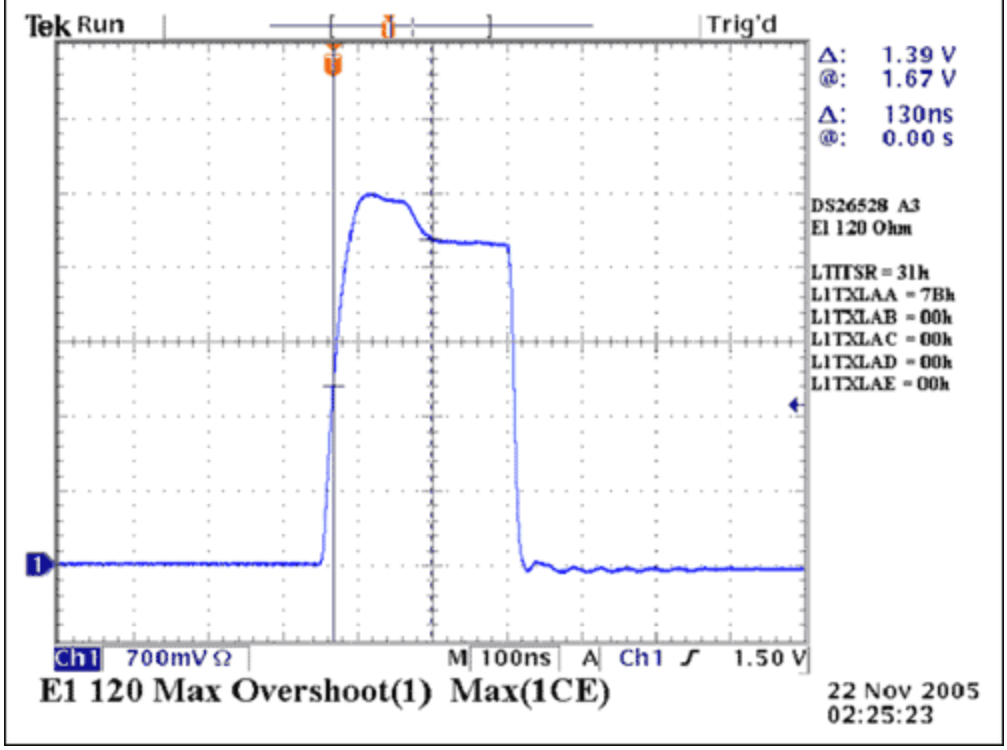
E1 120Ω Mode
Max Overshoot (1) = 3.12V
Min Clock Edge (1CE) = 100nS



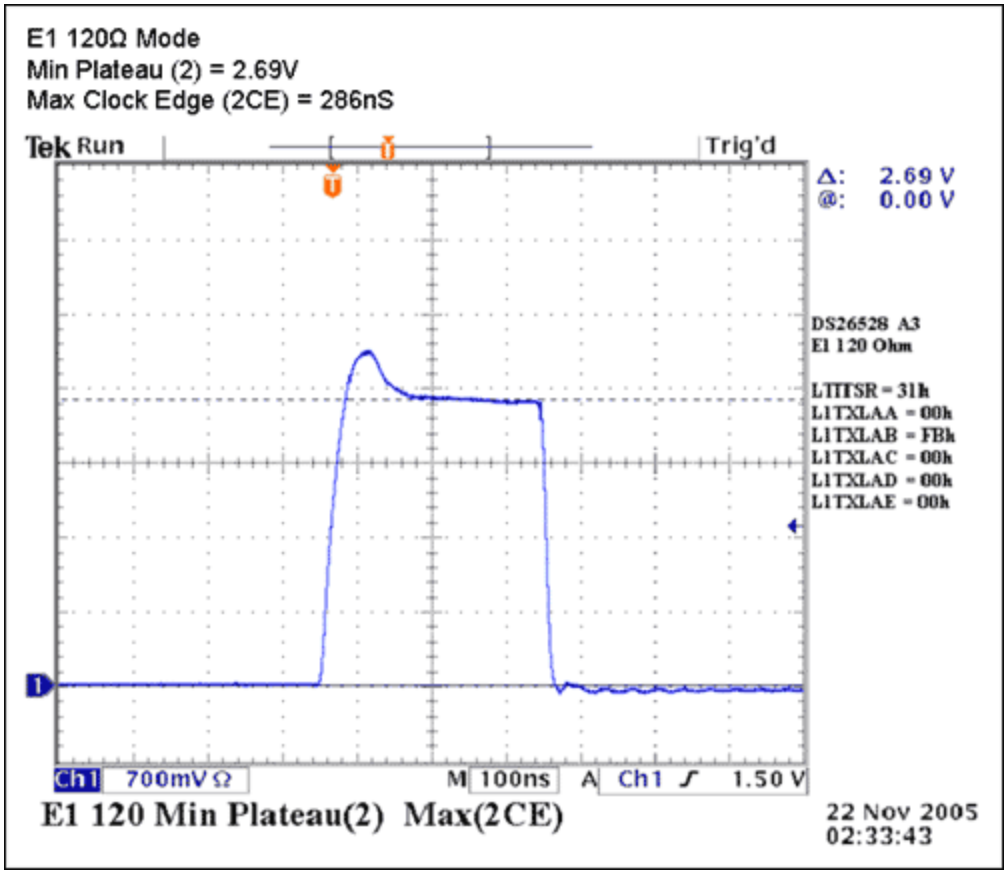
E1 120Ω Mode
Max Overshoot (1) = 3.47V
Normal Clock Edge (1CE) = 108nS

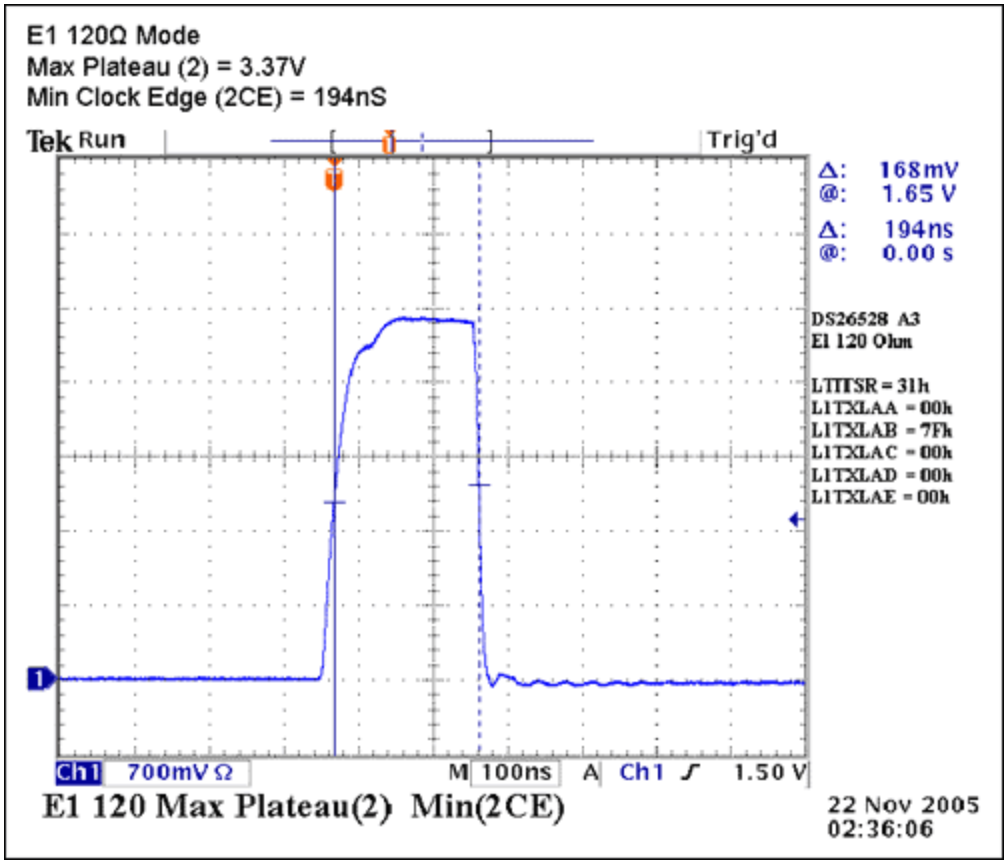


E1 120Ω Mode
Max Overshoot (1) = 3.47V
Max Clock Edge (1CE) = 130nS

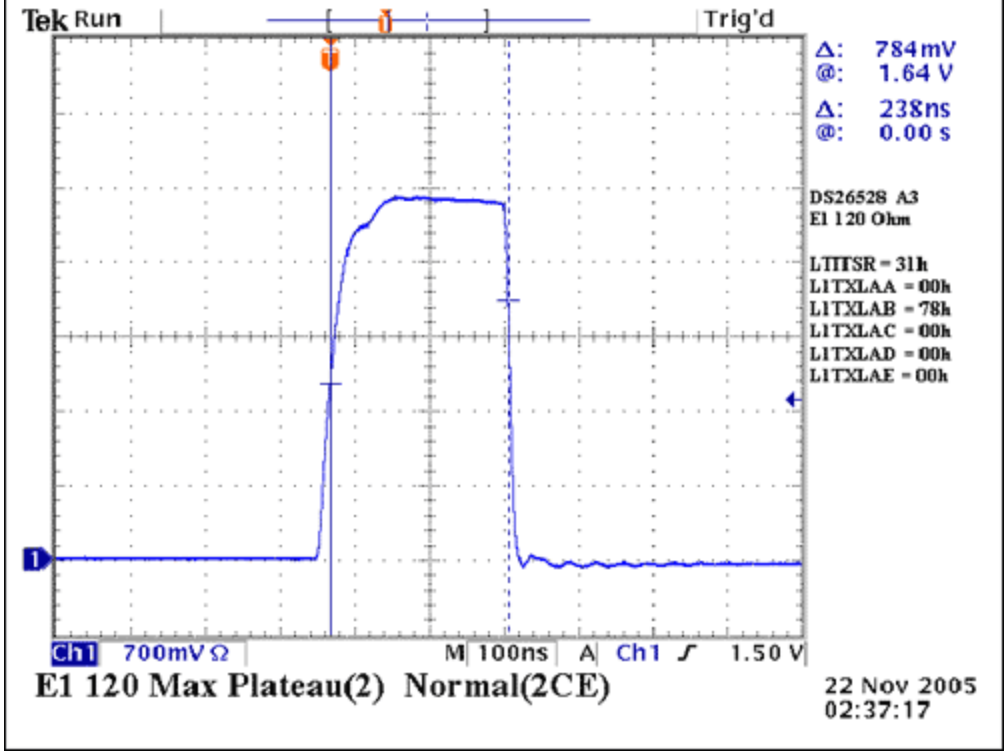


E1 120Ω Mode
Min Plateau (2) = 2.69V
Max Clock Edge (2CE) = 286nS

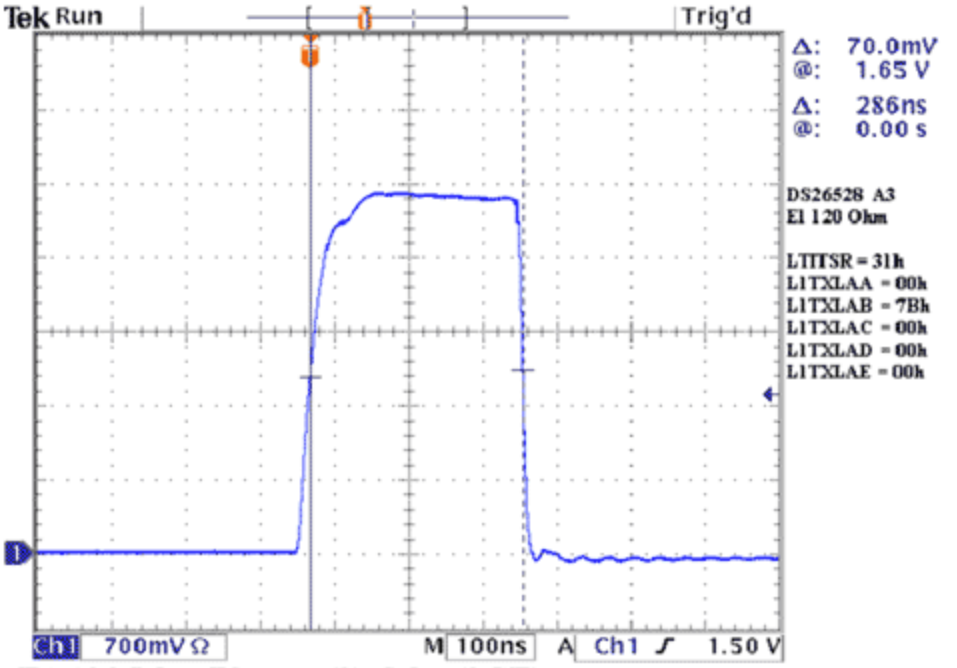


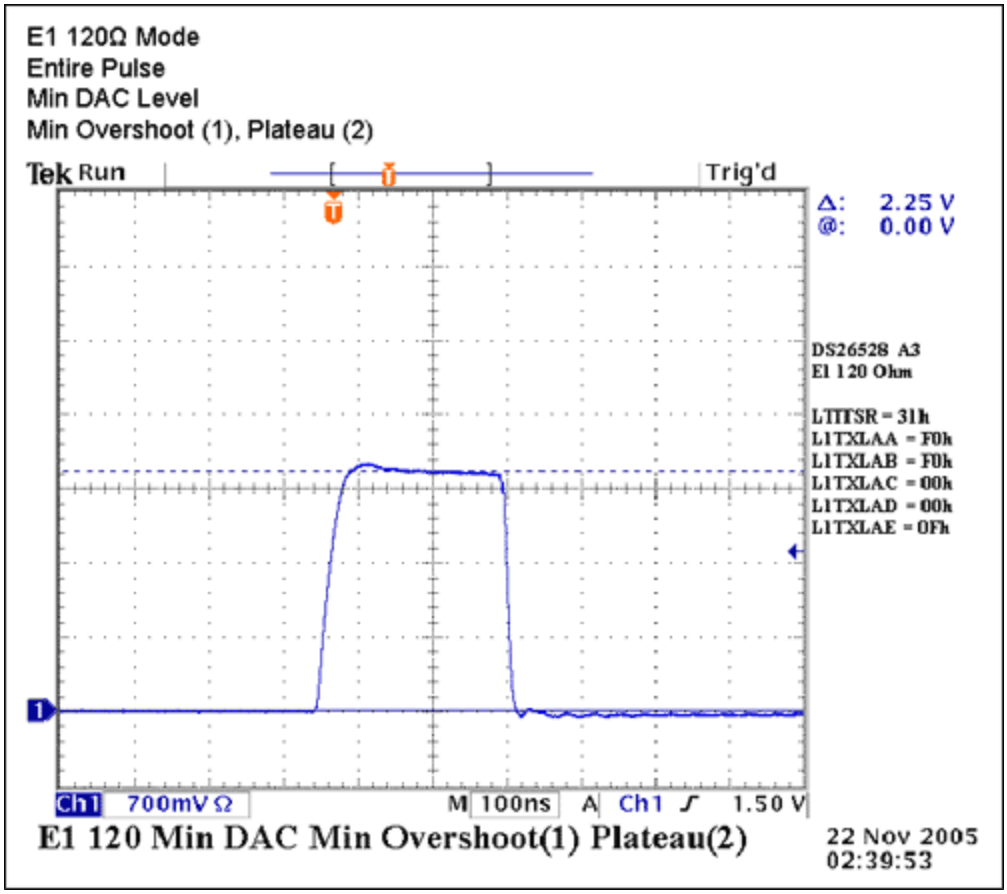

E1 120Ω Mode
Max Plateau (2) = 3.37V
Min Clock Edge (2CE) = 194nS
Tek Run
Trig'd
Δ: 168mV
@: 1.65 V
Δ: 194ns
@: 0.00 s
DS26528 A3
E1 120 Ohm
LIITSR = 31h
L1TXLAA = 00h
L1TXLAB = 7Fh
L1TXLAC = 00h
L1TXLAD = 00h
L1TXLAE = 00h
Ch1 700mV Ω
M 100ns A Ch1 1.50 V
E1 120 Max Plateau(2) Min(2CE)
22 Nov 2005
02:36:06

E1 120Ω Mode
Max Plateau (2) = 3.37V
Normal Clock Edge (2CE) = 238nS

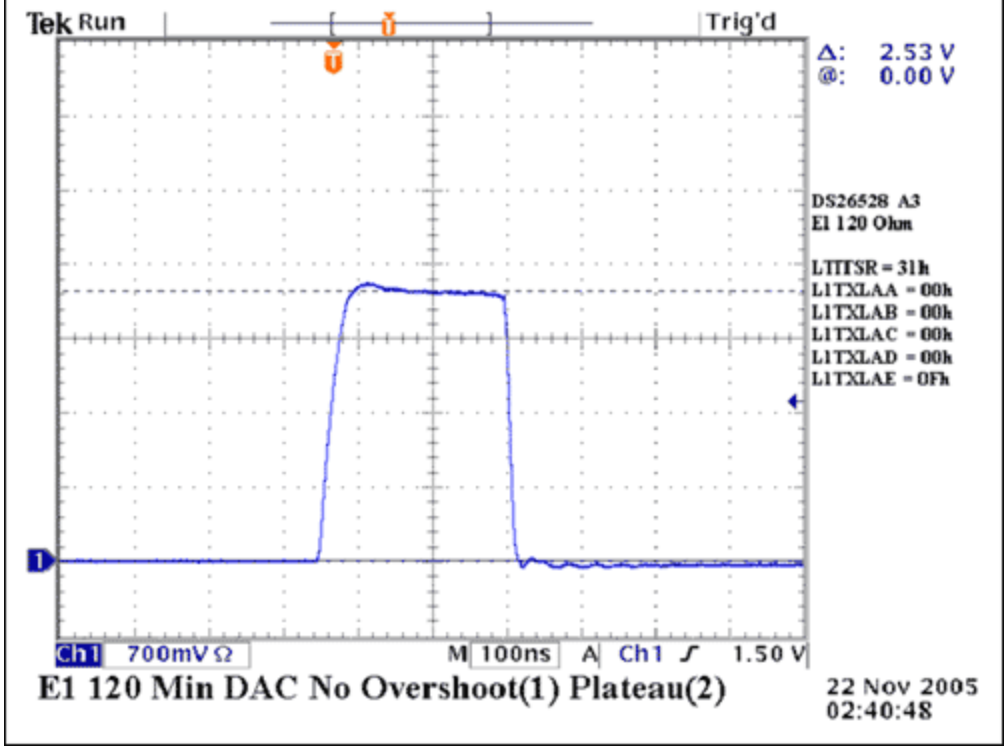


E1 120Ω Mode
Max Plateau (2) = 3.37V
Max Clock Edge (2CE) = 286nS

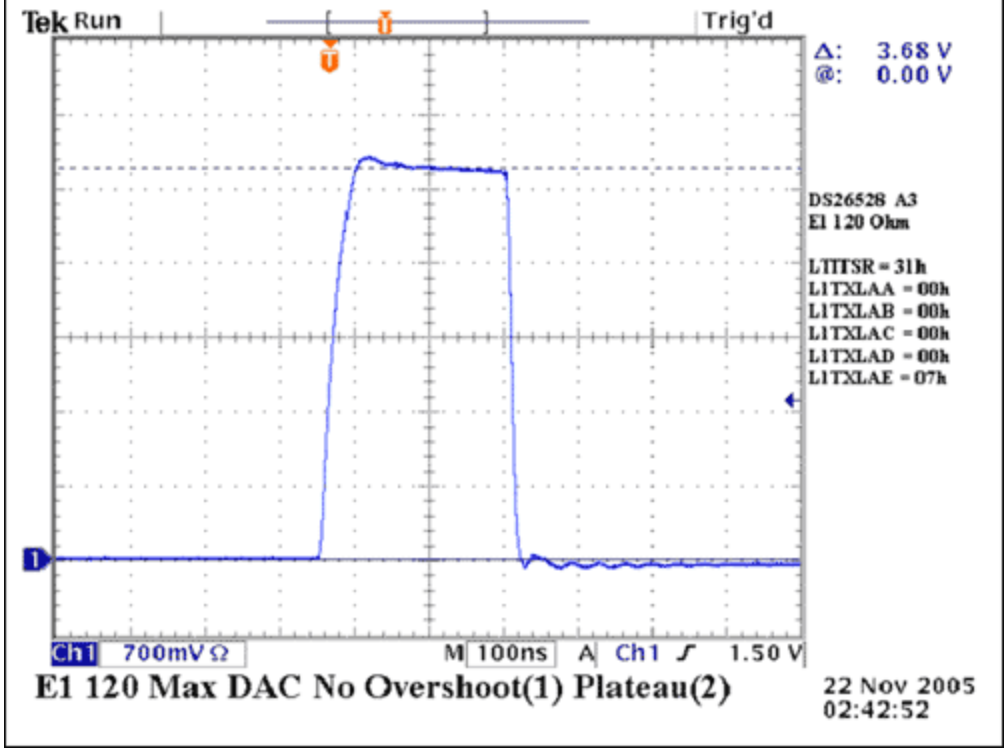



E1 120Ω Mode
Entire Pulse
Min DAC Level
Min Overshoot (1), Plateau (2)
Tek Run
Trig'd
Δ: 2.25 V
@: 0.00 V
DS26528 A3
E1 120 Ohm
LITSR = 31h
L1TXLAA = F0h
L1TXLAB = F0h
L1TXLAC = 00h
L1TXLAD = 00h
L1TXLAE = 0Fh
Ch1 700mV Ω
M 100ns A Ch1 1.50 V
E1 120 Min DAC Min Overshoot(1) Plateau(2)
22 Nov 2005
02:39:53

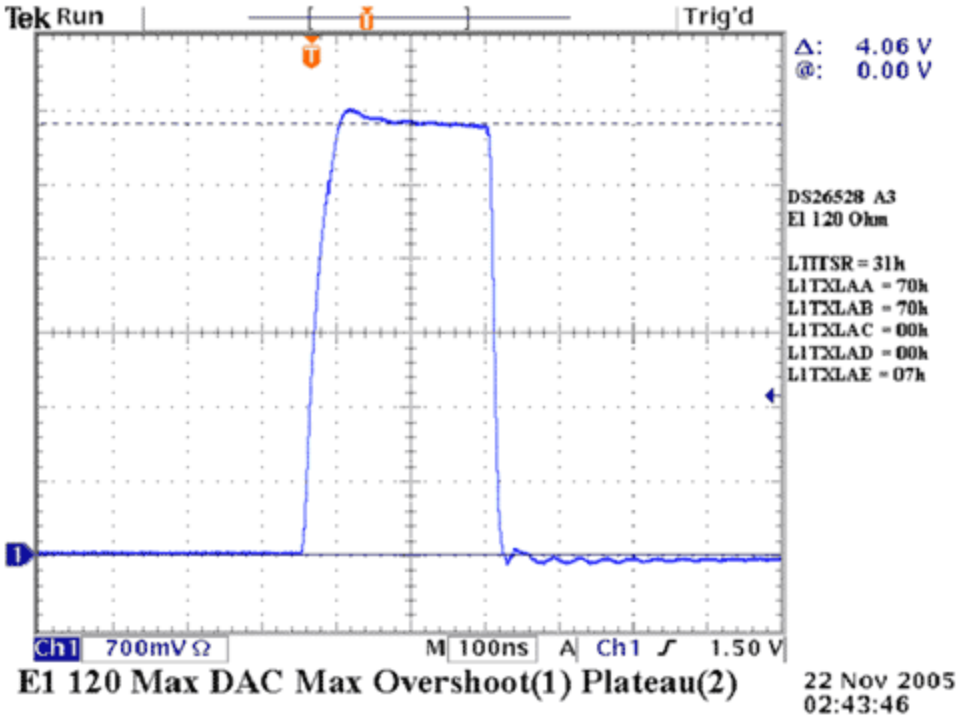
E1 120Ω Mode
Entire Pulse
Min DAC Level
No Overshoot (1), Plateau (2)

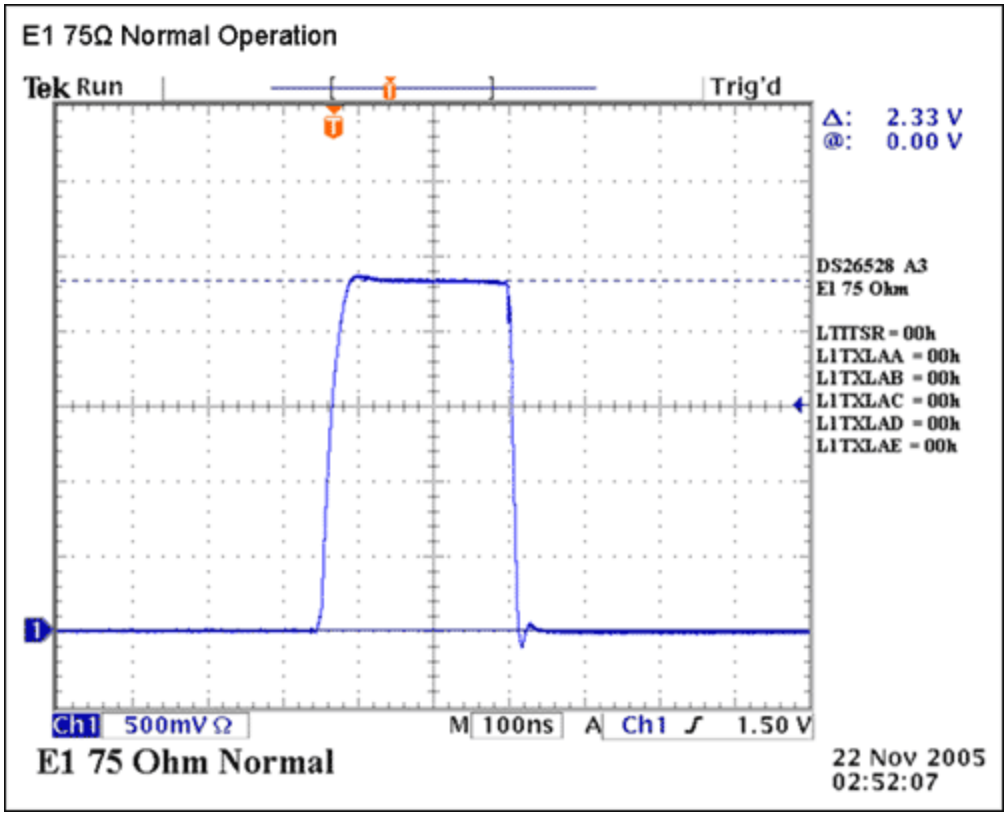


E1 120Ω Mode
Entire Pulse
Max DAC Level
No Overshoot (1), Plateau (2)

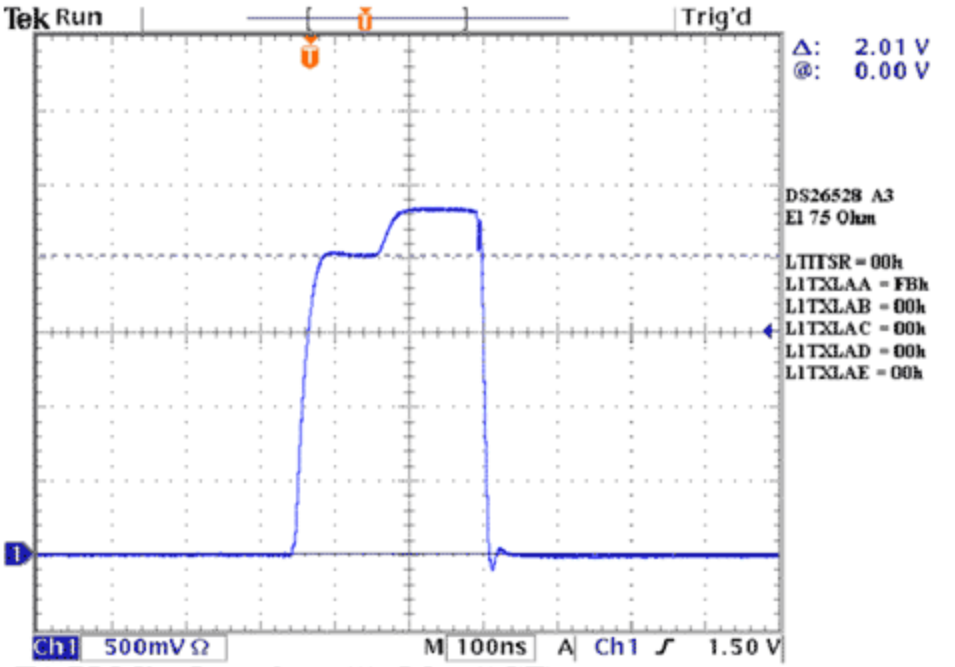


E1 120Ω Mode
Entire Pulse
Max DAC Level
Max Overshoot (1), Plateau (2)

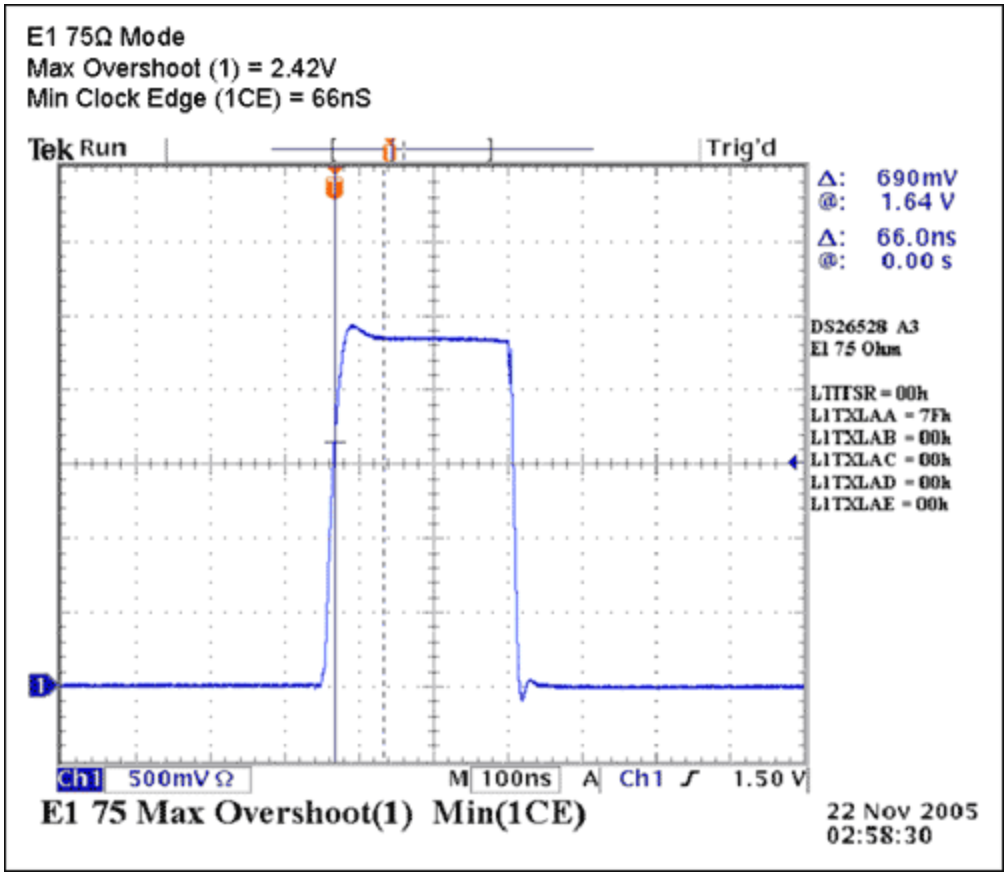



E1 75Ω Normal Operation
Tek Run
Trig'd
Δ: 2.33 V
@: 0.00 V
DS26528 A3
E1 75 Ohm
LTITSR = 00h
L1TXLAA = 00h
L1TXLAB = 00h
L1TXLAC = 00h
L1TXLAD = 00h
L1TXLAE = 00h
Ch1 500mV Ω
M 100ns A Ch1 1.50 V
E1 75 Ohm Normal
22 Nov 2005
02:52:07

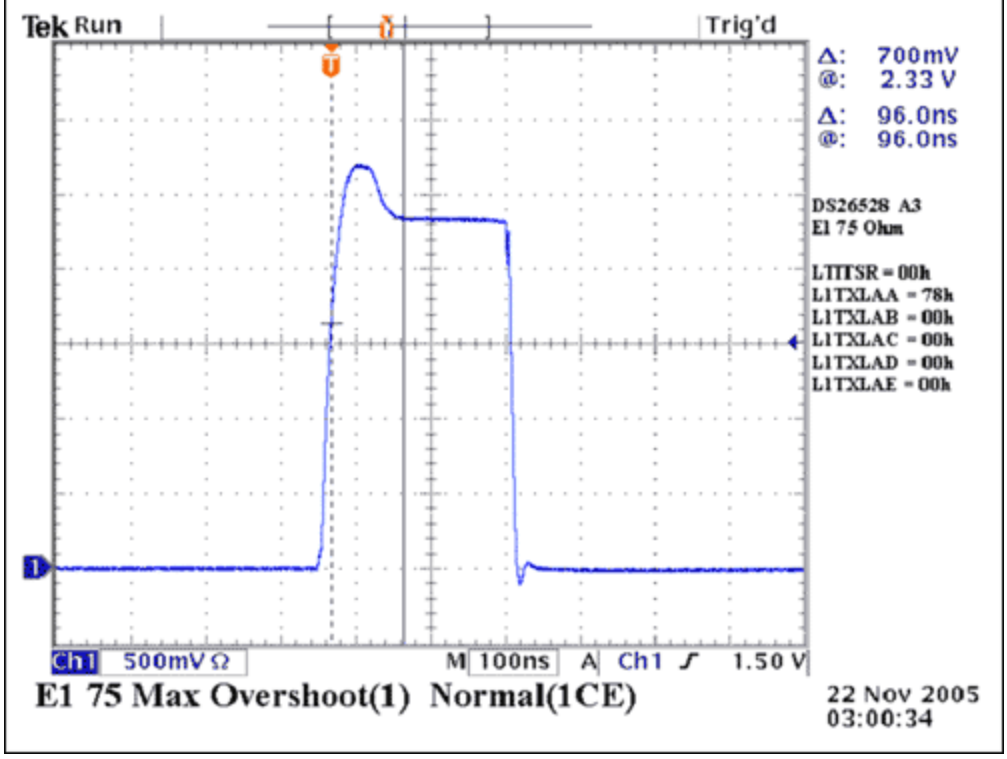
E1 75Ω Mode
Min Overshoot (1) = 2.01V
Max Clock Edge (1CE) = 130nS



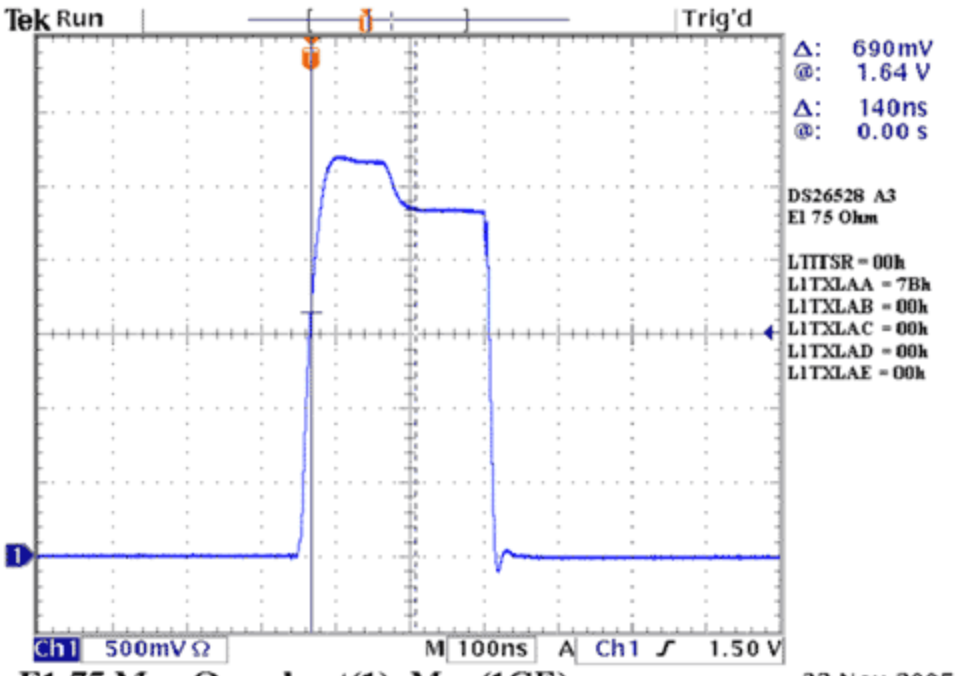
E1 75Ω Mode
Max Overshoot (1) = 2.42V
Min Clock Edge (1CE) = 66nS



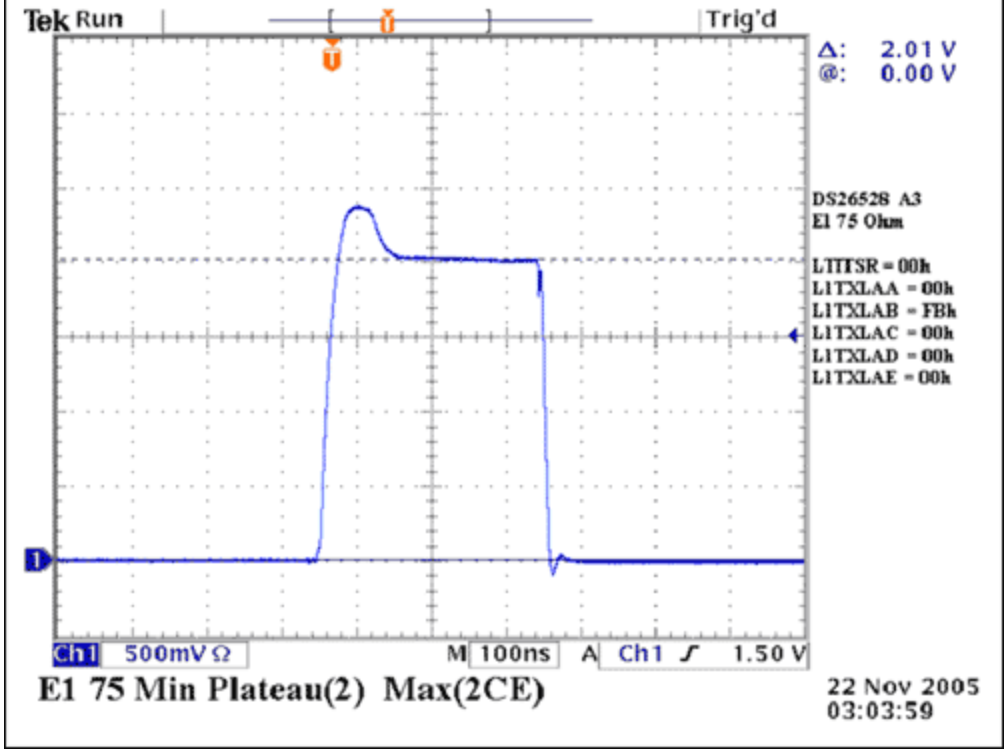
E1 75Ω Mode
Max Overshoot (1) = 2.67V
Normal Clock Edge (1CE) = 96nS



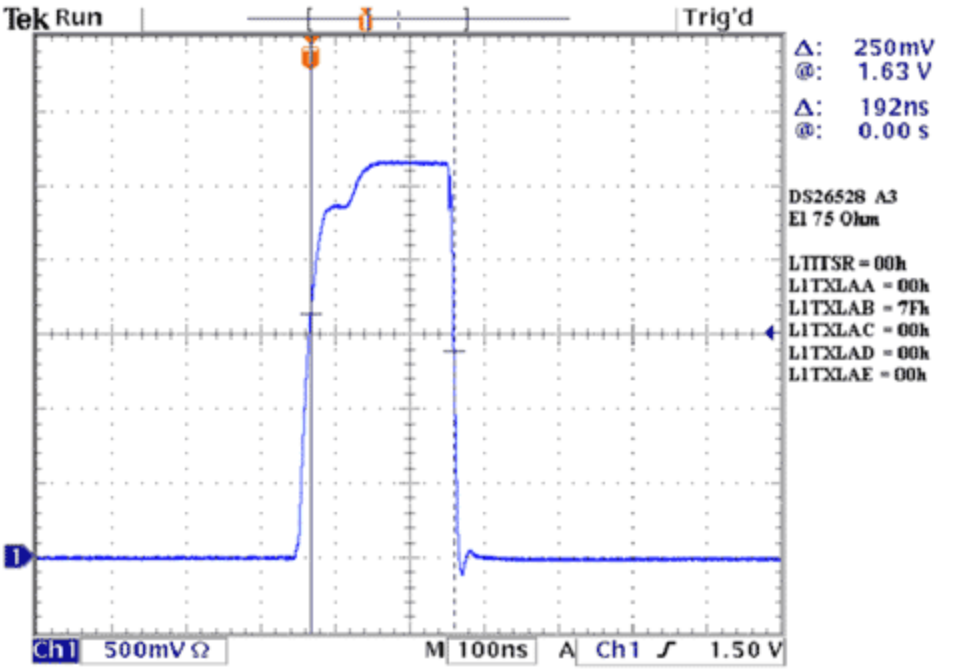
E1 75Ω Mode
Max Overshoot (1) = 2.67V
Max Clock Edge (1CE) = 140nS



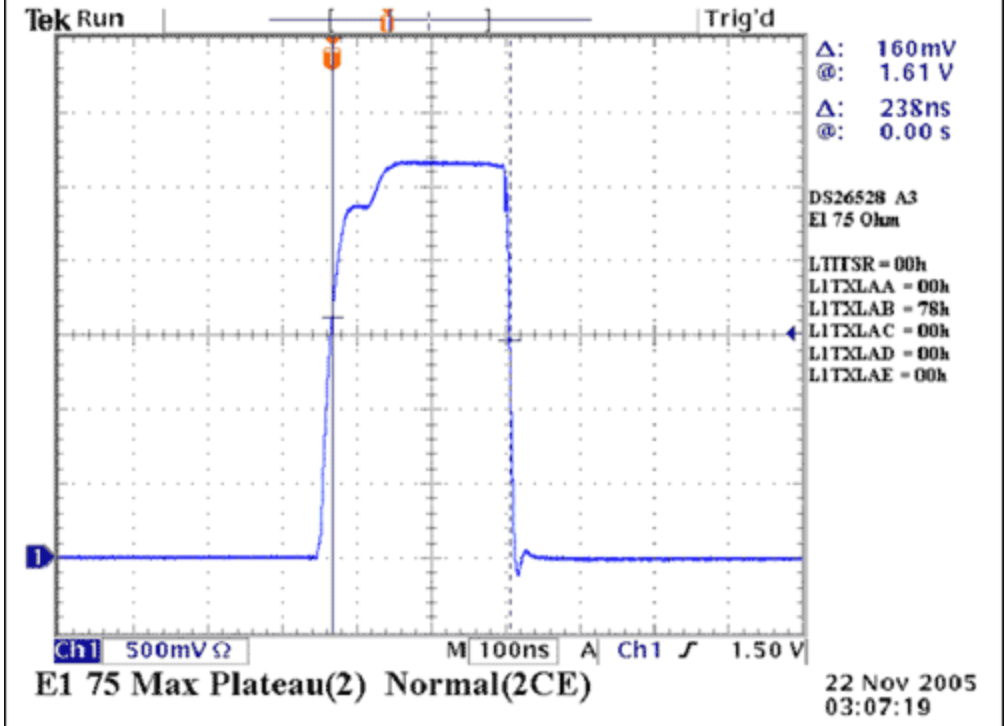
E1 75Ω Mode
Min Plateau (2) = 2.01V
Max Clock Edge (2CE) = 284nS



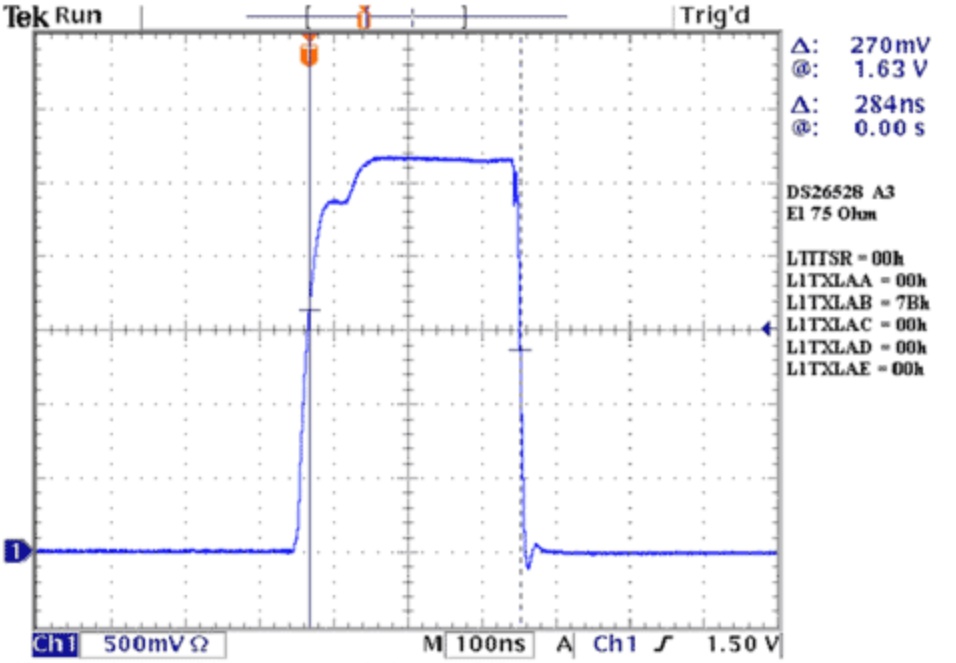
E1 75Ω Mode
Max Plateau (2) = 2.65V
Min Clock Edge (2CE) = 192nS



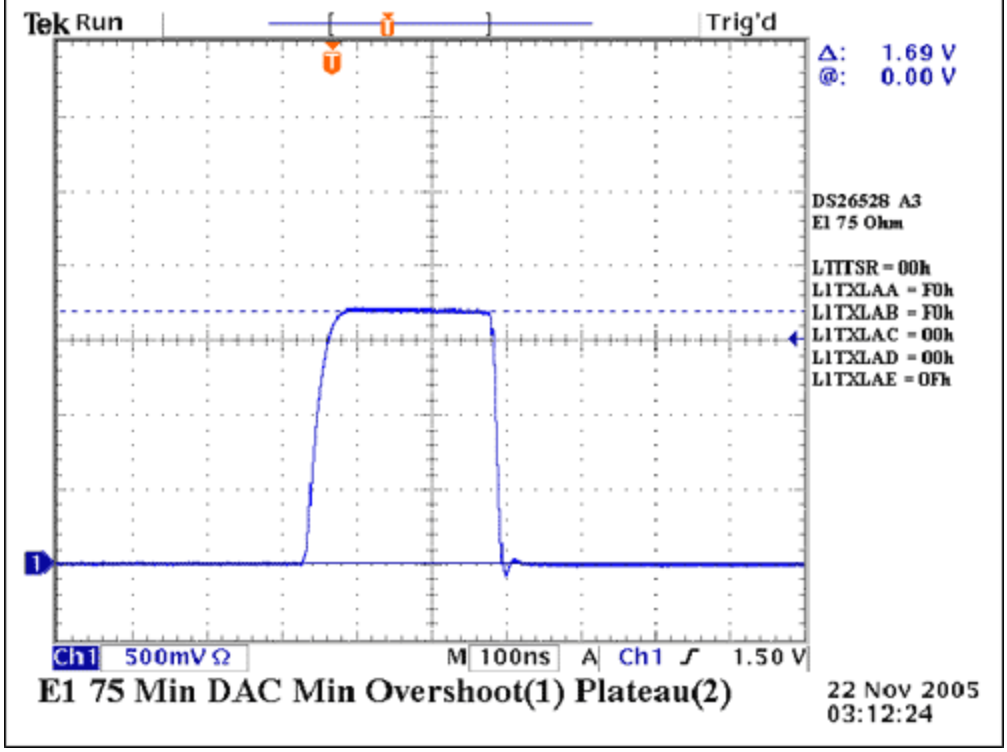
E1 75Ω Mode
Max Plateau (2) = 2.65V
Normal Clock Edge (2CE) = 238nS



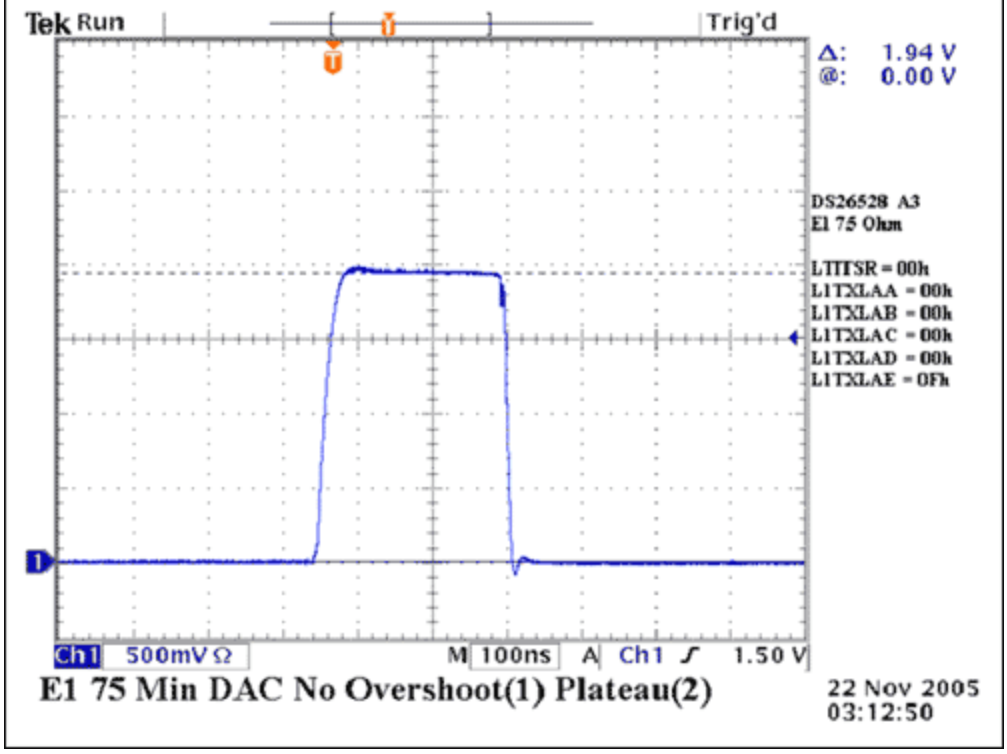
E1 75Ω Mode
Max Plateau (2) = 2.65V
Max Clock Edge (2CE) = 284nS



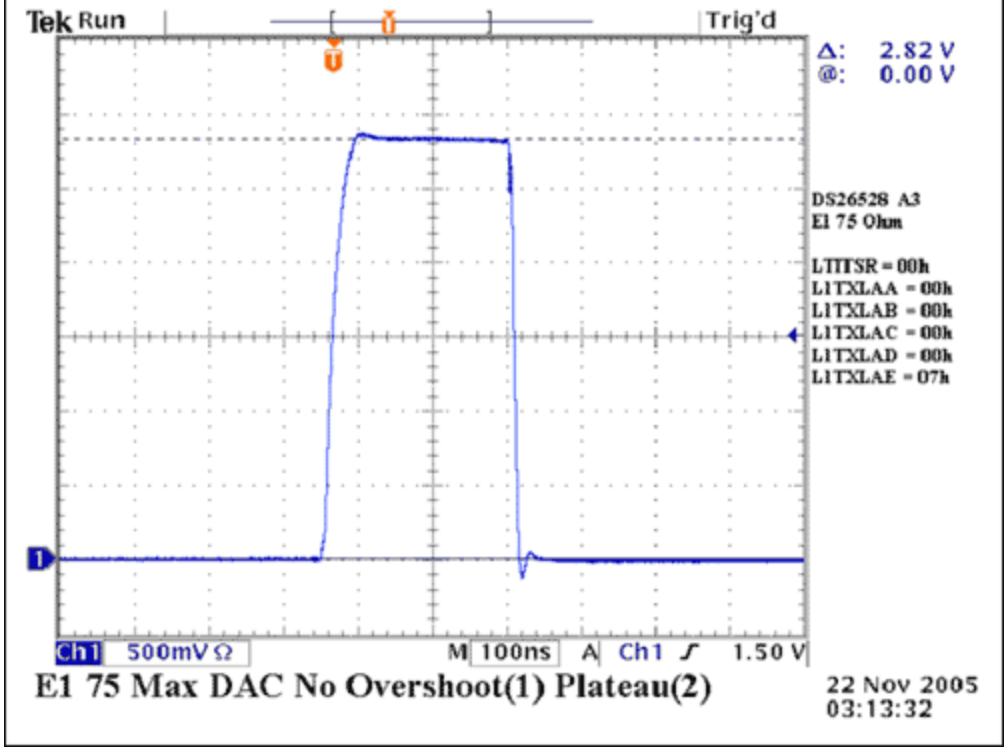
E1 75Ω Mode
Entire Pulse
Min DAC Level
Min Overshoot (1), Plateau (2)

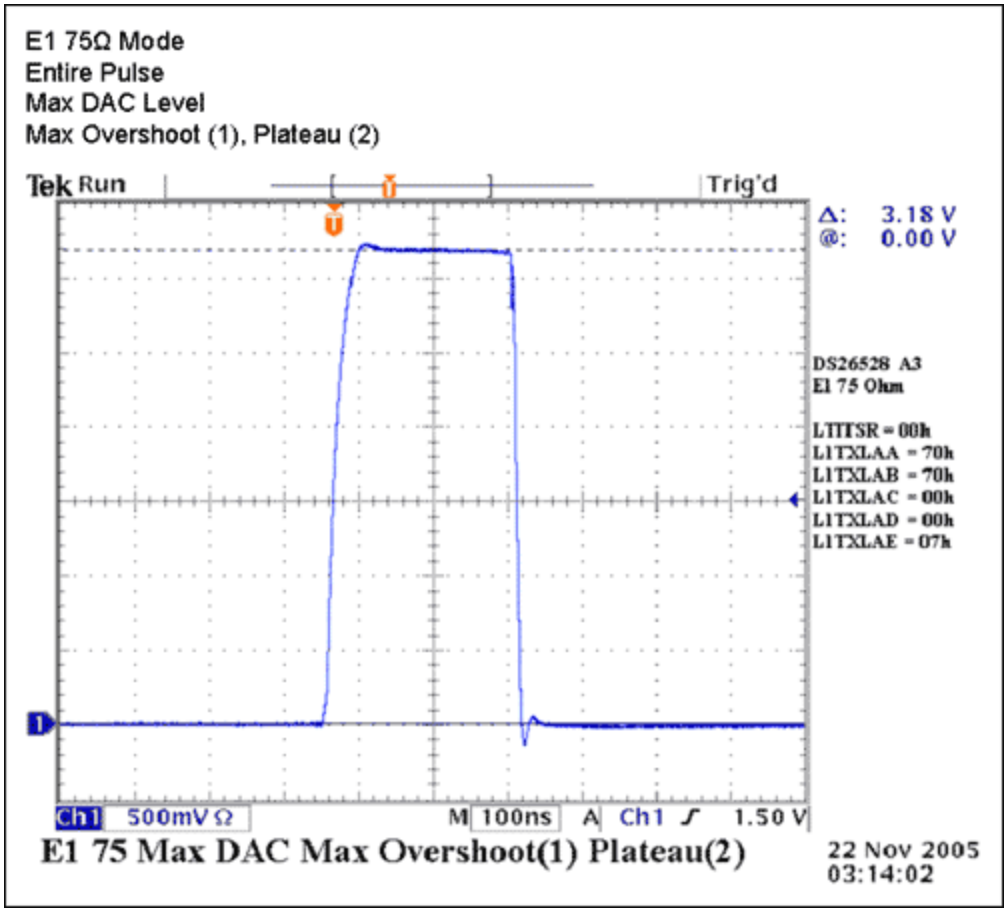


E1 75Ω Mode
Entire Pulse
Min DAC Level
No Overshoot (1), Plateau (2)



E1 75Ω Mode
Entire Pulse
Max DAC Level
No Overshoot (1), Plateau (2)





DS26528 and DS26524 Information

For more information about Maxim's products, please consult the data sheets available on our website at www.maximintegrated.com/telecom. If you have further questions concerning the operation of Maxim devices, please contact the Telecommunication Applications support team.

Related Parts		
DS26524	Quad T1/E1/J1 Transceiver	Free Samples
DS26528	Octal T1/E1/J1 Transceiver	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 3718: http://www.maximintegrated.com/an3718
APPLICATION NOTE 3718, AN3718, AN 3718, APP3718, Appnote3718, Appnote 3718