TPS56C215EVM-762 12-A, SWIFT™ Regulator Evaluation Module

This user's guide contains information for the TPS56C215EVM-762 evaluation module (PWR762) as well as for the TPS56C215 dc/dc converter. Also included are the performance specifications, the schematic, and the bill of materials for the TPS56C215EVM-762.

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Trademarks

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1 Introduction

1.1 Background

The TPS56C215 dc/dc converter is a synchronous buck converter designed to provide up to a 14-A output. The input (VIN) is rated for 4.5 V to 17 V. The TPS56C215 uses a proprietary DCAP3 Control mode and a MODE pin is used to select output current limit, switching frequency, and Forced Continuous Conduction Mode (FCCM)/Discontinuous Conduction Mode (DCM) operation. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS56C215 regulator. The MODE pin is configured for 1.2-MHz switching frequency, 12-A and DCM operation. The high-side and low-side MOSFETs are incorporated inside the TPS56C215 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS56C215 to achieve high efficiencies and helps keep the junction temperature low at high output currents. An external divider allows for an adjustable output voltage. Additionally, the TPS56C215 provides adjustable slow start and undervoltage lockout inputs and a power good output.

Table 1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS56C215EVM-762	VIN = 4.5 V to 17 V	0 A to 12 A

1.2 Performance Specification Summary

A summary of the TPS56C215EVM-762 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.2 V, unless otherwise specified. The TPS56C215EVM-762 is designed and tested for V_{IN} = 4.5 V to 17 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS56C215EVM-762 Performance Specification Summary

Specification	Test Conditions		MIN	TYP	MAX	Unit
V_{IN} voltage range			4.5	12	17	V
V_{IN} start voltage				Internal UVLO		V
V_{IN} stop voltage				Internal UVLO		V
Output voltage setpoint				1.2		V
Output current range	V_{IN} = 9.2 V to 14 V		0		12	A
Line regulation	I_O = 6 A, V_{IN} = 4.5 V to 17 V			±0.05%		
Load regulation	V_{IN} = 12 V, I_O = 0 A to 12 A			–0.02%, +0.6%		
Load transient response	I_O = 3 A to 9 A	Voltage change		–30		mV
		Recovery time		50		µs
	I_O = 9 A to 3 A	Voltage change		30		mV
		Recovery time		50		µs
Loop bandwidth	V_{IN} = 12 V, I_O = 6 A			135		kHz
Phase margin	V_{IN} = 12 V , I_O = 6 A			72		degree
Input ripple voltage	I_O = 12 A			120		mVPP
Output ripple voltage	I_O = 12 A			10		mVPP
Output rise time				6		ms
Operating frequency				1.2		MHz
Maximum efficiency	TPS56C215EVM-762, V_{IN} = 5 V, I_O = 5.7 A			82.2%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS56C215. Some modifications can be made to this module.

1.3.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R7 ($R_{(TOP)}$) and R9 ($R_{(BOT)}$). R9 is fixed at 10.0 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R7. Changing the value of R9 can change the output voltage above the 0.6 V reference voltage V_{REF}. The value of R7 for a specific output voltage can be calculated using Equation 1.

$$R_{(TOP)} = \frac{R_{(BOT)} x \left(V_{OUT} - V_{REF}\right)}{V_{REF}} \quad (1)$$

1.3.2 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R1 ($R_{EN(TOP)}$) and R2 ($R_{EN(BOT)}$). R1 and R2 are not populated on the EVM, which uses the internal UVLO default settings. See the TPS56C215 datasheet (SLVSD05) for detailed instructions for setting the external UVLO.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS56C215EVM-762 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS56C215EVM-762 is provided with input/output connectors and test points as shown in Table 3. A power supply capable of supplying greater than 4 A must be connected to J1 through a pair of 20-AWG wires or better. The load must be connected to J2 through a pair of 20-AWG wires or better. The maximum load current capability is 12 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP9 is used to monitor the output voltage with TP10 as the ground reference.

Table 3. EVM Connectors and Test Points

Reference Designator	Function
J1	VIN input voltage connector. (See Table 1 for V_{IN} range)
J2	1.2 V at 10 A maximum
J3	2-pin header for enable. Connect EN to ground to disable, open to enable. V_{OUT}.
J4	VOUT, 1.2 V at 10 A maximum
TP1	VIN test point
TP2	GND test point at VIN connector
TP3	Slow Start (SS) test point
TP4	PGOOD test point
TP5	VREG5 test point
TP6	Test point between voltage divider network and output. Used for loop response measurements
TP7	SW node test point
TP8	AGND test point
TP9	VOUT test point
TP10	GND test point

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 5 A and then decreases as the load current increases toward full load. Figure 1 shows the efficiency for the TPS56C215EVM-762 at an ambient temperature of 25°C.

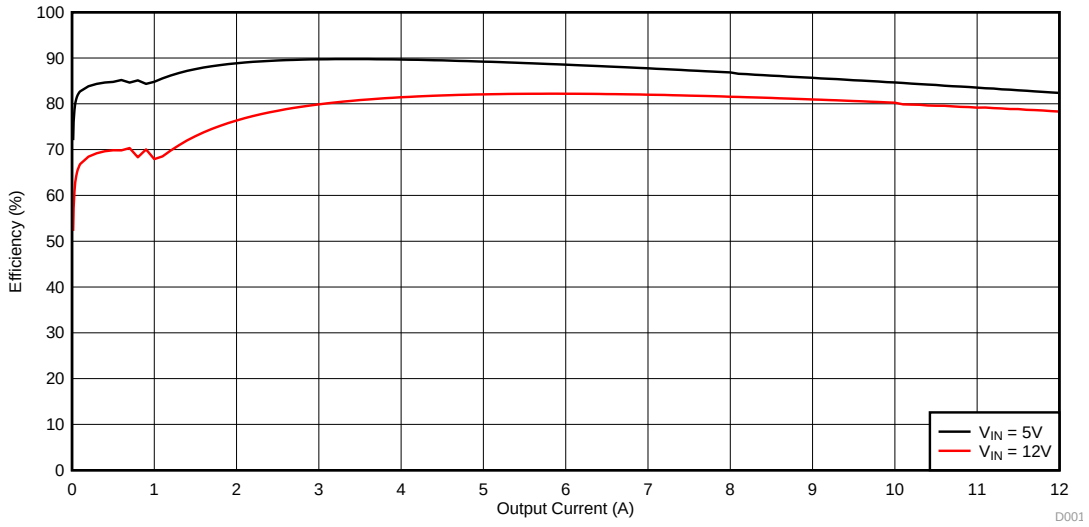

Figure 1. TPS56C215EVM-762 Efficiency

Figure 2 shows the efficiency for the TPS56C215EVM-762 using a semi-log scale to more easily show efficiency at lower output currents. The ambient temperature is 25°C.

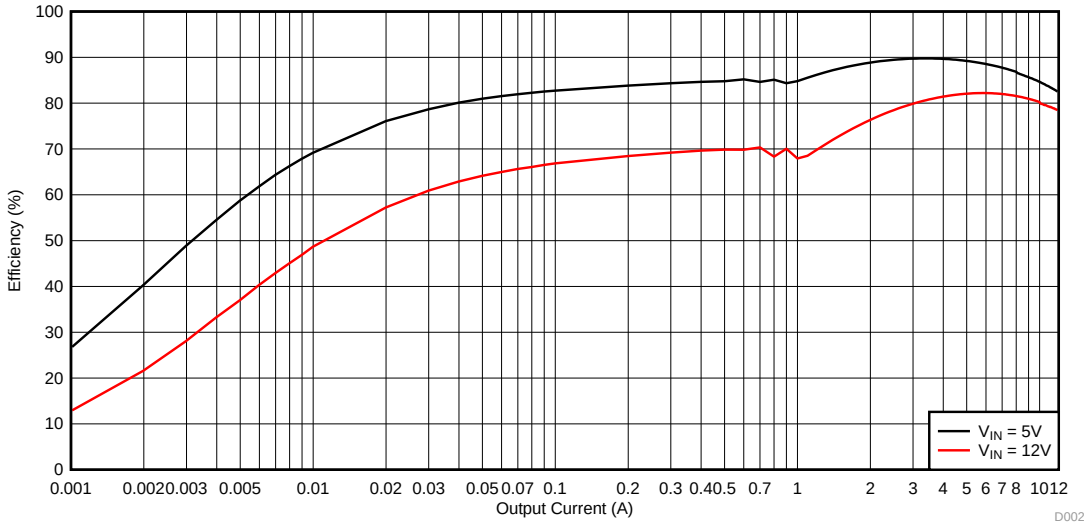

Figure 2. TPS56C215EVM-762 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 3 and Figure 4 show the load regulation for the TPS56C215EVM-762.

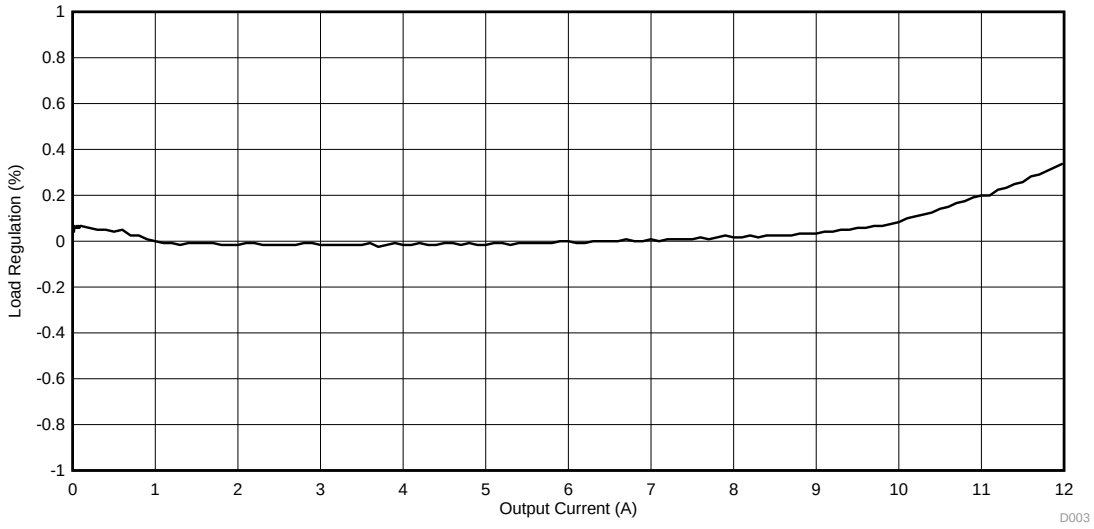

Figure 3. TPS56C215EVM-762 Load Regulation, V_{IN} = 5 V

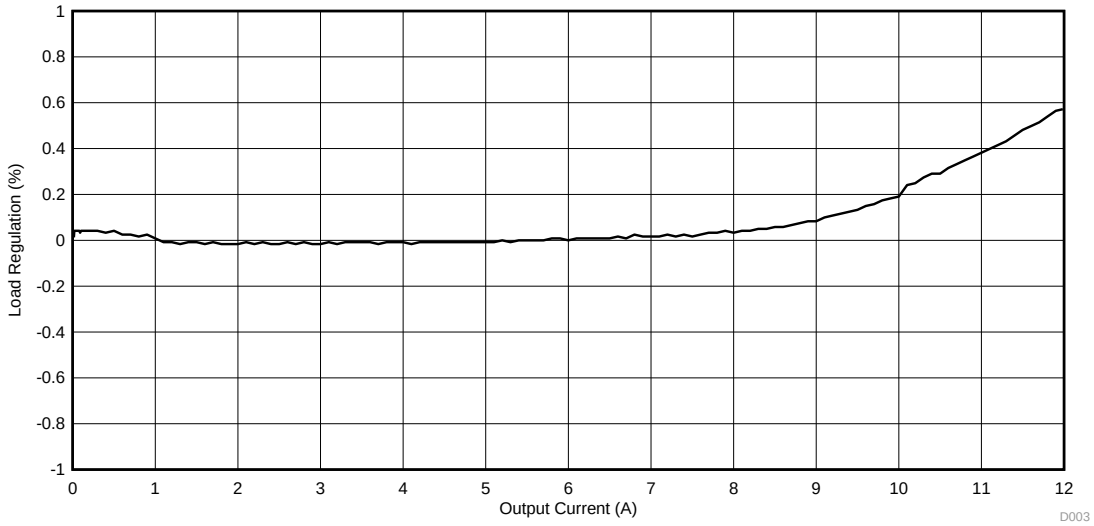

Figure 4. TPS56C215EVM-762 Load Regulation, V_{IN} = 12 V

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 5 shows the line regulation for the TPS56C215EVM-762.

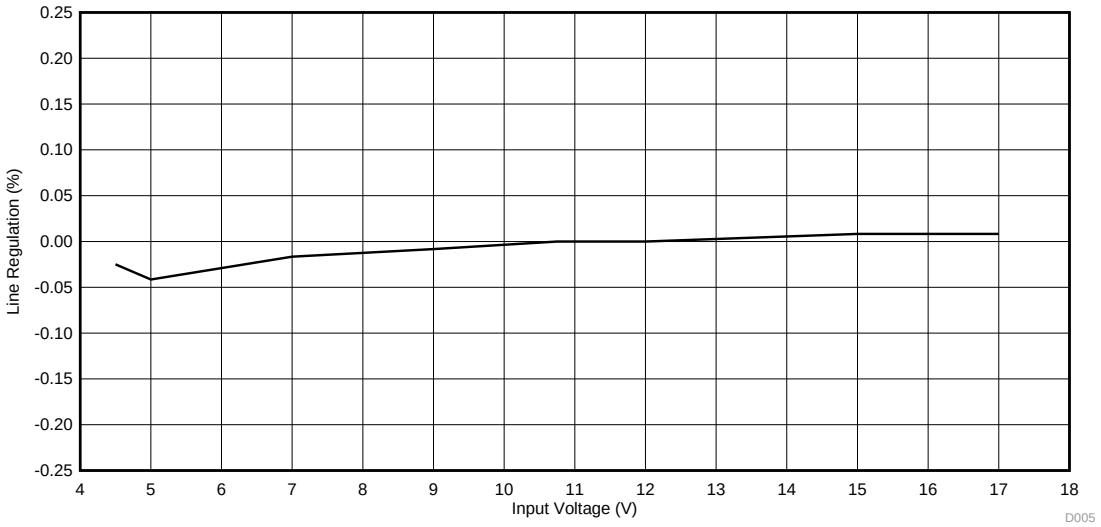

Figure 5. TPS56C215EVM-762 Line Regulation

2.5 Load Transients

Figure 6 shows the TPS56C215EVM-762 response to load transients. The current step is from 3 A to 9 A. The current step slew rate is 1 A/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output. The transient waveform is measured using the on-board fast transient circuit.

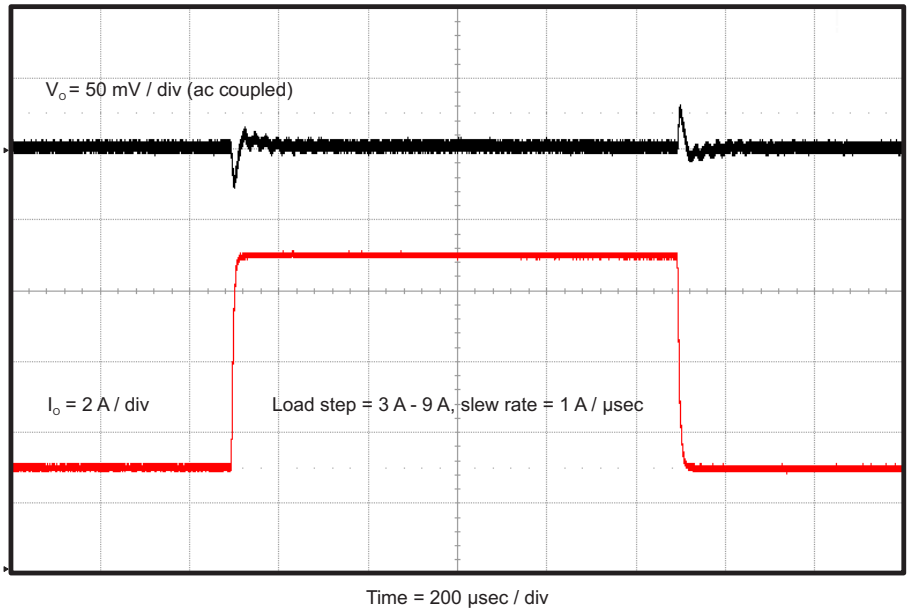

Figure 6. TPS56C215EVM-762 Transient Response

2.6 Loop Characteristics

Figure 7 shows the TPS56C215EVM-762 loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 5 A.

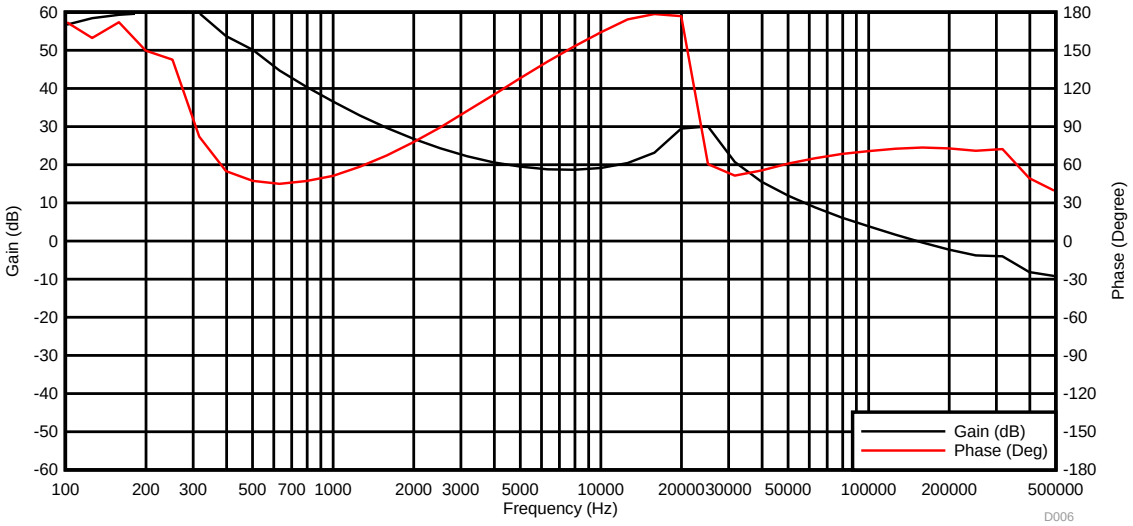

Figure 7. TPS56C215EVM-762 Loop Response

2.7 Output Voltage Ripple

Figure 8, Figure 9, and Figure 10 show the TPS56C215EVM-762 output voltage ripple. The load currents are 10 mA, 800 mA and 12 A. V_{IN} = 12 V. The ripple voltage is measured directly across TP7 and TP8.

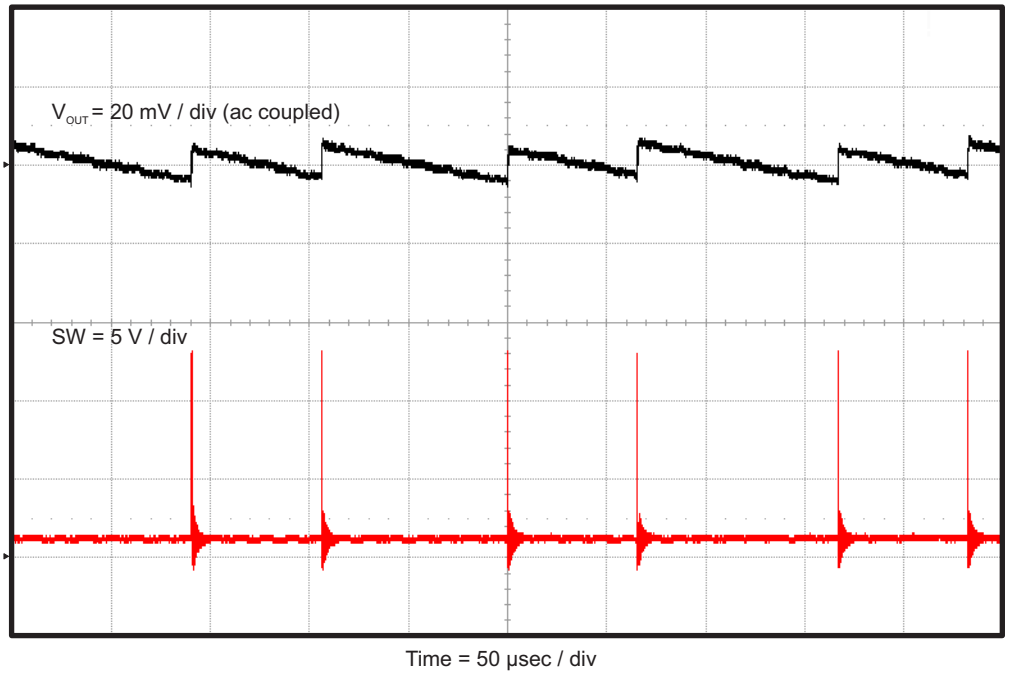

Figure 8. TPS56C215EVM-762 Output Ripple, 10 mA Load

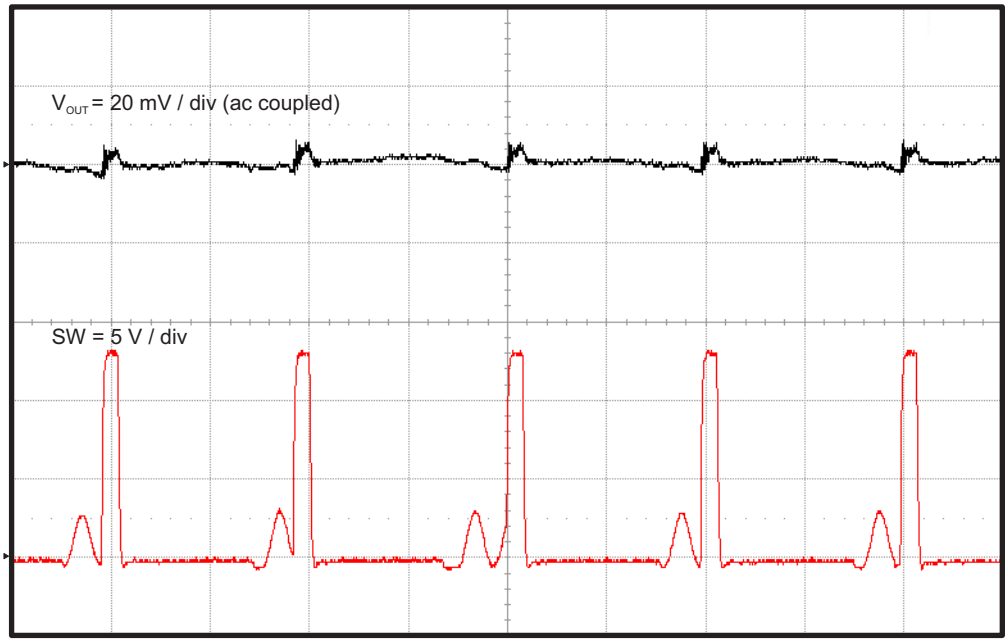

Figure 9. TPS56C215EVM-762 Output Ripple, 800 mA Load

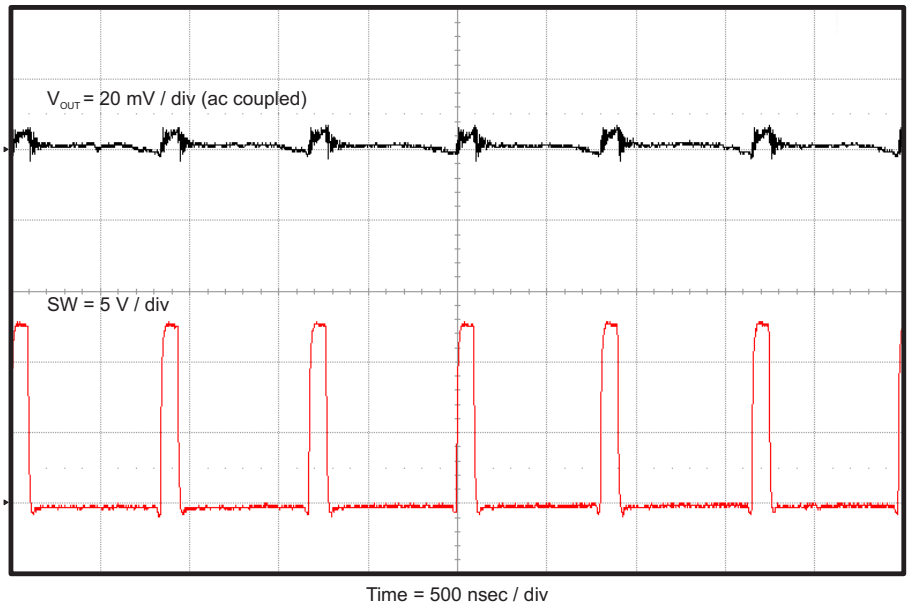

Figure 10. TPS56C215EVM-762 Output Ripple, 12-A Load

2.8 Input Voltage Ripple

Figure 11, Figure 12, and Figure 13 show the TPS56C215EVM-762 input voltage ripple. The load currents are 10 mA, 800 mA and 12 A. V_{IN} = 12 V. The ripple voltage is measured directly across TP1 and TP2.

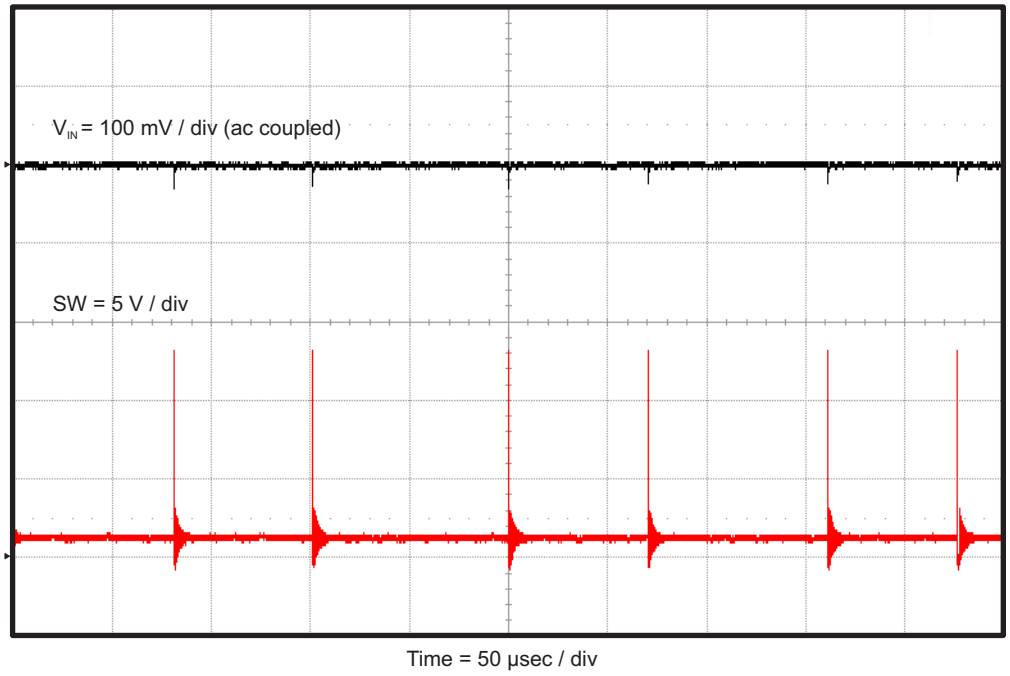

Figure 11. TPS56C215EVM-762 Input Ripple, 10-mA Load

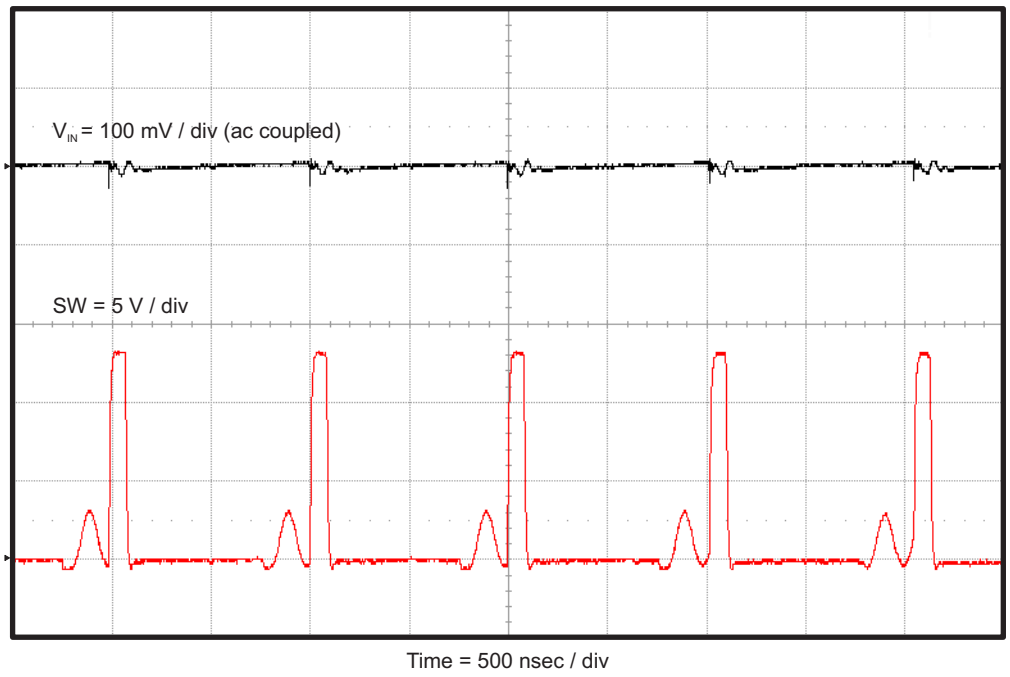

Figure 12. TPS56C215EVM-762 Input Ripple, 800-mA Load

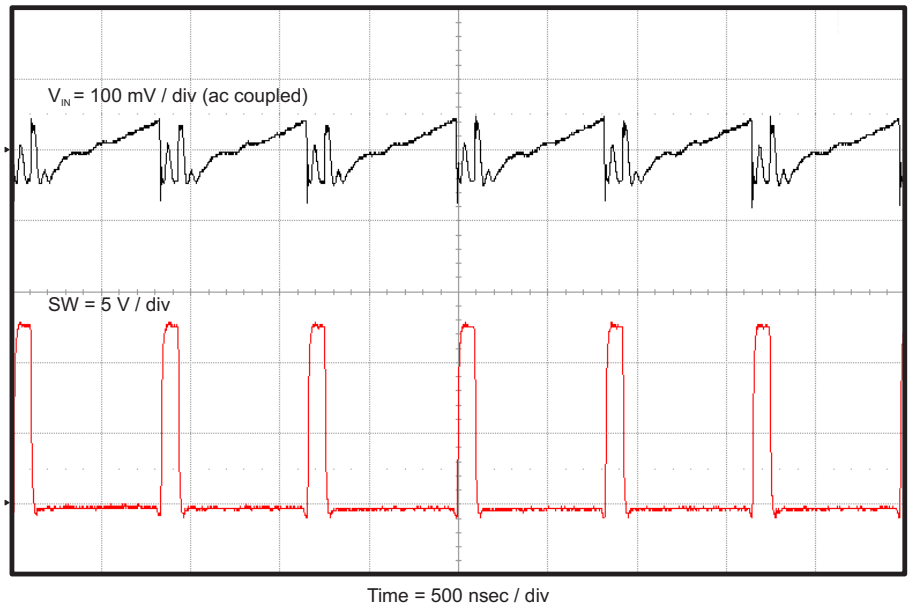

Figure 13. TPS56C215EVM-762 Input Ripple, 12-A Load

2.9 Powering Up

Figure 14 and Figure 15 show the start-up waveforms for the TPS56C215EVM-762. In Figure 14, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold. In Figure 15, the input voltage is initially applied and the output is inhibited by using a jumper at J2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.2 V. The input voltage for these plots is 12 V and the load is 1 Ω.

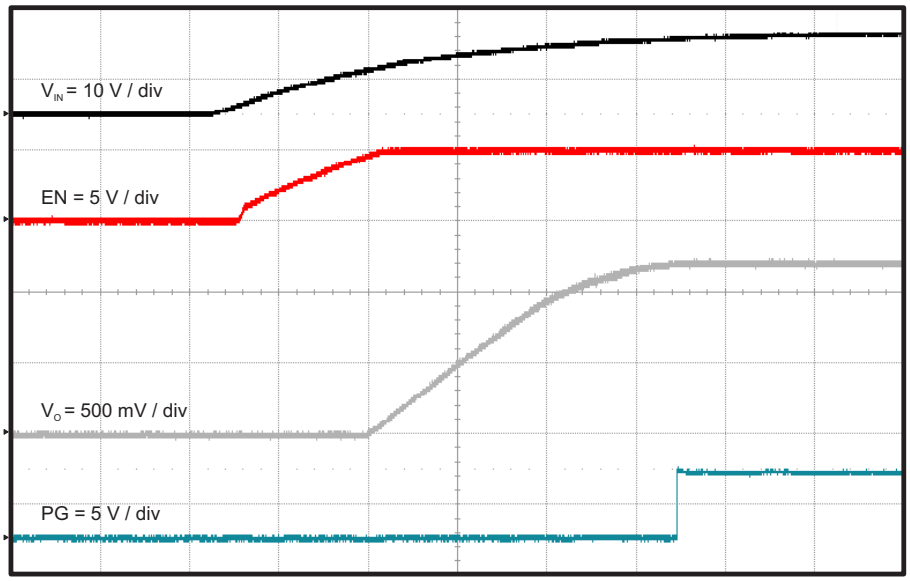

Figure 14. TPS56C215EVM-762 Start-Up Relative to V_{IN}

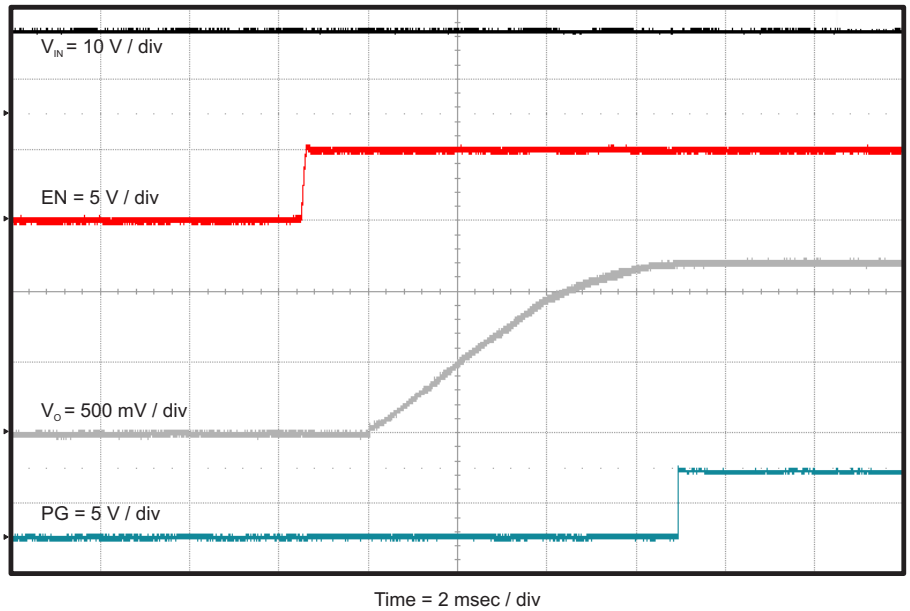

Figure 15. TPS56C215EVM-762 Start-Up Relative to Enable

2.10 Powering Down

Figure 16 and Figure 17 show the shutdown waveforms for the TPS56C215EVM-762. The input voltage for these plots is 12 V and the load is 1 Ω.

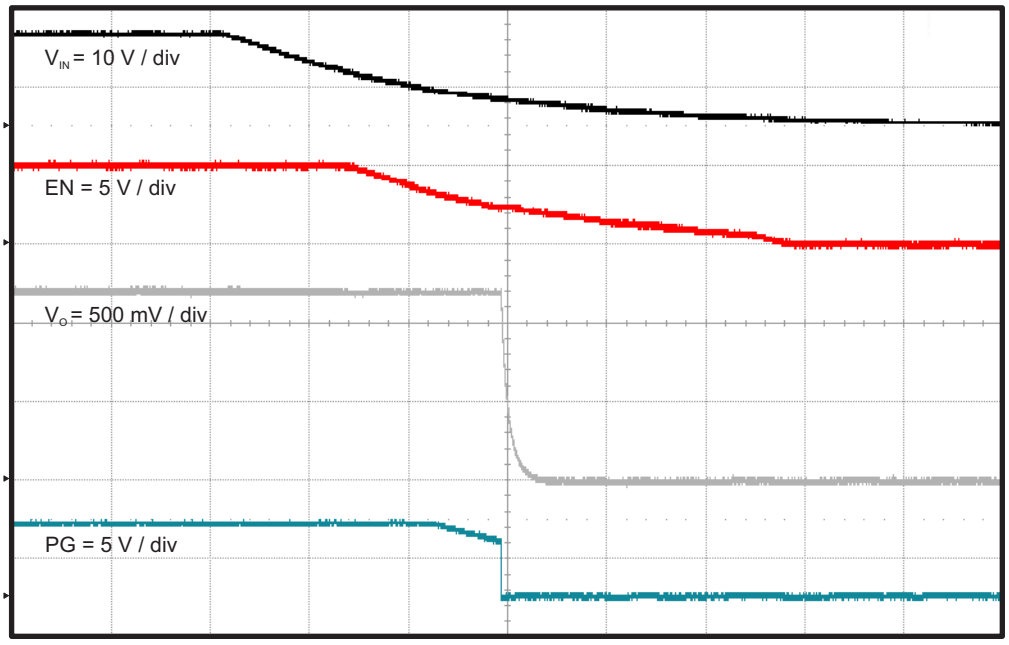

Figure 16. Shutdown Relative to V_{IN}

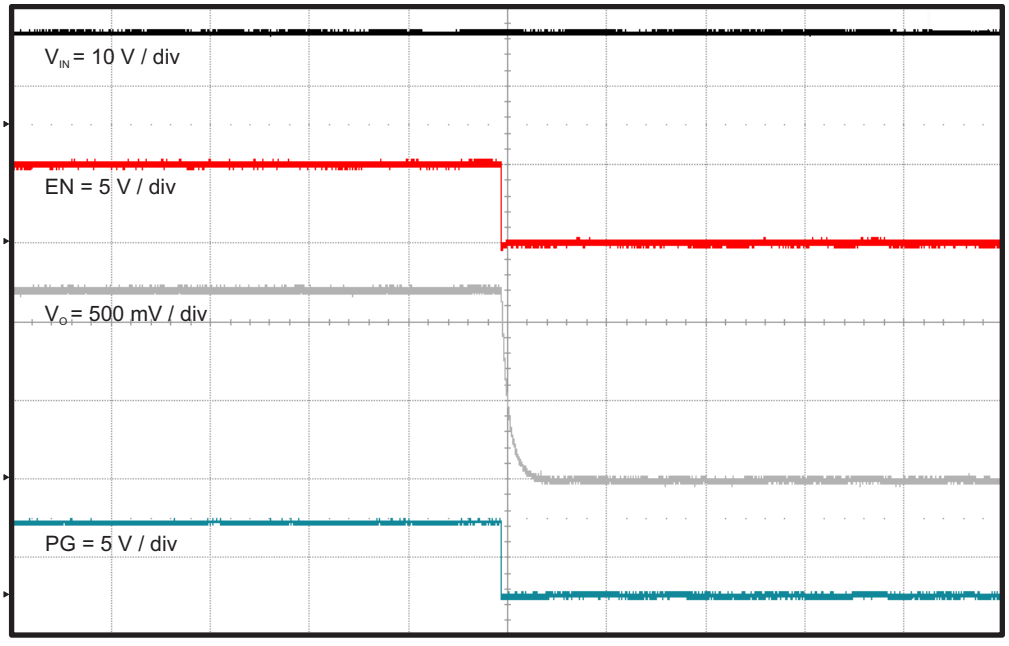

Figure 17. Shutdown Relative to Enable

3 Board Layout

This section provides a description of the TPS56C215EVM-762 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS56C215EVM-762 is shown in Figure 18 through Figure 22. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for VIN, VOUT, and SW. Also on the top layer are connections for the remaining pins of the TPS56C215 and the majority of the signal traces. There is a large area filled with ground. The internal layer-1 is dedicated ground plane with an island for quiet analog ground that is connected to the main power ground plane at a single point. The internal layer-2 contains an additional large ground copper area as well as an additional VIN and VOUT copper fill. The bottom layer is another ground plane with two additional traces for the output voltage feedback and BST capacitor connection. The top-side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board.

The input decoupling capacitors and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage setpoint resistor divider components are kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the TP9 test point. For the TPS56C215, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. Critical analog circuits such as the voltage set point divider, EN resistor, SS capacitor, MODE resistor, and AGND pin are terminated to quiet analog ground island on the internal layer-1.

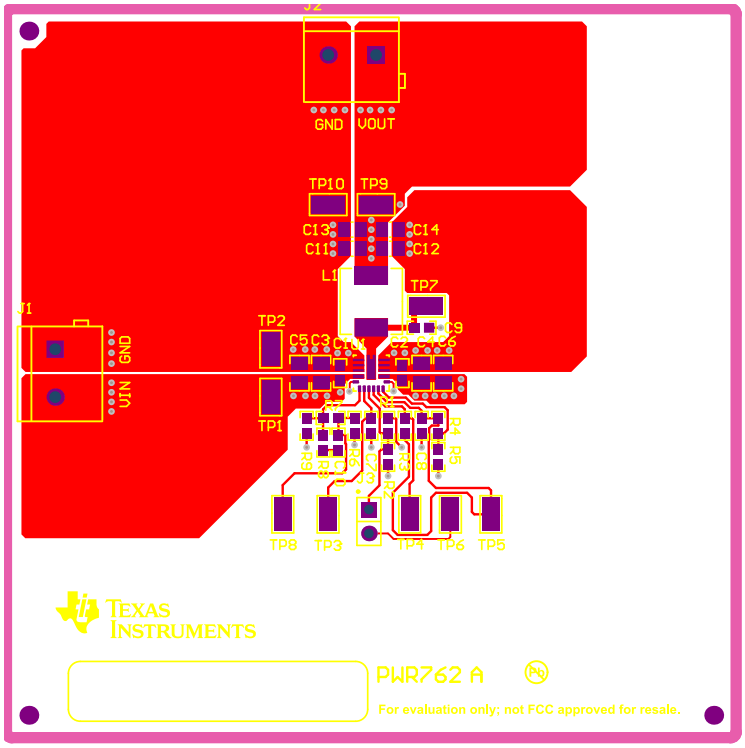

Figure 18. TPS56C215EVM-762 Top-Side Assembly

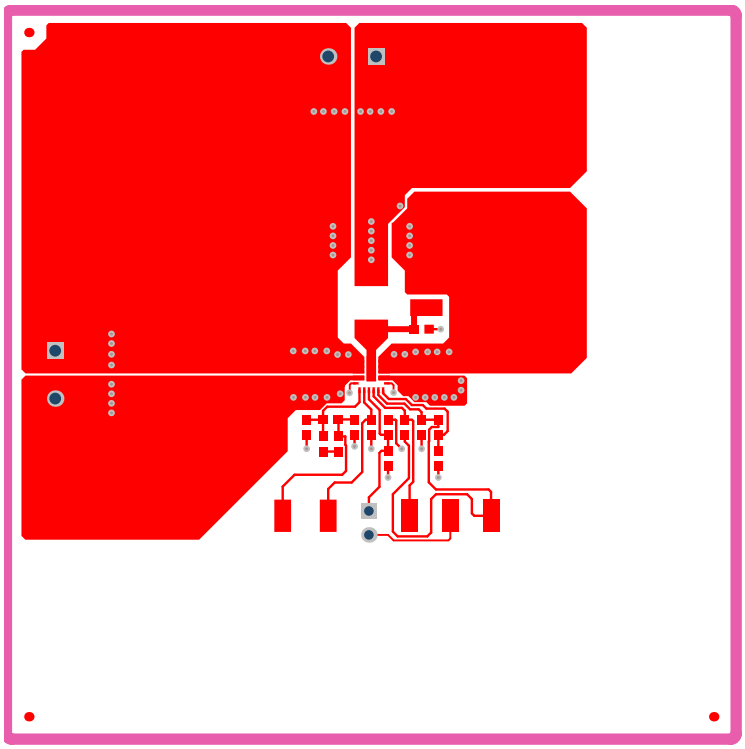

Figure 19. TPS56C215EVM-762 Top-Side Layout

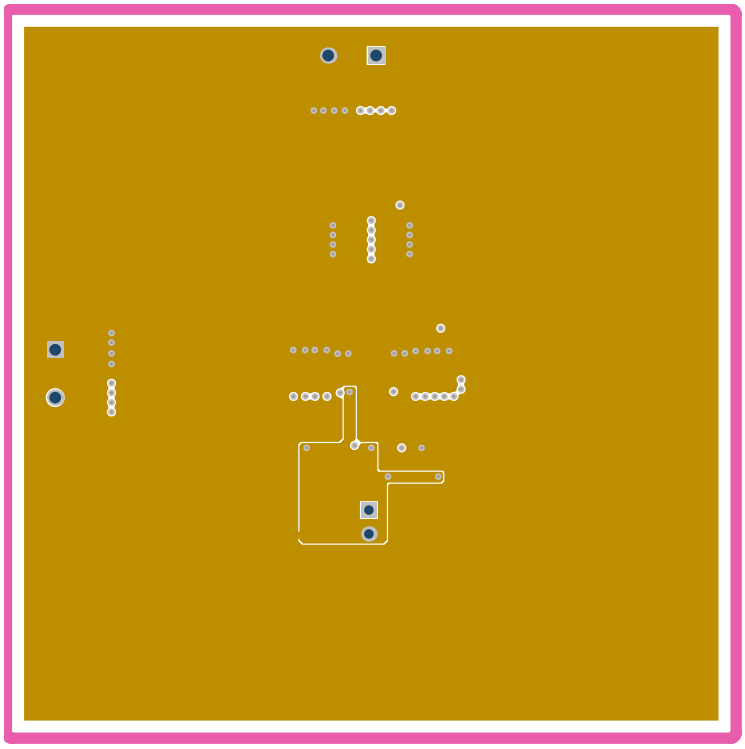

Figure 20. TPS56C215EVM-762 Internal Layer-1 Layout

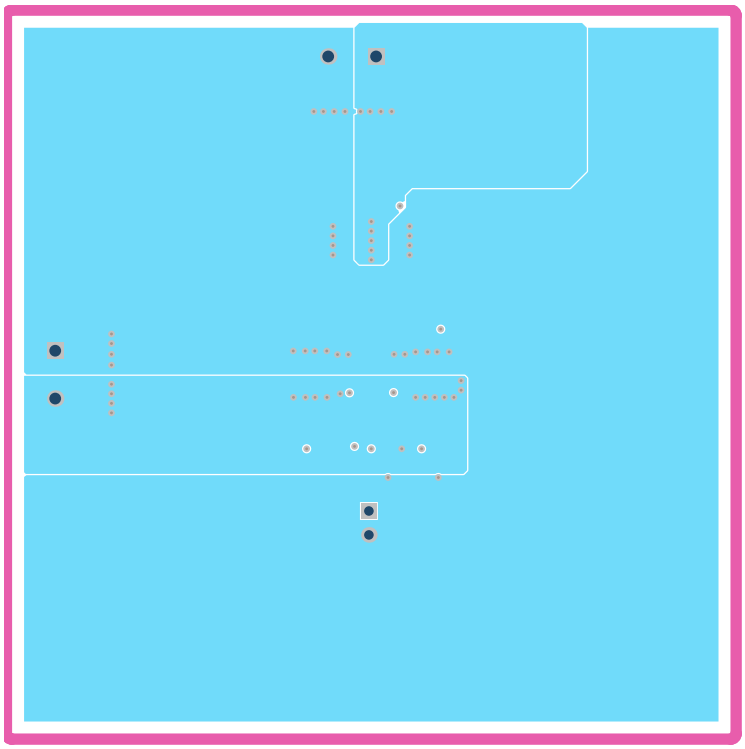

Figure 21. TPS56C215EVM-762 Internal Layer-2 Layout

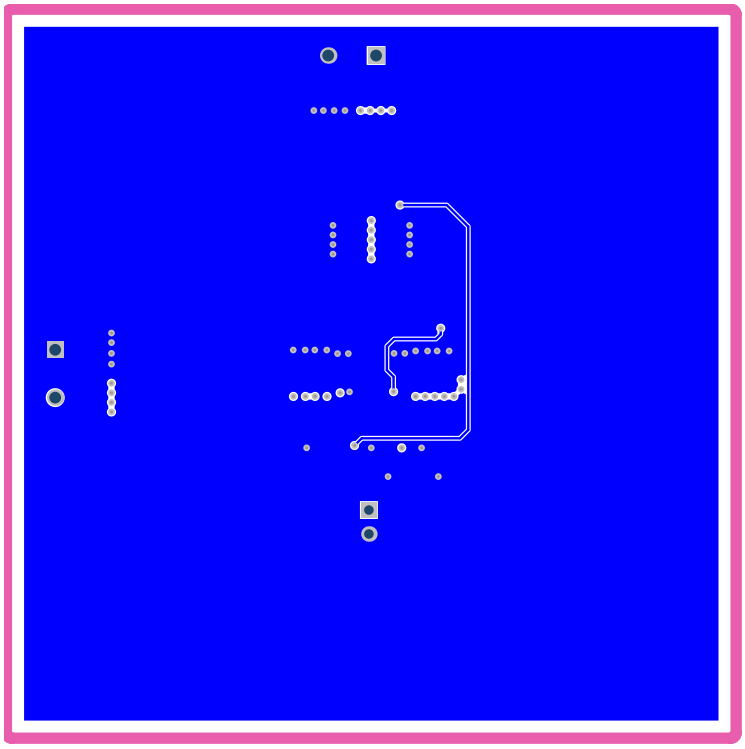

Figure 22. TPS56C215EVM-762 Bottom-Side Layout

4 Schematic and Bill of Materials

This section presents the TPS56C215EVM-762 schematic and bill of materials.

4.1 Schematic

Figure 23 is the schematic for the TPS56C215EVM-762.

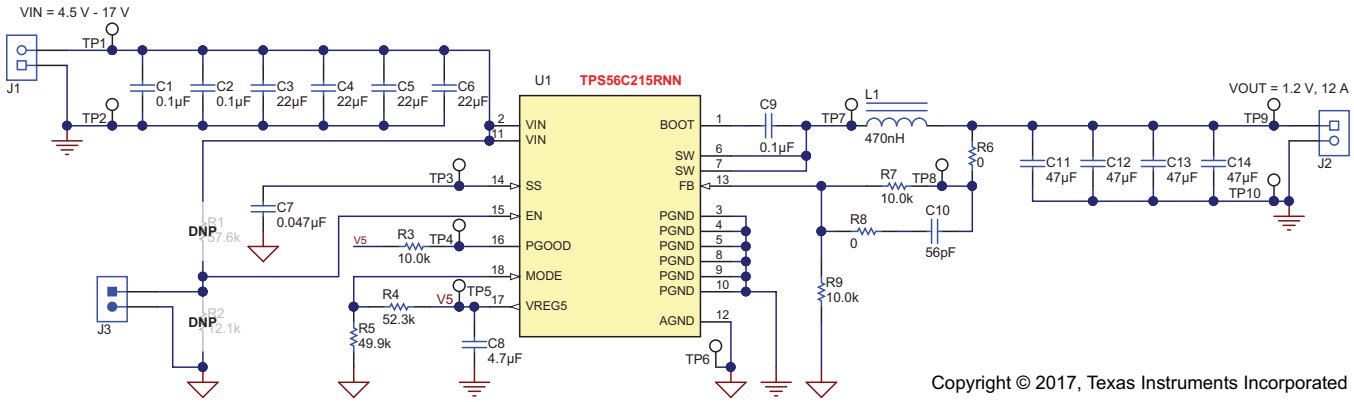

Figure 23. TPS56C215EVM-762 Schematic

4.2 Bill of Materials

Table 4 presents the bill of materials for the TPS56C215EVM-762.

Table 4. TPS56C215EVM-762 Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		PWR762	Any
C1, C2, C9	3	0.1uF	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E104KA01D	Murata
C3, C4, C5, C6	4	22uF	CAP, CERM, 22 µF, 35 V, +/- 20%, X5R, 0805	0805	C2012X5R1V226M125AC	TDK
C7	1	0.047uF	CAP, CERM, 0.047 µF, 50 V, +/- 10%, X7R, 0603	0603	GRM188R71H473KA61D	Murata
C8	1	4.7uF	CAP, CERM, 4.7 µF, 10 V, +/- 20%, X5R, 0603	0603	GRM188R61A475ME15	Murata
C10	1	56pF	CAP, CERM, 56 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H560JA01D	Murata
C11, C12, C13, C14	4	47uF	CAP, CERM, 47 µF, 10 V, +/- 20%, X5R, 0805	0805	GRM21BR61A476ME15	Murata
J1, J2	2		TERMINAL BLOCK 5.08MM VERT 2POS, TH		ED120/2DS	On-Shore Technology
J3	1		Header, 100mil, 2x1, Gold, TH		HTSW-102-07-G-S	Samtec
L1	1	470nH	Inductor, Shielded Drum Core, Powdered Iron, 470 nH, 17.5 A, 0.004 ohm, SMD	IHLP-2525CZ	IHLP2525CZERR47M01	Vishay-Dale
LBL1	1		Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	PCB Label 1.25"H x 0.250"W	THT-13-457-10	Brady
R3, R7, R9	3	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R4	1	52.3k	RES, 52.3 k, 1%, 0.1 W, 0603	0603	CRCW060352K3FKEA	Vishay-Dale
R5	1	49.9k	RES, 49.9 k, 1%, 0.1 W, 0603	0603	CRCW060349K9FKEA	Vishay-Dale
R6, R8	2	0	RES, 0, 5%, 0.1 W, 0603	0603	MCR03EZPJ000	Rohm
SH-J3	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	10	SMT	Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone
U1	1		4.5V to 17V Input, 12A Synchronous Step-Down Converter, RNN0017A	RNN0017A	TPS56C215RNNR	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
R1	0	57.6k	RES, 57.6 k, 1%, 0.1 W, 0603	0603	CRCW060357K6FKEA	Vishay-Dale
R2	0	12.1k	RES, 12.1 k, 1%, 0.1 W, 0603	0603	CRCW060312K1FKEA	Vishay-Dale

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (April 2016) to B Revision	Page
• Changed pin 17 and pin 18 in the *TPS56C215EVM-762 Schematic*.	16

Revision History

Changes from Original (March 2016) to A Revision	Page
• Changed Figure 23	16

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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