

# LM5160-Q1 Wide Input 65-V, 2-A Synchronous Buck / Fly-Buck™ DC/DC Converter

## 1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Temperature Grade 1:  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$
  - HBM ESD Classification Level 2
  - CDM ESD Classification Level C5
- Wide 4.5-V to 65-V Input Voltage Range
- Integrated High-Side and Low-Side Switches
  - No External Schottky Diode Required
- 2-A Maximum Load Current
- Meets CISPR 25 EMI Standard
- Adaptive Constant On-Time Control
  - No External Loop Compensation
  - Fast Transient Response
- Selectable Forced PWM or DCM Operation
  - FPWM Supports Multi-Output Fly-Buck™
- Nearly Constant Switching Frequency
  - Resistor Adjustable up to 1 MHz
- Programmable Soft-Start Time
- Prebiased Start-Up
- $\pm 1\%$  Feedback Voltage Reference
- Inherent Protection Features for Robust Design
  - Peak Current Limiting Protection
  - Adjustable Input UVLO and Hysteresis
  - VCC and Gate Drive UVLO Protection
  - Thermal Shutdown Protection With Hysteresis
- 14-Pin HTSSOP Package, 0.65-mm Pitch
- Create a Custom Design Using the LM5160-Q1 With the [WEBENCH® Power Designer](#)

## 2 Applications

- Automotive DC/DC Converter
- IGBT Gate Drive Bias Supply
- Low-Power Isolated DC/DC (Fly-Buck)

## 3 Description

The LM5160-Q1 is a 65-V, 2-A synchronous step-down converter with integrated high-side and low-side MOSFETs. The adaptive constant on-time control scheme requires no loop compensation and supports high step-down ratios with fast transient response. An internal feedback amplifier maintains  $\pm 1\%$  output voltage regulation over the entire operating temperature range. The on-time varies inversely with input voltage resulting in nearly constant switching frequency.

Peak and valley current limit circuits protect against overload conditions. The undervoltage lockout (EN/UVLO) circuit provides independently adjustable input undervoltage threshold and hysteresis. The LM5160-Q1 is programmed through the FPWM pin to operate in continuous conduction mode (CCM) from no load to full load or to automatically switch to discontinuous conduction mode (DCM) at light load for higher efficiency. Forced CCM operation supports multiple-output and isolated Fly-Buck applications using a coupled inductor.

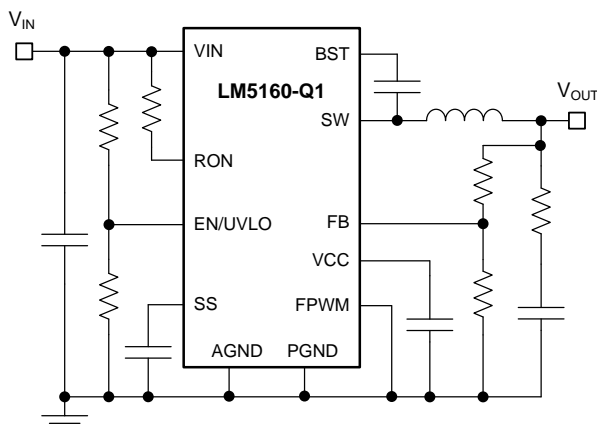
The LM5160-Q1 is qualified to automotive AEC-Q100 grade 1 and is available in 14-pin HTSSOP package with 0.65-mm pin pitch.

### Device Information<sup>(1)</sup>

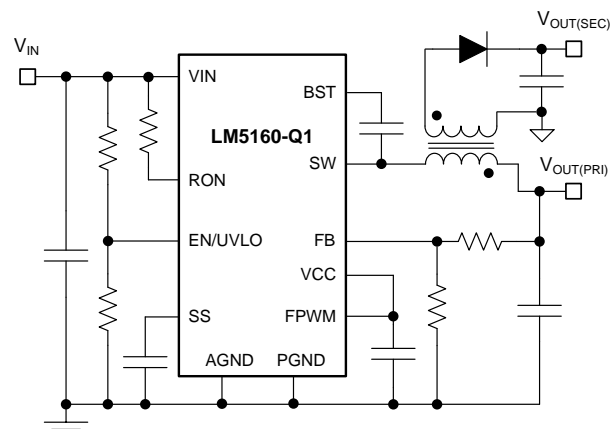
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5160-Q1	HTSSOP (14)	4.40 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Typical Synchronous Buck Application Circuit



### Typical Fly-Buck Application Circuit



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## 4 Revision History

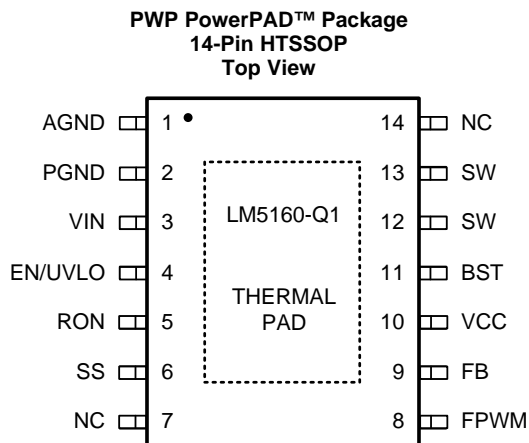
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (November 2017) to Revision C</b>	<b>Page</b>
• Changed <i>Features</i> .....	1
• Changed front page schematics.....	1
• Changed <i>Pinout Drawing</i> .....	3
• Changed <i>ESD Ratings</i> .....	4
• Changed <i>Function Block Diagram</i> .....	10
• Changed <i>Power Supply Recommendations</i> .....	25
• Changed <i>Related Documentation</i> .....	27

<b>Changes from Revision A (November 2015) to Revision B</b>	<b>Page</b>
• Updated AEC-Q100 qualified bullet points.....	1
• Deleted the lead temperature from the <i>Absolute Maximum Ratings</i> table .....	4
• Moved the <i>Ripple Configuration</i> section to the <i>Application Information</i> section .....	15
• Changed the <i>Application Performance Plots</i> title to <i>Application Curves</i> in both typical application sections .....	20
• Added layout details with LM5160-Q1 HTSSOP-14 package .....	26
• Changed the <i>Electrostatic Discharge Caution</i> statement.....	28

<b>Changes from Original (July 2015) to Revision A</b>	<b>Page</b>
• Changed current limit off-timer in the Electrical Characteristics to 16.....	5

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	AGND	—	Analog Ground. Ground connection of internal control circuits.
2	PGND	P	Power Ground. Ground connection of the internal synchronous rectifier FET.
3	VIN	P	Input supply connection. Operating input range is 4.5 V to 65 V.
4	EN/UVLO	I	Precision enable. Input pin of undervoltage lockout (UVLO) comparator.
5	RON	I	On-time programming pin. A resistor between this pin and VIN sets the switch on-time as a function of input voltage.
6	SS	I	Soft-start. Connect a capacitor from SS to AGND to control output rise time and limit overshoot.
8	FPWM	I	Forced PWM logic input pin. Connect to AGND for discontinuous conduction mode (DCM) with light loads. Connect to VCC for continuous conduction mode (CCM) at all loads and Fly-Buck configuration.
9	FB	I	Feedback input of voltage regulation comparator.
10	VCC	O	Internal high voltage start-up regulator bypass capacitor pin.
11	BST	P	Bootstrap capacitor pin. Connect a capacitor between BST and SW to bias gate driver of high-side buck FET.
12,13	SW	P	Switch node. Source connection of high-side buck FET and drain connection of low-side synchronous rectifier FET.
7,14	NC	—	No Connection.
—	EP	—	Exposed Pad. Connect to AGND and printed-circuit board ground plane to improve power dissipation.

(1) P = Power, G = Ground, I = Input, O = Output.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature of  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  (unless otherwise noted).<sup>(1)(2)</sup>

		MIN	MAX	UNIT
Input voltages	V <sub>IN</sub> to AGND	-0.3	70	V
	EN/UVLO to AGND	-0.3	70	
	RON to AGND	-0.3	70	
	BST to AGND	-0.3	84	
	VCC to AGND	-0.3	14	
	FPWM to AGND	-0.3	14	
	SS to AGND	-0.3	7	
	FB to AGND	-0.3	7	
Output voltages	BST to SW	-0.3	14	V
	BST to VCC		70	
	SW to AGND	-1.5	70	
	SW to AGND (20-ns transient)	-3		
Operating junction temperature, T <sub>J</sub> <sup>(3)</sup>		-40	150	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than  $125^{\circ}\text{C}$ .

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	
		All pins		

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

Over the recommended operating junction temperature of  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  (unless otherwise noted).<sup>(1)</sup>

	MIN	MAX	UNIT
V <sub>IN</sub> input voltage	4.5	65	V
I <sub>OUT</sub> output current		2	A
Operating junction temperature	-40	150	°C

- (1) *Recommended Operating Ratings* are conditions under the device is intended to be functional. For specifications and test conditions, see [Electrical Characteristics](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM5160-Q1	UNIT
		PWP (HTSSOP)	
		14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	39.3	°C/W
R <sub>θJCb</sub>	Junction-to-case (bottom) thermal resistance	2.0	°C/W
ψ <sub>JB</sub>	Junction-to-board thermal characteristic parameter	19.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	19.6	°C/W
R <sub>θJc</sub>	Junction-to-case (top) thermal resistance	22.8	°C/W
ψ <sub>JT</sub>	Junction-to-top thermal characteristic parameter	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) report.

## 6.5 Electrical Characteristics

Typical values correspond to T<sub>J</sub> = 25°C. Minimum and maximum limits apply over T<sub>J</sub> = –40°C to 125°C. Unless otherwise stated, V<sub>IN</sub> = 24 V. <sup>(1)(2)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
I <sub>SD</sub>	Input shutdown current	V <sub>IN</sub> = 24 V, V <sub>EN/UVLO</sub> = 0 V		50	90.7	μA
I <sub>OP</sub>	Input operating current	V <sub>IN</sub> = 24 V, V <sub>FB</sub> = 3 V, non-switching		2.3	2.84	mA
<b>VCC SUPPLY</b>						
V <sub>CC</sub>	Bias regulator output	V <sub>IN</sub> = 24 V, I <sub>CC</sub> = 20 mA	6.47	7.5	8.52	V
V <sub>CC</sub>	Bias regulator current limit	V <sub>IN</sub> = 24 V	30			mA
V <sub>CC(UV)</sub>	VCC undervoltage threshold	V <sub>VCC</sub> rising		3.98	4.1	V
V <sub>CC(HYS)</sub>	VCC undervoltage hysteresis	V <sub>VCC</sub> falling		185		mV
V <sub>CC(LDO)</sub>	VIN – VCC dropout voltage	V <sub>IN</sub> = 4.5 V, I <sub>VCC</sub> = 20 mA		165	260	mV
<b>HIGH-SIDE FET</b>						
R <sub>DS(ON)</sub>	High-side on-state resistance	V <sub>BST</sub> – V <sub>SW</sub> = 7 V, I <sub>SW</sub> = 1 A		0.29		Ω
BST <sub>(UV)</sub>	Bootstrap gate drive UV	V <sub>BST</sub> – V <sub>SW</sub> rising		2.93	3.6	V
BST <sub>(HYS)</sub>	Gate drive UV hysteresis	V <sub>BST</sub> – V <sub>SW</sub> falling		200		mV
<b>LOW-SIDE FET</b>						
R <sub>DS(ON)</sub>	Low-side on-state resistance	I <sub>SW</sub> = 1 A		0.13		Ω
<b>HIGH-SIDE CURRENT LIMIT</b>						
I <sub>LIM(HS)</sub>	High-side current limit threshold		2.125	2.5	2.875	A
T <sub>RES</sub>	Current limit response time	I <sub>LIM(HS)</sub> threshold detect to FET turnoff		100		ns
T <sub>OFF1</sub>	Current limit forced off-time	V <sub>FB</sub> = 0 V, V <sub>IN</sub> = 65 V	16	29	39.8	μs
T <sub>OFF2</sub>	Current limit forced off-time	V <sub>FB</sub> = 1 V, V <sub>IN</sub> = 24 V	2.18	3.5	5.12	μs
<b>LOW-SIDE CURRENT LIMIT</b>						
I <sub>SOURCE(LS)</sub>	Sourcing current limit		1.9	2.5	3	A
I <sub>SINK(LS)</sub>	Sinking current limit			5.4		A
<b>DIODE EMULATION</b>						
V <sub>FPWM(LOW)</sub>	FPWM input logic low	V <sub>IN</sub> = 24 V			1	V
V <sub>FPWM(HIGH)</sub>	FPWM input logic high	V <sub>IN</sub> = 24 V	3			V
I <sub>ZX</sub>	Zero cross detect current	FPWM = AGND (diode emulation)		0		mA
<b>REGULATION COMPARATOR</b>						
V <sub>REF</sub>	FB regulation level	V <sub>IN</sub> = 24 V	1.975	1.995	2.015	V
I <sub>(Bias)</sub>	FB input bias current	V <sub>IN</sub> = 24 V			100	nA

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) The junction temperature (T<sub>J</sub> in °C) is calculated from the ambient temperature (T<sub>A</sub> in °C) and power dissipation (P<sub>D</sub> in Watts) as follows: T<sub>J</sub> = T<sub>A</sub> + (P<sub>D</sub> • R<sub>θJA</sub>) where R<sub>θJA</sub> (in °C/W) is the package thermal impedance provided in [Thermal Information](#).

## Electrical Characteristics (continued)

Typical values correspond to  $T_J = 25^\circ\text{C}$ . Minimum and maximum limits apply over  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ . Unless otherwise stated,  $V_{IN} = 24\text{ V}$ .<sup>(1)(2)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ERROR CORRECTION AMPLIFIER and SOFT START</b>						
$G_M$	Error amp transconductance	$V_{FB} = V_{REF} \pm 10\text{ mV}$		105		$\mu\text{A/V}$
$I_{EA(\text{Source})}$	Error amp source current	$V_{FB} = 1\text{ V}, V_{SS} = 1\text{ V}$	7.62	10.2	12.51	$\mu\text{A}$
$I_{EA(\text{Sink})}$	Error amp sink current	$V_{FB} = 5\text{ V}, V_{SS} = 2.25\text{ V}$	7.46	10	12.2	$\mu\text{A}$
$V_{(SS-FB)}$	$V_{SS} - V_{FB}$ clamp voltage	$V_{FB} = 1.75\text{ V}, C_{SS} = 1\text{ nF}$		135		mV
$I_{SS}$	Soft-start charging current	$V_{SS} = 0.5\text{ V}$	7.63	10.2	12.5	$\mu\text{A}$
<b>ENABLE/UVLO</b>						
$V_{UVLO(\text{TH})}$	UVLO threshold	$V_{EN/UVLO}$ rising	1.213	1.24	1.277	V
$I_{UVLO(\text{HYS})}$	UVLO hysteresis current	$V_{EN/UVLO} = 1.4\text{ V}$	15	20	25	$\mu\text{A}$
$V_{SD(\text{TH})}$	Shutdown mode threshold	$V_{EN/UVLO}$ falling	0.28	0.35		V
$V_{SD(\text{HYS})}$	Shutdown threshold hysteresis	$V_{EN/UVLO}$ rising		47		mV
<b>THERMAL SHUTDOWN</b>						
$T_{SD}$	Thermal shutdown threshold			175		$^\circ\text{C}$
$T_{SD(\text{HYS})}$	Thermal shutdown hysteresis			20		$^\circ\text{C}$

## 6.6 Switching Characteristics

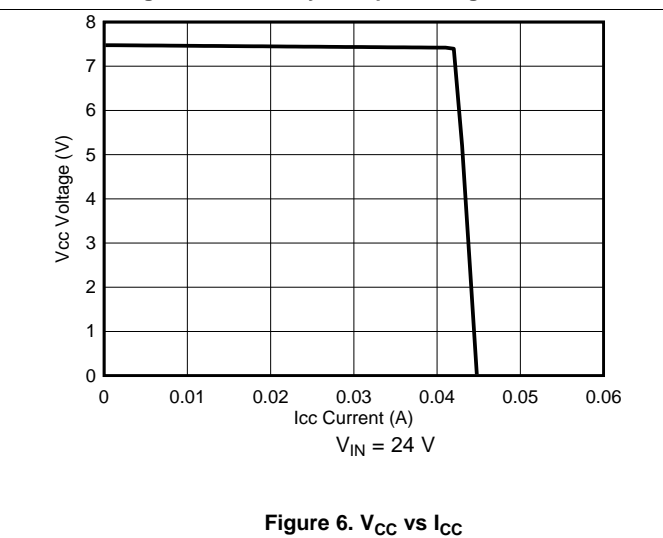
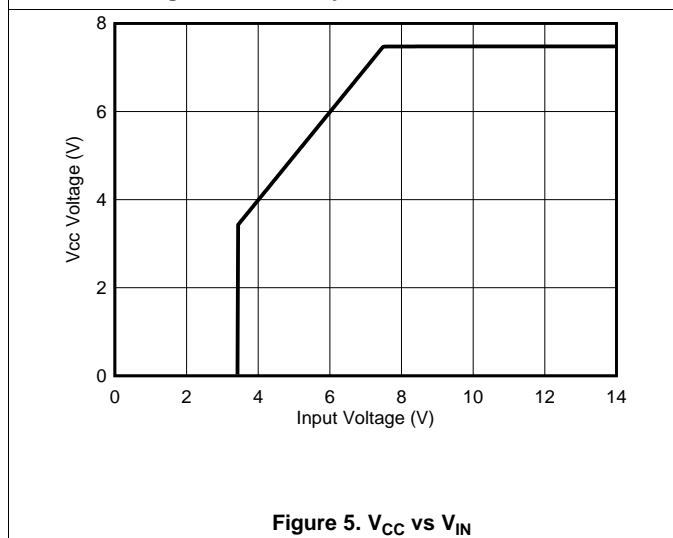
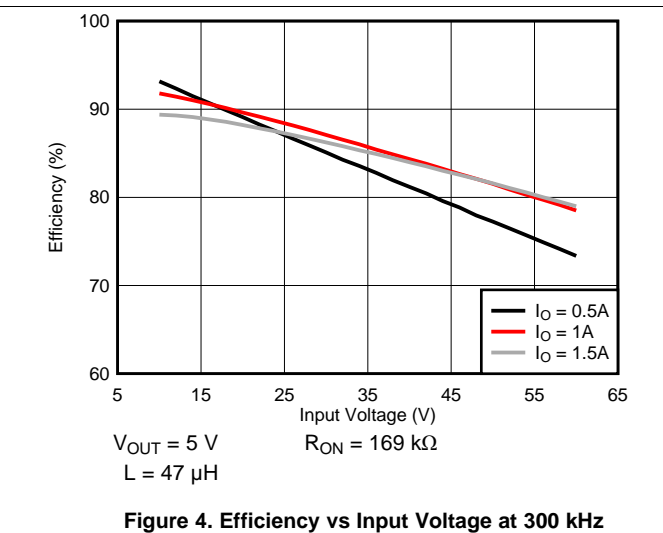
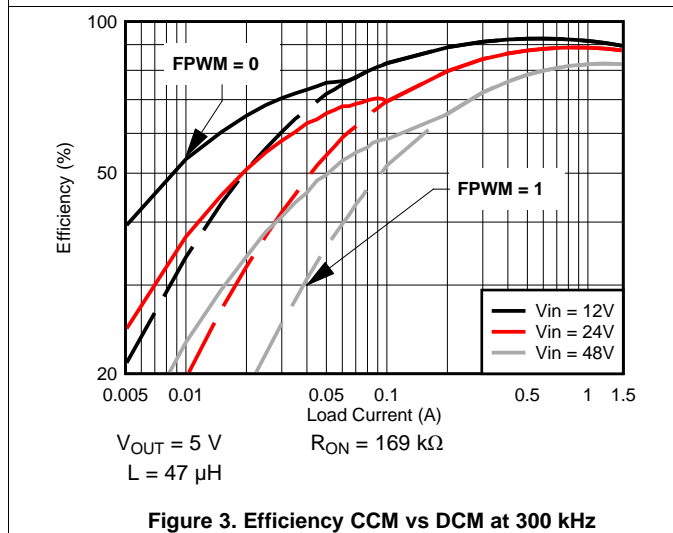
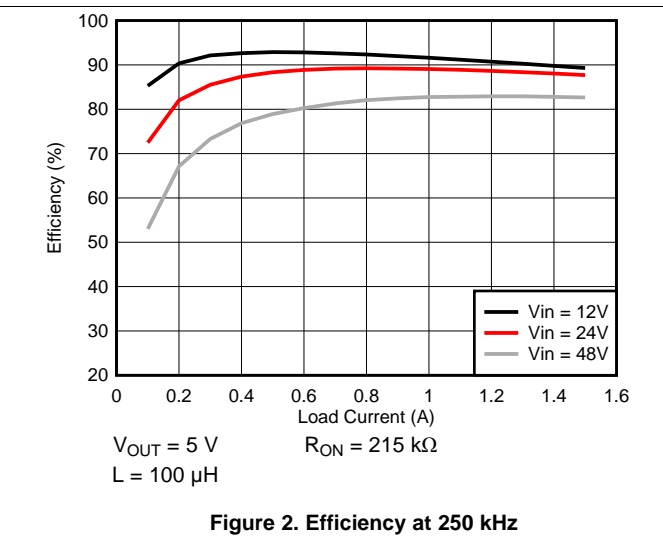
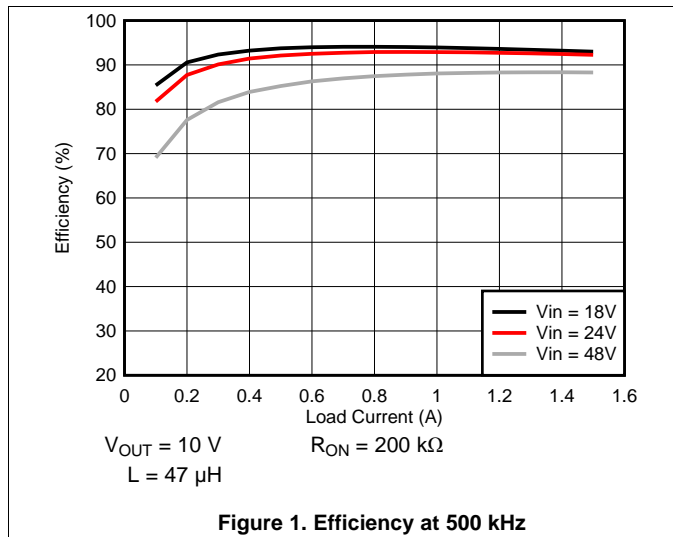
Typical values correspond to  $T_J = 25^\circ\text{C}$ . Minimum and maximum limits apply over  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ . Unless otherwise stated,  $V_{IN} = 24\text{ V}$ .<sup>(1)</sup>

		MIN	TYP	MAX	UNIT
<b>MINIMUM OFF-TIME</b>					
$T_{\text{OFF-MIN}}$	Minimum off-time, $V_{FB} = 0\text{ V}$		170		ns
<b>ON-TIME GENERATOR</b>					
$T_{\text{ON1}}$	$V_{IN} = 24\text{ V}, R_{\text{ON}} = 100\text{ k}\Omega$	312	428	520	ns
$T_{\text{ON2}}$	$V_{IN} = 24\text{ V}, R_{\text{ON}} = 200\text{ k}\Omega$	625	818	1040	ns
$T_{\text{ON3}}$	$V_{IN} = 8\text{ V}, R_{\text{ON}} = 100\text{ k}\Omega$	937	1247	1563	ns
$T_{\text{ON4}}$	$V_{IN} = 65\text{ V}, R_{\text{ON}} = 100\text{ k}\Omega$	132	176	220	ns

- (1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

### 6.7 Typical Characteristics

T<sub>A</sub> = 25°C, unless otherwise noted. Please refer to [Typical Applications](#) for circuit designs.



Typical Characteristics (continued)

T<sub>A</sub> = 25°C, unless otherwise noted. Please refer to [Typical Applications](#) for circuit designs.

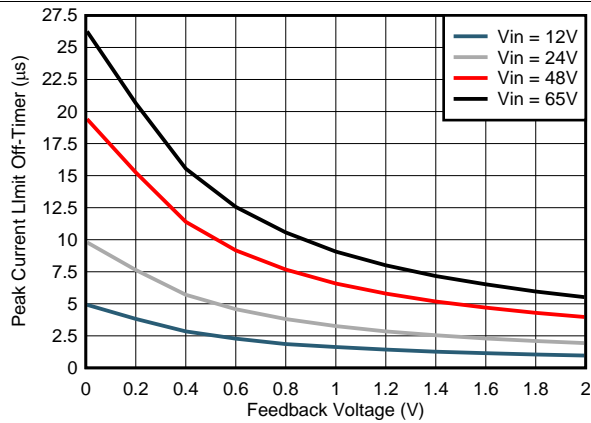


Figure 7. T<sub>OFF</sub> (I<sub>LIM</sub>) vs V<sub>FB</sub>

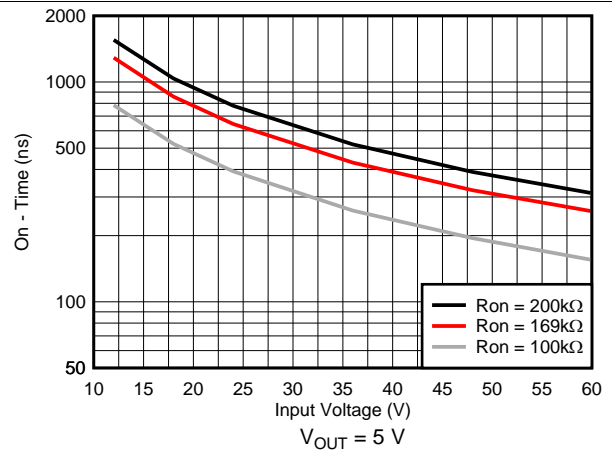


Figure 8. T<sub>ON</sub> vs V<sub>IN</sub>

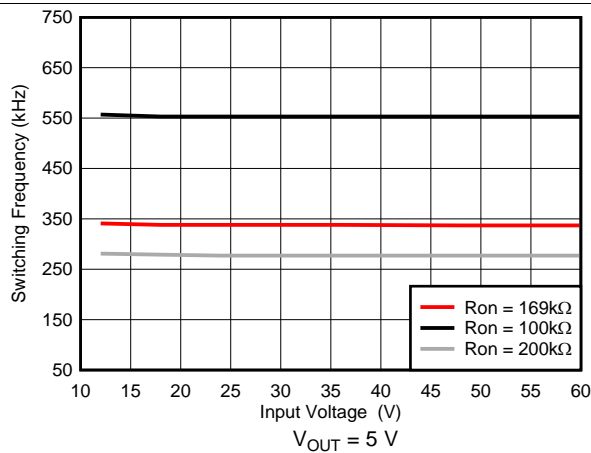


Figure 9. Switching Frequency vs V<sub>IN</sub>

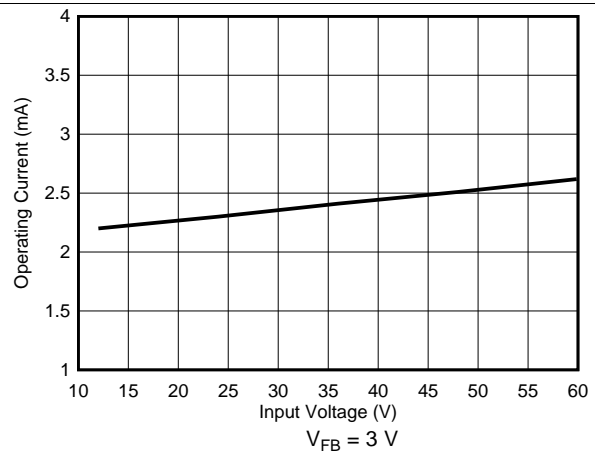


Figure 10. I<sub>IN</sub> vs V<sub>IN</sub> (Operating, Non-Switching)

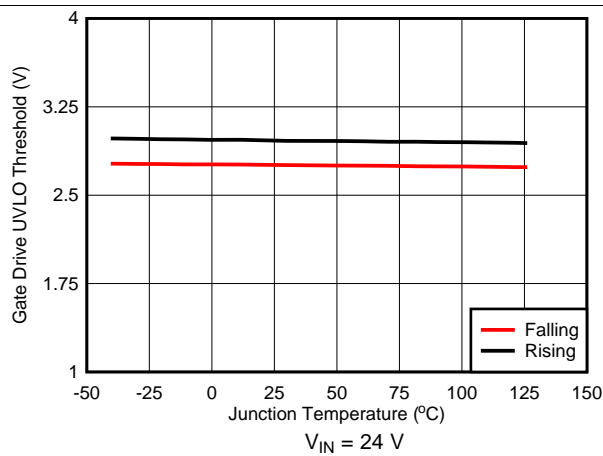


Figure 11. Gate Drive UVLO vs Temperature

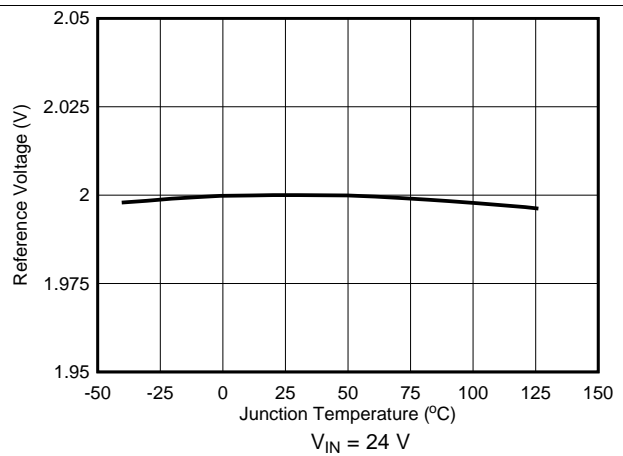


Figure 12. Reference Voltage vs Temperature



Typical Characteristics (continued)

T<sub>A</sub> = 25°C, unless otherwise noted. Please refer to [Typical Applications](#) for circuit designs.

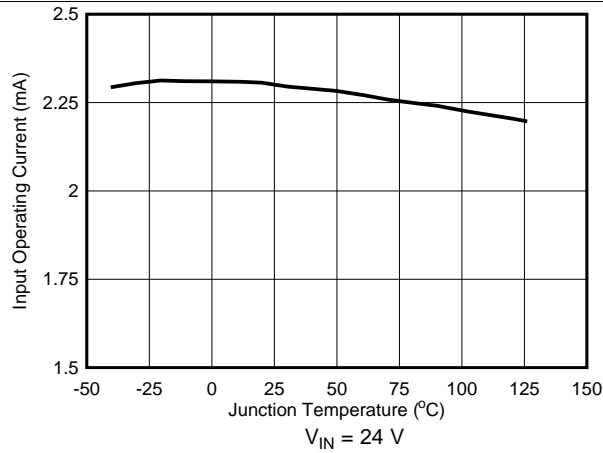


Figure 13. Input Operating Current vs Temperature

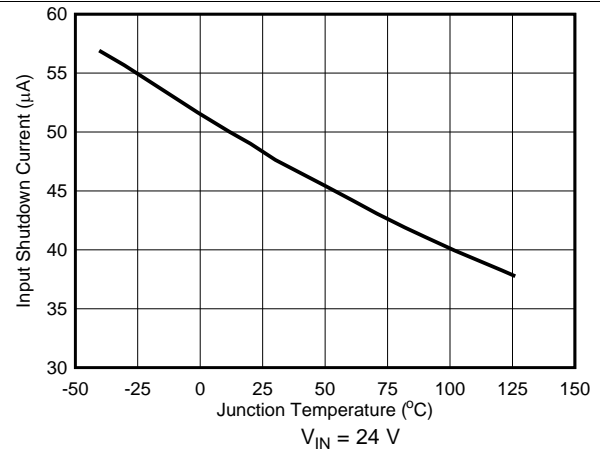


Figure 14. Input Shutdown Current vs Temperature

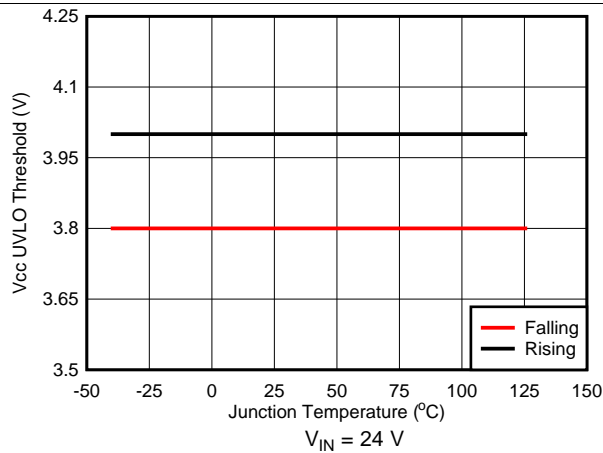


Figure 15. V<sub>CC</sub> UVLO vs Temperature

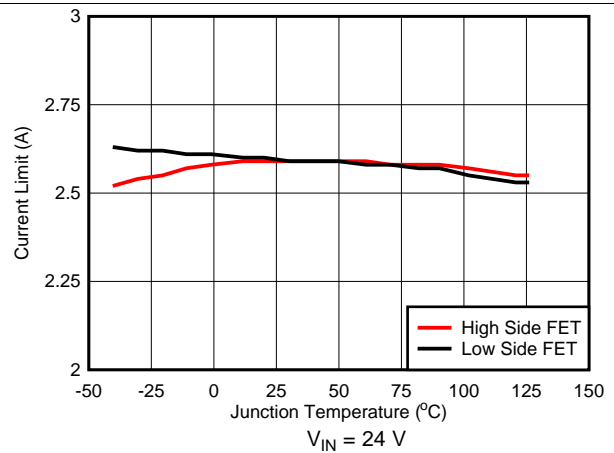


Figure 16. Current Limit vs Temperature

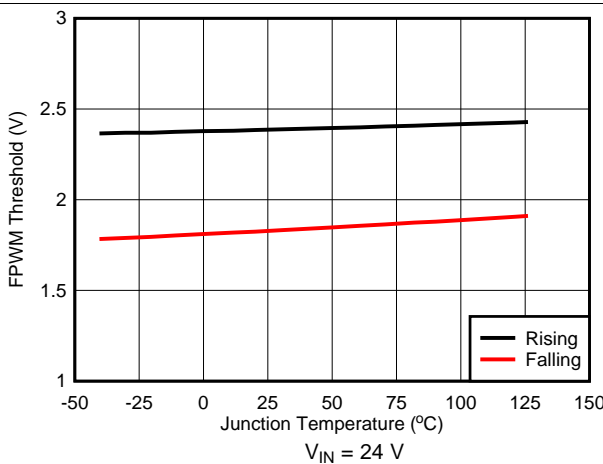


Figure 17. FPWM Threshold vs Temperature

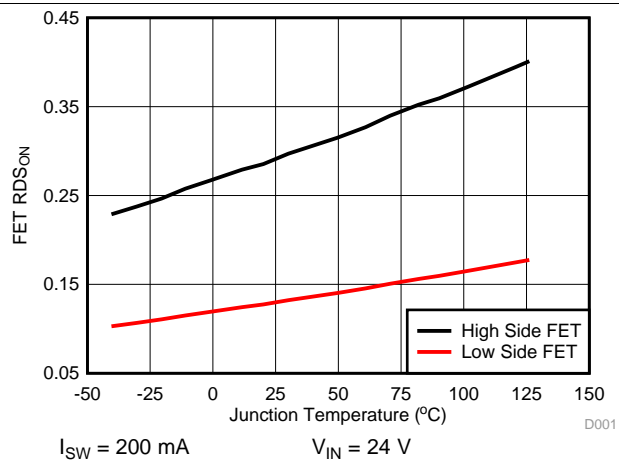


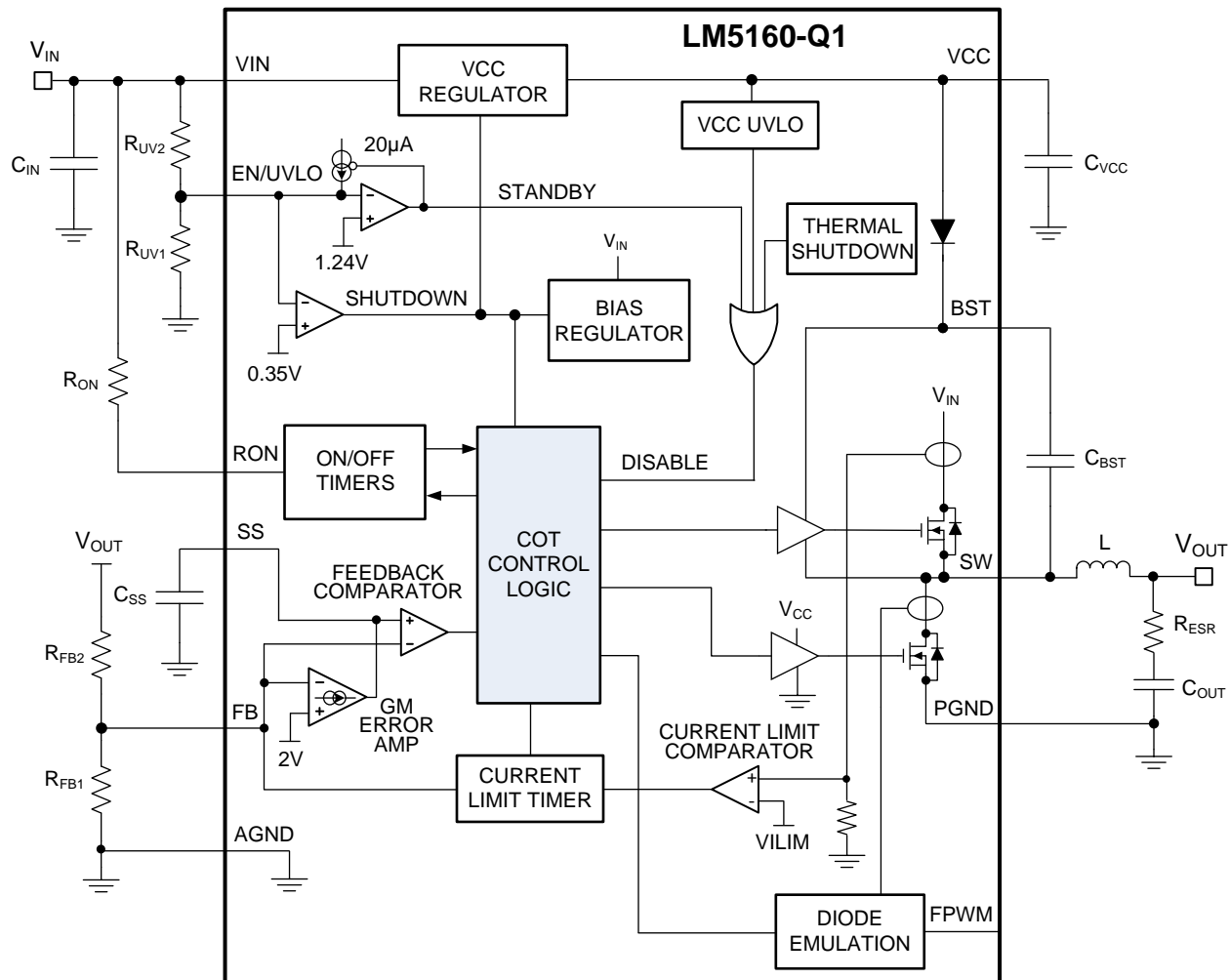
Figure 18. Switch Resistance vs Temperature

## 7 Detailed Description

### 7.1 Overview

The LM5160-Q1 step-down synchronous switching regulator features all the functions needed to implement a low-cost, efficient buck converter capable of supplying 2 A to the load. This high voltage regulator contains 65-V N-channel buck and synchronous rectifier switches and is available in a 14-pin HTSSOP package with 0.65-mm pin pitch. The regulator operation is based on an adaptive constant on-time control architecture where the on-time is inversely proportional to input voltage  $V_{IN}$ . This feature maintains a relatively constant operating frequency with load and input voltage variations. A constant on-time switching regulator requires no loop compensation resulting in fast load transient response. Peak current limit detection circuit is implemented with a forced off-time during current limiting which is inversely proportional to voltage at the feedback pin,  $V_{FB}$  and directly proportional to  $V_{IN}$ . Varying the current limit off-time with  $V_{FB}$  and  $V_{IN}$  ensures short-circuit protection with minimal current limit foldback. The LM5160-Q1 can be applied in numerous end equipment systems requiring efficient step-down regulation from higher input voltages. This regulator is well-suited for 24-V industrial systems as well as 48-V telecom and PoE voltage ranges. The LM5160-Q1 integrates an undervoltage lockout (EN/UVLO) circuit to prevent faulty operation of the device at low input voltages and features intelligent current limit and thermal shutdown to protect the device during overload or short circuit.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Control Circuit

The LM5160-Q1 step-down switching regulator employs a control principle based on a comparator and a one-shot timer, with the output voltage feedback (FB) compared to the voltage at the soft-start (SS) pin ( $V_{SS}$ ). If the FB voltage is below  $V_{SS}$ , the internal buck switch is turned on for a conduction time determined by the input voltage and the one-shot programming resistor ( $R_{ON}$ ). Following the on-time, the buck switch must stay off for the off-time forced by the minimum off-time one-shot. The buck switch remains off until the FB voltage falls below the SS voltage again, when it turns back on for another on-time interval.

During a rapid start-up or when the load current increases suddenly, the regulator operates with minimum off-time per cycle. When regulating the output in steady-state operation, the off-time automatically adjusts to produce the SW voltage duty cycle required for output voltage regulation.

When in regulation, the LM5160-Q1 operates in continuous conduction mode at heavy load currents. If FPWM is connected to ground or left floating, the regulator operates in discontinuous conduction mode at light load with the synchronous rectifier FET in diode emulation. With sufficient load, the LM5160-Q1 operates in continuous conduction mode with the inductor current never reaching zero during the off-time of the high-side FET. In this mode the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. The operating frequency is programmed by the resistor connected from VIN to  $R_{ON}$  and can be calculated from [Equation 1](#) with  $R_{ON}$  expressed in Ohms.

$$F_{sw} = \frac{V_{OUT}}{R_{ON} \times 1 \times 10^{-10}} \text{ Hz} \quad (1)$$

In discontinuous conduction mode, current through the inductor ramps up from zero to a peak value during the on-time, then ramps back to zero before the end of the off-time. The next on-time interval starts when the voltage at FB falls below  $V_{SS}$ . When the inductor current is zero during the high-side FET off-time, the load current is supplied by the output capacitor. In this mode, the operating switching frequency is lower than the continuous conduction mode switching frequency and the frequency varies with load. Discontinuous conduction mode maintains conversion efficiency at light loads because the switching losses reduce with the decrease in load and frequency.

The output voltage is set by two external resistors ( $R_{FB1}$ ,  $R_{FB2}$ ). Calculate the regulated output voltage from [Equation 2](#).

$$V_{OUT} = \frac{V_{REF} \times (R_{FB2} + R_{FB1})}{R_{FB1}} \text{ V}$$

where

- $V_{REF} = 2 \text{ V}$  (typical) is the feedback reference voltage. (2)

### 7.3.2 VCC Regulator

The LM5160-Q1 contains an internal high-voltage linear regulator with a nominal output voltage of 7.5 V (typical). The VCC regulator is internally current limited to 30 mA (minimum). This regulator supplies power to internal circuit blocks including the synchronous FET gate driver and the logic circuits. When the VCC voltage reaches the undervoltage lockout ( $V_{CC(UV)}$ ) threshold of 3.98 V (typical), the IC is enabled. An external capacitor at the VCC pin stabilizes the regulator and supplies transient VCC current to the gate drivers. An internal diode connected from VCC to BST replenishes the charge in the high-side gate drive bootstrap capacitor when the SW voltage is low.

## Feature Description (continued)

### 7.3.3 Regulation Comparator

The feedback voltage at the FB pin is compared to the SS pin voltage  $V_{SS}$ . In normal operation when the output voltage is in regulation, an on-time interval is initiated when the voltage at FB pin falls below  $V_{SS}$ . The high-side buck switch stays on for a pre-defined on-time causing the FB voltage to rise. After the on-time interval expires, the high-side switch remains off until the FB voltage falls below  $V_{SS}$ . During start-up, the FB voltage is below  $V_{SS}$  at the end of each on-time interval and the high-side switch turns on again after the minimum forced off-time of 170 ns (typical). When the output is shorted to ground ( $V_{FB} = 0$  V), the high-side peak current limit is triggered, the high-side FET is turned off and remains off for a period determined by the current limit off-timer. See [Current Limit](#) for additional information.

### 7.3.4 Soft Start

The soft-start feature of the LM5160-Q1 allows the converter to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. When the EN/UVLO voltage is above the EN/UVLO standby threshold  $V_{UVLO(TH)} = 1.24$  V (typical) and the VCC voltage exceeds the VCC undervoltage threshold,  $V_{CC(UV)} = 3.98$  V (typical), an internal 10- $\mu$ A current source charges the external capacitor at the SS pin ( $C_{SS}$ ) from 0 V to 2 V. The voltage at SS is the noninverting input of the internal FB comparator. The soft-start interval ends when the SS capacitor is charged to the 2-V reference level. The ramping voltage at SS produces a controlled, monotonic output voltage start-up. Use a minimum soft-start capacitance of 1 nF for all applications.

### 7.3.5 Error Amplifier

The LM5160-Q1 provides a transconductance ( $G_M$ ) error amplifier that minimizes the difference between the reference voltage ( $V_{REF}$ ) and the average feedback (FB) voltage. This amplifier reduces the load and line regulation errors that are common in constant on-time regulators. The soft-start capacitor  $C_{SS}$  provides compensation for this error correction loop. The soft-start capacitor must be greater than 1 nF to ensure stability.

### 7.3.6 On-Time Generator

The on-time of the LM5160-Q1 high-side MOSFET is determined by the  $R_{ON}$  resistor and is inversely proportional to the input voltage ( $V_{IN}$ ). The inverse relationship with  $V_{IN}$  results in a nearly constant frequency as  $V_{IN}$  is varied. Calculate the on-time from [Equation 3](#) with  $R_{ON}$  expressed in Ohms.

$$T_{ON} = \frac{R_{ON} \times 1 \times 10^{-10}}{V_{IN}} \text{ s} \quad (3)$$

To set a specific continuous conduction mode switching frequency ( $F_{SW}$  expressed in Hz), determine the  $R_{ON}$  resistor from [Equation 4](#).

$$R_{ON} = \frac{V_{OUT}}{F_{SW} \times 1 \times 10^{-10}} \Omega \quad (4)$$

$R_{ON}$  must be selected for a minimum on-time (at maximum  $V_{IN}$ ) greater than 150 ns for proper operation. This minimum on-time requirement limits the maximum switching frequency of applications with relatively high  $V_{IN}$  and low  $V_{OUT}$ .

### 7.3.7 Current Limit

The LM5160-Q1 provides an intelligent current limit off-timer that adjusts the off-time to reduce the foldback in the current limit. If the peak value of the current in the buck switch exceeds 2.5 A (typical), the present on-time interval is immediately terminated and a non-resettable off-timer is initiated. The length of the off-time is controlled by the FB voltage and the input voltage  $V_{IN}$ . As an example, when  $V_{FB} = 0$  V and  $V_{IN} = 24$  V, the off-time is set to 10  $\mu$ s. This condition occurs if the output is shorted or during the initial phase of start-up. In cases of output overload where the FB voltage is greater than zero volts (a soft short), the current limit off-time is reduced. Decreasing the off-time during less severe overloads reduces the current limit foldback, overload recovery time, and start-up time. Calculate the current limit off-time using [Equation 5](#).

$$T_{OFF(CL)} = \frac{5V_{IN}}{24V_{FB} + 12} \mu\text{s} \quad (5)$$

## Feature Description (continued)

### 7.3.8 N-Channel Buck Switch and Driver

The LM5160-Q1 integrates an N-channel buck switch and associated floating high-side gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage bootstrap diode. A 10-nF or larger ceramic capacitor connected between BST and SW provides the voltage to the high-side driver during the buck switch on-time. During the off-time, the SW node is pulled down to approximately 0 V and the bootstrap capacitor charges from VCC through the internal bootstrap diode. The minimum off-time of 170 ns (typical) provides a minimum time each cycle to recharge the bootstrap capacitor.

### 7.3.9 Synchronous Rectifier

The LM5160-Q1 provides an internal low-side synchronous rectifier N-channel FET. This low-side FET provides a low resistance path for the inductor current when the high-side FET is turned off.

With the FPWM pin connected to ground or left floating, the LM5160-Q1 synchronous rectifier operates in diode emulation mode. Diode emulation enables the pulse-skipping during light load conditions. This leads to a reduction in the average switching frequency at light loads. Switching losses and FET gate driver losses, both of which are proportional to switching frequency, are significantly reduced and efficiency is improved. This pulse-skipping mode also reduces the circulating inductor currents and losses associated with a continuous conduction mode (CCM).

When FPWM is pulled high, diode emulation is disabled. The inductor current can flow in either direction through the low-side FET, resulting in CCM operation with nearly constant switching frequency. A negative sink current limit circuit limits the current that can flow into SW and through the low-side FET to ground. In a buck regulator application, large negative current typically only flows from  $V_{OUT}$  to SW if  $V_{OUT}$  is lifted above the output regulation setpoint.

### 7.3.10 Enable / Undervoltage Lockout (EN/UVLO)

The LM5160-Q1 contains a dual-level undervoltage lockout (EN/UVLO) circuit. When the EN/UVLO voltage is below 0.35 V, the regulator is in a low-current shutdown mode. When the EN/UVLO voltage is greater than 0.35 V (typical) but less than 1.24 V (typical), the regulator is in standby mode. In standby mode, the VCC bias regulator is active but converter switching remains disabled. When the voltage at the VCC exceeds the VCC rising threshold,  $V_{CC(UV)} = 3.98$  V (typical), and the EN/UVLO voltage is greater than 1.24 V, normal switching operation begins. Use an external resistor voltage divider from VIN to GND to set the minimum operating voltage of the regulator.

EN/UVLO hysteresis is implemented with an internal 20  $\mu$ A (typical) current source ( $I_{UVLO(HYS)}$ ) that is switched on or off into the impedance of the EN/UVLO pin resistor divider. When the EN/UVLO threshold is exceeded, the current source is activated to effectively raise the voltage at the EN/UVLO pin. The hysteresis is equal to the value of this current times the upper resistance of the resistor divider,  $R_{UV2}$ . See [Functional Block Diagram](#).

### 7.3.11 Thermal Protection

The LM5160-Q1 must be operated such that the junction temperature does not exceed 150°C during normal operation. An internal thermal shutdown circuit is provided to protect the LM5160-Q1 in the event of higher than normal junction temperature. When activated, typically at 175°C, the controller is forced into a low-power reset state, disabling the high-side buck switch and the VCC regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature falls below 155°C (typical hysteresis of 20°C), the VCC regulator is enabled and operation resumes.

## 7.4 Device Functional Modes

### 7.4.1 Forced Pulse Width Modulation (FPWM) Mode

The [Synchronous Rectifier](#) section gives a brief introduction to the LM5160-Q1 diode emulation feature. The FPWM pin allows the power supply designer to select either CCM or DCM operation at light loads. When FPWM is connected to ground or left floating (FPWM = 0), a pulse-skipping mode and a zero-cross current detector circuit are enabled. The zero-cross detector turns off the low-side FET when the inductor current falls to zero ( $I_{LZ}$ , see [Electrical Characteristics](#)). This feature allows the LM5160-Q1 regulator to operate in DCM mode at light loads. In the DCM state, the switching frequency decreases with lighter loads.

If FPWM is pulled high (FPWM connected to VCC), the LM5160-Q1 operates in CCM even at light loads. This option allows the synchronous rectifier FET to conduct until the start of the next high-side switch cycle. The inductor current drops to zero and then reverse direction (negative direction through inductor), passing from drain to source of the low-side FET. The current flows continuously until the FB comparator initiates another high-side switch on-time. CCM operation reduces efficiency at light load but improves the transient response to step load changes and provides nearly constant switching frequency.

**Table 1. FPWM Pin Mode Summary**

FPWM PIN CONNECTION	LOGIC STAGE	DESCRIPTION
GND or Floating (High Z)	0	The FPWM pin is grounded or left floating. DCM enabled at light loads.
V <sub>CC</sub>	1	The FPWM pin is connected to VCC. The LM5160-Q1 then operates in CCM mode at light loads.

### 7.4.2 Undervoltage Detector

The following table summarizes the dual threshold levels of the undervoltage lockout (EN/UVLO) circuit explained in [Enable / Undervoltage Lockout \(EN/UVLO\)](#).

**Table 2. UVLO Pin Mode Summary**

EN/UVLO PIN VOLTAGE	VCC REGULATOR	MODE	DESCRIPTION
< 0.35 V	Off	Shutdown	V <sub>CC</sub> regulator disabled. High-side and low-side FETs disabled.
0.35 V to 1.24 V	On	Standby	V <sub>CC</sub> regulator enabled. High-side and low-side FETs disabled.
> 1.24 V	V <sub>CC</sub> < V <sub>CC(UV)</sub>	Standby	V <sub>CC</sub> regulator enabled. High-side and low-side FETs disabled.
	V <sub>CC</sub> > V <sub>CC(UV)</sub>	Operating	V <sub>CC</sub> regulator enabled. Switching enabled.

If input UVLO is not required, EN/UVLO can be driven by a logic signal as an enable input or connected directly to VIN. If EN/UVLO is directly connected to VIN, the regulator begins switching when V<sub>CC(UV)</sub> = 3.98 V (typical) is satisfied.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LM5160-Q1 is a synchronous buck or Fly-Buck DC/DC converter designed to operate over wide input voltage and output current ranges. LM5160-Q1 [quick-start calculator tools](#) are available for download to design a single-output synchronous buck converter or an isolated dual-output Fly-Buck converter. For a detailed design guide of the Fly-Buck converter, refer to [AN-2292 Designing an Isolated Buck \(Fly-Buck\) Converter](#) application report (SNVA674). Alternatively, use online WEBENCH software to create a complete buck or Fly-Buck design and generate the bill of materials, estimated efficiency, solution size and cost of the complete solution.

[Typical Applications](#) describes a few application circuits using the LM5160-Q1 with detailed, step-by-step design procedures.

#### 8.1.1 Ripple Configuration

The LM5160-Q1 uses an adaptive constant on-time (COT) control scheme in which the PWM on-time is set by a one-shot timer and the off-time is set by the feedback voltage ( $V_{FB}$ ) falling below the reference voltage. Therefore, for stable operation, the feedback voltage must decrease monotonically in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage ( $V_{FB}$ ) during the off-time must be large enough to dominate any noise present at the feedback node.

Table 3 presents three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple from the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor ripple current charging or discharging the output capacitor.
2. Resistive ripple caused by the inductor ripple current flowing through the ESR of the output capacitor and  $R_3$ .

Table 3. Ripple Configurations


TYPE 1	TYPE 2	TYPE 3
Lowest Cost	Reduced Ripple	Minimum Ripple
$R_3 \geq \frac{25 \text{ mV} \times V_O}{V_{REF} \times \Delta I_{L1, \min}}$	$C_{ff} \geq \frac{5}{F_{SW} \times (R_{FB2} \parallel R_{FB1})}$ $R_3 \geq \frac{25 \text{ mV}}{\Delta I_{L1, \min}}$	$R_A C_A \leq \frac{(V_{IN, \min} - V_O) \times T_{ON}(@ V_{IN, \min})}{25 \text{ mV}}$
	(6)	(7)
		(8)



The capacitive ripple is out-of-phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at output ( $V_{OUT}$ ) for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses a ripple injection circuit with  $R_A$ ,  $C_A$  and the switch-node (SW) voltage to generate a triangular ramp. This ramp is then AC-coupled into the feedback node (FB) using coupling capacitor  $C_B$ . Because this circuit does not use the output voltage ripple, it is suited for applications where low output voltage ripple is imperative. For more information on each ripple generation method, refer to the [AN-1481 Controlling Output Ripple & Achiev ESR Indep Constant On-Time Regulator Designs](#) application note.

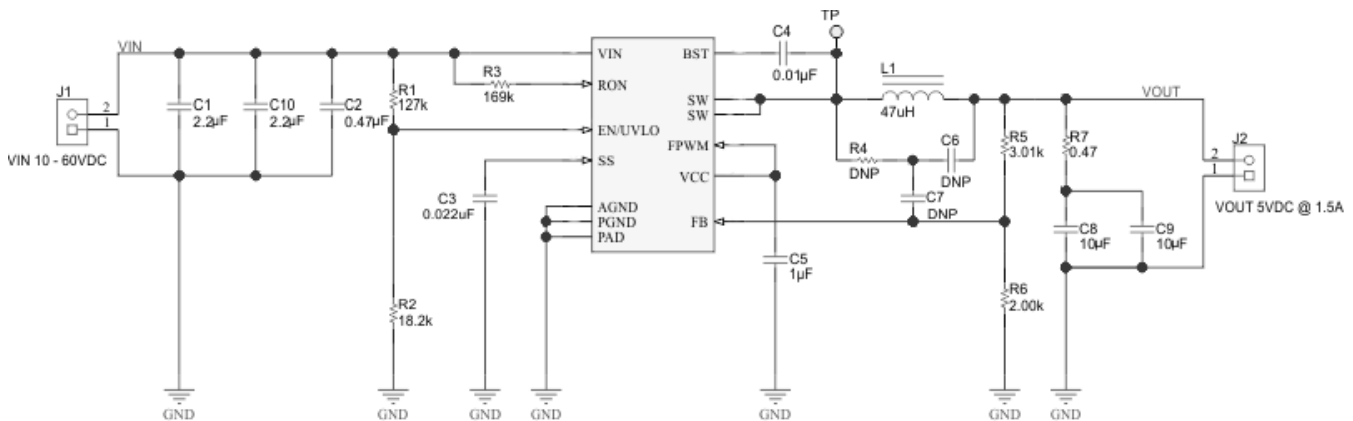
## 8.2 Typical Applications



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation and test results of an LM5160-powered implementation, refer to [Wide-Input Isolated IGBT Gate-Drive Fly-Buck Power Supply for Three-Phase Inverters](#) reference design.

### 8.2.1 LM5160-Q1 Synchronous Buck (10-V to 60-V Input, 5-V Output, 1.5-A Load)

A typical application example is a synchronous buck converter operating from a wide input voltage range of 10 V to 65 V and providing a stable 5-V output voltage with output current capability of 1.5 A. [Figure 19](#) shows the complete schematic for a typical synchronous buck application circuit. The components are labeled by numbers instead of the descriptive name used in the previous sections. For example, R3 represents  $R_{ON}$  and so forth.



**Figure 19. LM5160-Q1 Synchronous Buck Application Circuit**

#### NOTE

This and subsequent design examples are provided herein to showcase the LM5160-Q1 converter in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor may be required at the input to ensure stability, particularly at low input voltage and high output current operating conditions. See [Power Supply Recommendations](#) for more detail.



### 8.2.1.1 Design Requirements

Table 4 summarizes the operating parameters:

**Table 4. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10 V to 65 V
Output	5 V
Load current	1.5 A
Nominal switching frequency	300 kHz
Light-load operating mode	CCM, FPWM = VCC

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Custom Design With WEBENCH® Tools

Click [here](#) to create a custom design using the LM5160-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

#### 8.2.1.2.2 Feedback Resistor Divider - $R_{FB1}$ , $R_{FB2}$

With the required output voltage setpoint at 5 V and  $V_{FB} = 2$  V (typical), calculate the ratio of R6 ( $R_{FB1}$ ) to R5 ( $R_{FB2}$ ) using [Equation 9](#).

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{V_{REF}} - 1 \quad (9)$$

The resistor ratio calculates to be 3:2. Choose standard values of R6 ( $R_{FB1}$ ) = 2 k $\Omega$  and R5 ( $R_{FB2}$ ) = 3.01 k $\Omega$ . Higher or lower values can be used as long as a ratio of the 3:2 is maintained.

#### 8.2.1.2.3 Switching Frequency - $R_{ON}$

The duty cycle required to maintain output regulation at the minimum input voltage restricts the maximum switching frequency of the LM5160-Q1. The maximum value of the minimum forced off-time,  $T_{OFF,min}$ , limits the duty cycle and therefore the switching frequency. Calculate the maximum frequency that avoids output dropout at minimum input voltage using [Equation 10](#).

$$F_{SW,max}(@V_{IN,min}) = \frac{V_{IN,min} - V_{OUT}}{V_{IN,min} \times T_{OFF,min}(ns)} \quad (10)$$

For this design example, the maximum frequency based on the minimum off-time limitation of  $T_{OFF,min}$  (typical) = 170 ns is calculated as  $F_{SW,max}(@V_{IN,min}) = 2.9$  MHz. This value is well above 1 MHz, the maximum possible operating frequency of the LM5160-Q1.

At maximum input voltage the maximum switching frequency of the LM5160-Q1 is restricted by the minimum on-time,  $T_{ON,min}$  which limits the minimum duty cycle of the converter. Calculate the maximum frequency at maximum input voltage using [Equation 11](#).

$$F_{SW, \max (@ V_{IN, \max})} = \frac{V_{OUT}}{V_{IN, \max} \times T_{ON, \min} (\text{ns})} \quad (11)$$

Using Equation 11 and  $T_{ON, \min}$  (typical) = 150 ns, the maximum achievable switching frequency is  $F_{SW, \max (@ V_{IN, \min})} = 514$  kHz. Taking this value as the maximum possible switching frequency over the input voltage range for this application, choose a nominal switching frequency of  $F_{SW} = 300$  kHz for this design. The value of resistor  $R_{ON}$  sets the nominal switching frequency based on Equation 12.

$$R_{ON} = \frac{V_{OUT}}{F_{SW} \times 1 \times 10^{-10}} \Omega \quad (12)$$

For this particular application with  $F_{SW} = 300$  kHz,  $R_{ON}$  calculates to be 167 k $\Omega$ . Selecting a standard value for R3 ( $R_{ON}$ ) = 169 k $\Omega$  ( $\pm 1\%$ ) results in a nominal frequency of 296 kHz. The resistor value may need to be adjusted further in order to achieve the required switching frequency as the switching frequency in COT converters varies slightly ( $\pm 10\%$ ) with input voltage and/or output current. Operation at a lower nominal switching frequency results in higher efficiency but increases the inductor and capacitor values leading to a larger total solution size.

#### 8.2.1.2.4 Inductor - L

Select the inductor to limit the inductor ripple current between 20 and 40 percent of the maximum load current. Calculate the minimum value of the inductance required in this application from Equation 13.

$$L_{\min} = \frac{V_O \times (V_{IN, \max} - V_O)}{V_{IN, \max} \times F_{SW} \times I_{O, \max} \times 0.4} \quad (13)$$

Based on Equation 13, determine the minimum value of the inductance as 26  $\mu\text{H}$  for  $V_{IN} = 65$  V (maximum) and inductor ripple current equal to 40 percent of the maximum load current. Allowing some margin for inductance variation with current, select a higher standard value of L1 ( $L$ ) = 47  $\mu\text{H}$  for this design.

The peak inductor current at maximum load must be smaller than the minimum current limit threshold of the high-side FET, as given in *Electrical Characteristics* table. Determine the inductor ripple current at any input voltage using Equation 14.

$$\Delta I_L = \frac{V_O \times (V_{IN} - V_O)}{V_{IN} \times F_{SW} \times L} \quad (14)$$

Calculate the peak-to-peak inductor ripple current as 180 mA and 332 mA at the minimum and maximum input voltages, respectively. Determine the maximum peak inductor current in the buck FET using Equation 15.

$$I_{L(\text{peak})} = I_{O, \max} + \frac{\Delta I_{L, \max}}{2} \quad (15)$$

In this design with an output current of 1.5 A, the maximum peak inductor current is calculated to be approximately 1.67 A, which is less than the high-side FET minimum current limit threshold.

The saturation current of the inductor must also be carefully considered. The peak value of the inductor current is bound by the high-side FET current limit during overload or short circuit conditions. Based on the high-side FET current limit specification in *Electrical Characteristics*, select an inductor with saturation current rating above 2.875 A.

#### 8.2.1.2.5 Output Capacitor - $C_{OUT}$

Select the output capacitor to limit the capacitive ripple at the output of the regulator. Maximum capacitive ripple is observed at maximum input voltage. The output capacitance required for a ripple voltage  $\Delta V_O$  across the capacitor is given by Equation 16.

$$C_{OUT} = \frac{\Delta I_{L, \max}}{8 \times F_{SW} \times \Delta V_{O, \text{ripple}}} \quad (16)$$

Substituting  $\Delta V_{O, \text{ripple}} = 10$  mV gives  $C_{OUT} = 14$   $\mu\text{F}$ . Two standard 10- $\mu\text{F}$  ceramic capacitors in parallel (C8, C9) are selected. An X7R type capacitor with a voltage rating 16 V or higher must be used for  $C_{OUT}$  (C8, C9) to limit the reduction of capacitance due to DC bias voltage.

### 8.2.1.2.6 Series Ripple Resistor - $R_{ESR}$

Select the series resistor such that sufficient ripple is injected at the feedback node (FB). The ripple voltage produced by  $R_{ESR}$  is proportional to the inductor ripple current. Therefore, select  $R_{ESR}$  based on the lowest inductor ripple current occurring at minimum input voltage. Calculate  $R_{ESR}$  using [Equation 17](#).

$$R_{ESR} \geq \frac{25 \text{ mV} \times V_O}{V_{REF} \times \Delta I_{L, \min}} \quad (17)$$

With  $V_O = 5 \text{ V}$ ,  $V_{REF} = 2 \text{ V}$  and  $\Delta I_{L, \min} = 180 \text{ mA}$  (at  $V_{IN, \min} = 10 \text{ V}$ ) as calculated in [Equation 14](#), [Equation 17](#) requires an  $R_{ESR}$  greater than or equal to  $0.35 \Omega$ . Selecting R7 ( $R_{ESR}$ ) =  $0.47 \Omega$  results in approximately 150 mV of maximum output voltage ripple at  $V_{IN, \max}$ . For applications requiring lower output voltage ripple, use Type II or Type III ripple injection circuits as described in [Ripple Configuration](#).

### 8.2.1.2.7 VCC and Bootstrap Capacitors - $C_{VCC}$ , $C_{BST}$

The VCC capacitor charges the bootstrap capacitor during the off-time of the high-side switch and powers internal logic circuits and the low-side sync FET gate driver. The bootstrap capacitor biases the high-side gate driver during the high-side FET on-time. Recommended values for C5 ( $C_{VCC}$ ) and C4 ( $C_{BST}$ ) are 1  $\mu\text{F}$  and 10 nF, respectively. Both must be high-quality X7R ceramic capacitors.

### 8.2.1.2.8 Input Capacitor - $C_{IN}$

The input capacitor must be large enough to limit the input voltage ripple to an acceptable level. [Equation 18](#) provides the input capacitance  $C_{IN}$  required for a worst-case input ripple of  $\Delta V_{IN, \text{ripple}}$ .

$$C_{IN} = \frac{I_{O, \max} \times D \times (1 - D)}{\Delta V_{IN, \text{ripple}} \times F_{SW}} \quad (18)$$

$C_{IN}$  (C1, C10) supplies most of the switch current during the on-time to limit the voltage ripple at the VIN pin. At maximum load current, when the buck switch turns on, the current into the VIN pin quickly increases to the valley current of the inductor ripple and then ramps up to the peak of the inductor ripple during the on-time of the high-side FET. The average current during the on-time is the output load current. For a worst-case calculation,  $C_{IN}$  must supply this average load current during the maximum on-time, without letting the voltage at VIN drop more than the desired input ripple. For this design, the input voltage drop is limited to 0.5 V and the value of  $C_{IN}$  is calculated using [Equation 18](#).

Based on [Equation 18](#), the value of the input capacitor is determined as approximately 2.5  $\mu\text{F}$  at  $D = 0.5$ . Taking into account the decrease in capacitance with applied voltage, two standard value 2.2- $\mu\text{F}$ , 100-V, X7R ceramic capacitors are selected for C1 and C10. The input capacitors must be rated for the maximum input voltage under all operating and transient conditions.

A third input capacitor C2 may be needed in this design as a bypass path for the high-frequency components of input switching current. The value of C2 is 0.1  $\mu\text{F}$  and this bypass capacitor must be placed directly across VIN and PGND (pins 3 and 2) near the IC. The  $C_{IN}$  values and location are critical to reducing switching noise and transients.

### 8.2.1.2.9 Soft-Start Capacitor - $C_{SS}$

The capacitor at the SS pin determines the soft-start time, that is, the time for the output voltage to reach its final steady-state value. Determine the SS capacitor value from [Equation 19](#):

$$C_{SS} = \frac{I_{SS} \times T_{\text{Startup}}}{V_{SS}} \quad (19)$$

With C3 ( $C_{SS}$ ) set at 22 nF and  $V_{SS} = 2 \text{ V}$ ,  $I_{SS} = 10 \mu\text{A}$ ,  $T_{\text{Startup}}$  is approximately 4 ms.

### 8.2.1.2.10 EN/UVLO Resistors - $R_{UV1}$ , $R_{UV2}$

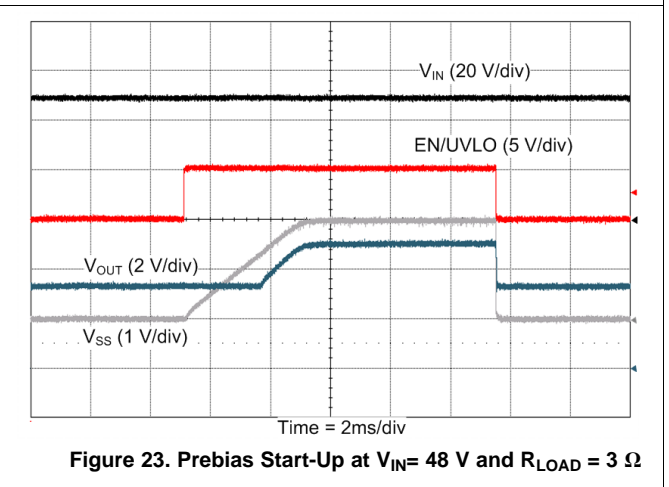
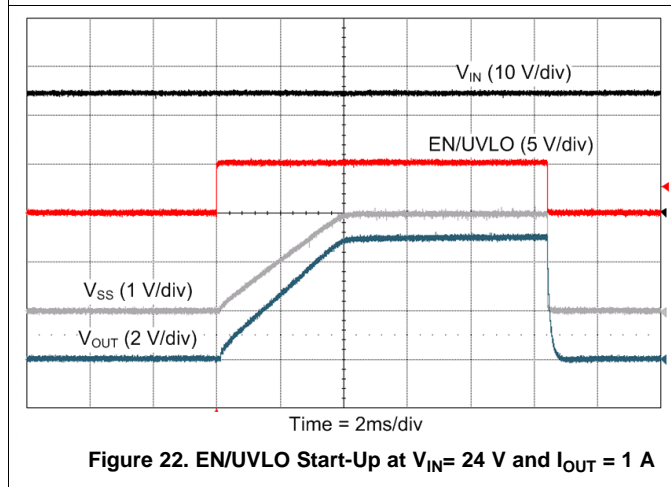
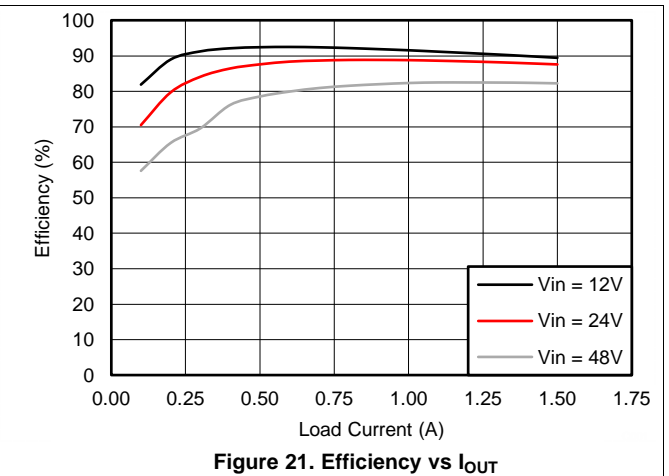
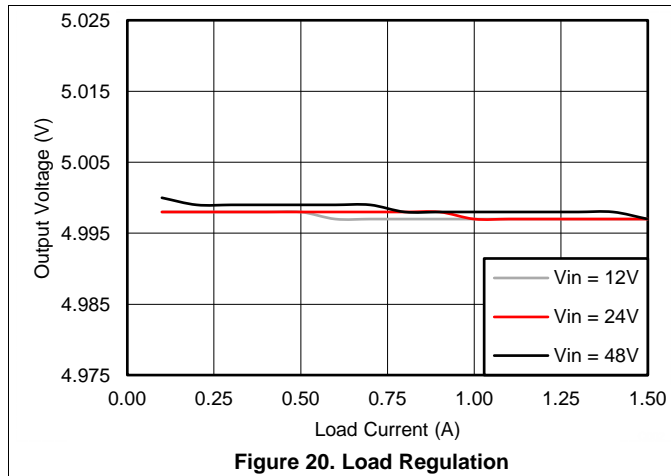
The UVLO resistors R1 ( $R_{UV2}$ ) and R2 ( $R_{UV1}$ ) set the input undervoltage lockout threshold and hysteresis according to [Equation 20](#) and [Equation 21](#).

$$V_{IN(\text{HYS})} = I_{UVLO(\text{HYS})} \times R_{UV2} \quad (20)$$

$$V_{IN,UVLO(rising)} = V_{UVLO(TH)} \left( 1 + \frac{R_{UV2}}{R_{UV1}} \right) \tag{21}$$

From the *Electrical Characteristics* table,  $I_{UVLO(HYS)} = 20 \mu A$  (typical). To design for a  $V_{IN}$  rising threshold ( $V_{IN,UVLO(rising)}$ ) of 10 V and hysteresis of 2.5 V, Equation 20 and Equation 21 yield  $R_{UV1} = 17.98 \text{ k}\Omega$  and  $R_{UV2} = 125 \text{ k}\Omega$ . Selecting 1% standard values of R2 ( $R_{UV1}$ ) = 18.2 kΩ and R1 ( $R_{UV2}$ ) = 127 kΩ result in UVLO rising threshold and hysteresis voltages of 9.89 V and 2.54 V, respectively.

### 8.2.1.3 Application Curves



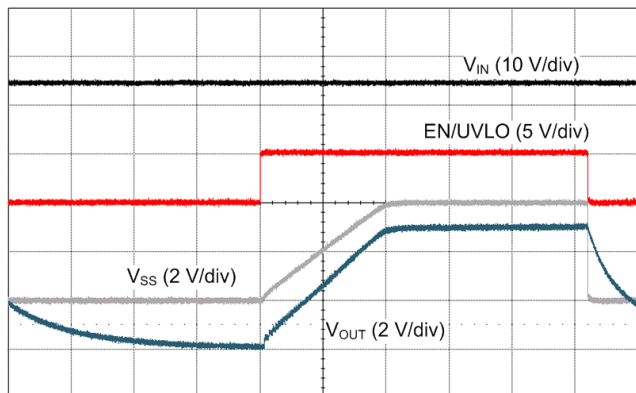


Figure 24. EN/UVLO Start-Up at  $V_{IN} = 24\text{ V}$  and  $R_{LOAD} = 100\ \Omega$

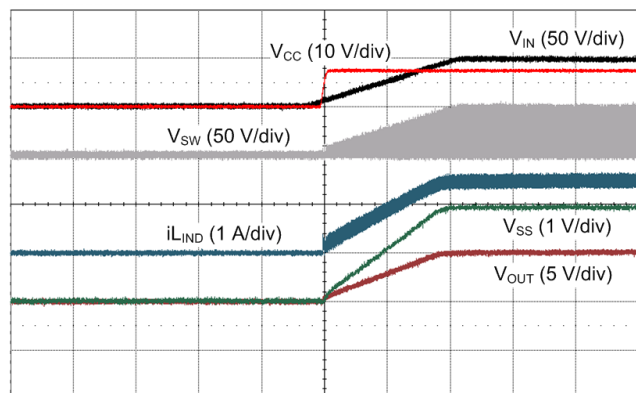


Figure 25. Start-Up at  $V_{IN} = 48\text{ V}$  and  $R_{LOAD} = 10\ \Omega$

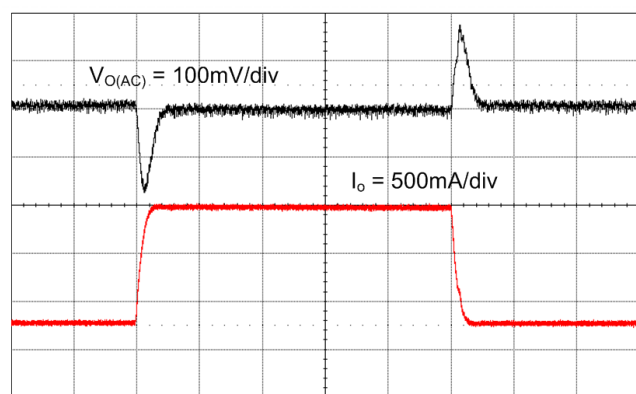


Figure 26. Load Transient (300 mA – 1.5 A) at  $V_{IN} = 24\text{ V}$  With Type 3 Ripple Configuration

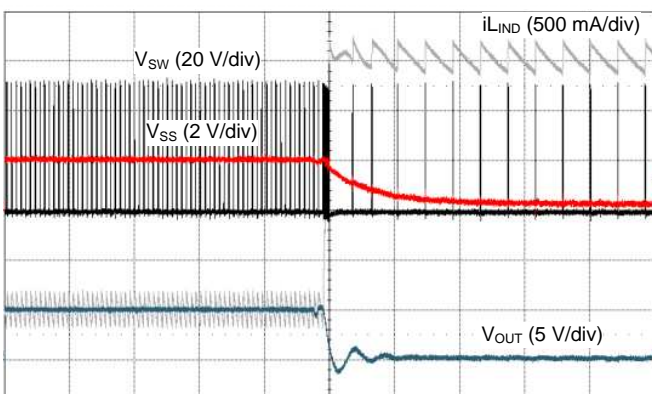


Figure 27. Output Short-Circuit at  $V_{IN} = 48\text{ V}$

### 8.2.2 LM5160-Q1 Isolated Fly-Buck (18-V to 32-V Input, 12-V, 4.5-W Isolated Output)



For technical solutions, industry trends, and insights for designing and managing power supplies, please refer to TI's [Power House](#) blog series.

Below is an application example of an isolated Fly-Buck converter that operates over an input voltage range of 18 V to 32 V. It provides a stable 12-V isolated output voltage with an output power capability of 4.5 W. [Figure 28](#) shows the complete schematic of the Fly-Buck application circuit.

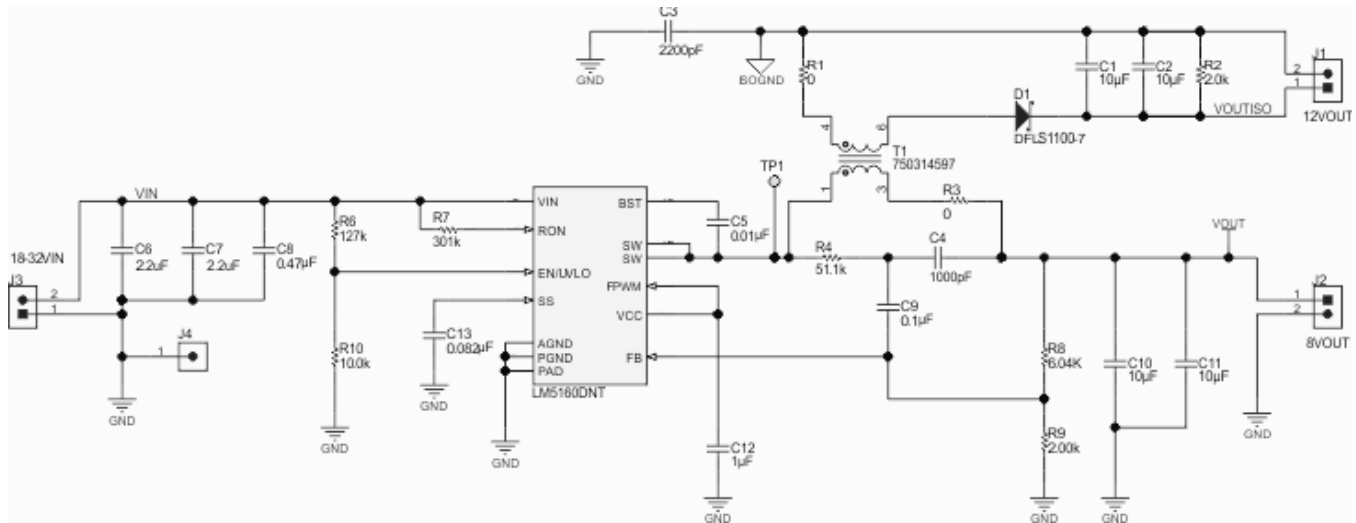


Figure 28. LM5160-Q1 12-V, 4.5-W Fly-Buck Converter Schematic

#### 8.2.2.1 LM5160-Q1 Fly-Buck Design Requirements

This LM5160-Q1 Fly-Buck application example is designed to operate from a 24-V DC supply with line variations from 18 V to 32 V. The example provides a space-optimized and efficient 12-V isolated output solution with secondary load current capability from 0 mA to 400 mA. The primary side remains unloaded in this application. The switching frequency is set at 300 kHz (nominal). This design achieves greater than 88% peak efficiency.

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	18 V to 32 V
Isolated output	12 V
Isolated load current range	0 mA to 400 mA
Nominal switching frequency	300 kHz
Peak Efficiency	88%

#### 8.2.2.2 Detailed Design Procedure

The Fly-Buck converter design procedure closely follows the buck converter design outlined in [LM5160-Q1 Synchronous Buck \(10-V to 60-V Input, 5-V Output, 1.5-A Load\)](#). The selection of primary output voltage, transformer turns ratio, rectifier diode, and output capacitors are covered here.

##### 8.2.2.2.1 Selection of $V_{OUT1}$ and Turns Ratio

The primary-side output voltage of a Fly-Buck converter must be no more than one half of the minimum input voltage. For a minimum  $V_{IN}$  of 18 V, the primary output voltage ( $V_{OUT}$ ) must be no higher than 9 V. To generate an isolated output voltage of  $V_{OUT(ISO)} = 12$  V, a transformer turns ratio of 1 : 1.5 ( $N1 : N2$ ) is selected. Using this turns ratio, calculate the required primary output voltage  $V_{OUT}$  using [Equation 22](#).

$$V_{OUT} = \frac{V_{OUT(ISO)} + 0.7 \text{ V}}{1.5} = 8.47 \text{ V} \quad (22)$$

The 0.7 V subtracted from  $V_{OUT(ISO)}$  represents the forward voltage drop of the secondary rectifier diode. Fine tuning the primary side  $V_{OUT1}$  may be required to account for voltage errors due to the leakage inductance of the transformer and the resistance of the transformer windings and the low-side MOSFET of the LM5160-Q1.

### 8.2.2.2.2 Secondary Rectifier Diode

The secondary rectifier diode must block the maximum input voltage multiplied by the transformer turns ratio. Determine the minimum diode reverse voltage  $V_{R(diode)}$  rating from Equation 23.

$$V_{R(diode)} = V_{IN(max)} \times \frac{N2}{N1} + V_{OUT(ISO)} = 32 \text{ V} \times 1.5 + 12 \text{ V} = 60 \text{ V} \quad (23)$$

Select a diode with 60 V or higher reverse voltage rating for this application. If the input voltage ( $V_{IN}$ ) has transients above the normal operating maximum input voltage of 32 V, then the worst-case transient input voltage must be used in the diode voltage calculation given by Equation 23.

### 8.2.2.2.3 External Ripple Circuit

A Type 3 ripple circuit is required for Fly-Buck converter applications. The design procedure for ripple components is identical to that in a buck converter. See [Ripple Configuration](#) for ripple design information.

### 8.2.2.2.4 Output Capacitor - $C_{OUT2}$

The Fly-Buck output capacitor conducts higher ripple current than a buck converter output capacitor. Calculate the capacitive ripple for the isolated output capacitor based on the time the rectifier diode is off. During this time the entire output current is supplied by the output capacitor. Calculate the required capacitance for a worst-case  $V_{OUT2}$  ( $V_{OUT(ISO)}$ ) ripple voltage using Equation 24.

$$C_{OUT2} = \frac{I_{OUT2}}{\Delta V_{OUT2}} \left( \frac{V_{OUT1}}{V_{IN(MIN)}} \right) \times \frac{1}{f_{sw}}$$

where

- $\Delta V_{OUT2}$  is the target ripple at the secondary output. (24)

Equation 24 is an approximation and ignores the ripple components associated with ESR and ESL of the output capacitor. For a  $\Delta V_{OUT2} = 100 \text{ mV}$ , Equation 24 requires  $C_{OUT2} = 6.5 \text{ }\mu\text{F}$ . When selecting a ceramic capacitor, consider its voltage coefficient to ensure sufficient capacitance at the output voltage operating point.

### 8.2.2.3 Application Curves

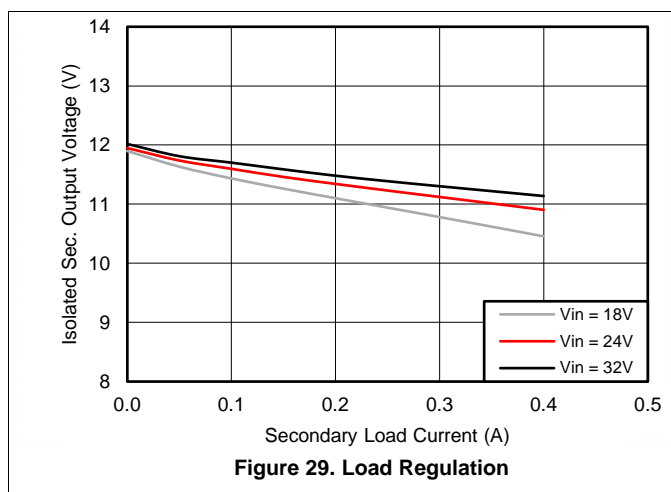


Figure 29. Load Regulation

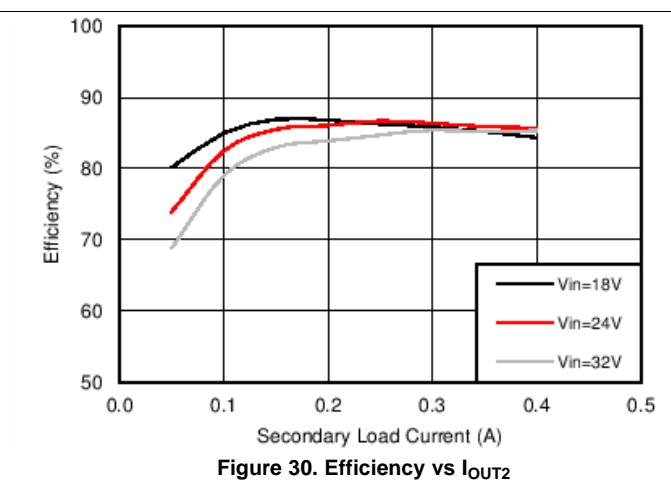
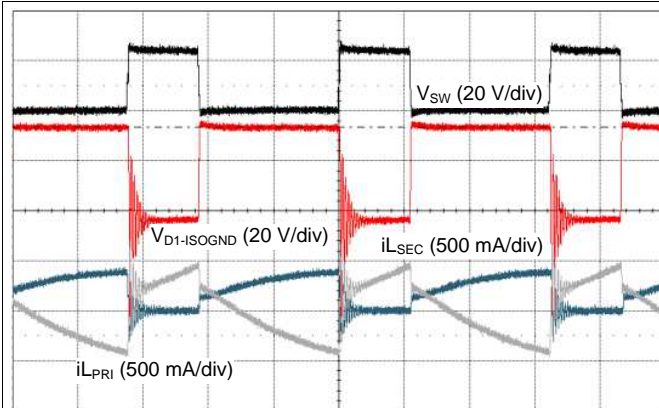
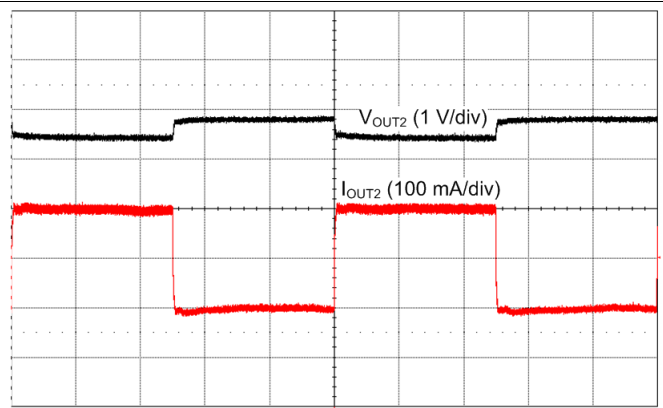


Figure 30. Efficiency vs  $I_{OUT2}$

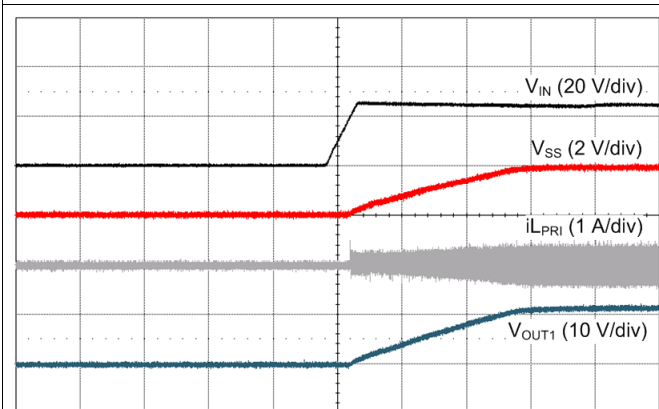




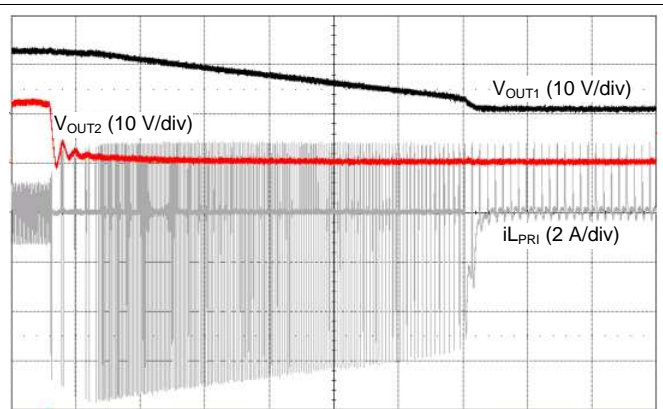
**Figure 31. Primary Switch Node at  $V_{IN} = 24\text{ V}$  and  $I_{OUT2} = 200\text{ mA}$**



**Figure 32. Load Transient at  $I_{OUT2} = 100\text{ mA} - 300\text{ mA}$**



**Figure 33. VIN Start-Up at  $I_{OUT2} = 200\text{ mA}$**



**Figure 34. Secondary Short at  $I_{OUT2} = 600\text{ mA}$  and  $I_{OUT1} = 200\text{ mA}$**

### 8.3 Do's and Don'ts

As mentioned earlier in [Soft Start](#), the SS capacitor  $C_{SS}$  must always be more than 1 nF in both buck and Fly-Buck converter applications. Apart from determining the start-up time, this capacitor serves as the external compensation of the internal  $G_M$  error amplifier. A minimum value of 1 nF is necessary to maintain stability. The SS pin must not be left floating.

The VCC pin of the LM5160-Q1 must not be biased with an external voltage source. When an improved efficiency requirement warrants an external  $V_{CC}$  bias, the LM5160A must be used.



## 9 Power Supply Recommendations

The LM5160-Q1 DC/DC converter is designed to operate from a wide input voltage range of 4.5 V to 65 V. The characteristics of the input supply must be compatible with the [Absolute Maximum Ratings](#) and [Recommended Operating Conditions](#) tables. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with [Equation 25](#).

$$I_{IN} = \frac{P_{OUT}}{V_{IN} \cdot \eta}$$

where

- $\eta$  is the efficiency (25)

If the regulator is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables may have an adverse affect on converter operation, particularly during operation at low input voltage. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled on and off. The parasitic resistance causes the input voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10  $\mu$ F to 47  $\mu$ F is usually sufficient to provide input parallel damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The application report [Simple Success with Conducted EMI for DC-DC Converters](#) (SNVA489) provides helpful suggestions when designing an input filter for any switching regulator.

## 10 Layout

### 10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. In particular, observe the following guidelines:

- $C_{IN}$ : The loop consisting of input capacitor ( $C_{IN}$ ), VIN pin and PGND pin carries the switching current. The input capacitor must be placed close to the IC, directly across VIN and PGND pins, and the connections to these two pins must be direct to minimize the switching power loop area. In general, it is not possible to place all of input capacitances near the IC. A good layout practice includes placing the bulk capacitor(s) as close as possible to the VIN pin (see Figure 35). A bypass capacitor measuring 0.1  $\mu\text{F}$  must be placed directly across VIN and PGND (pin 3 and 2, respectively), as close as possible to the IC while complying with all layout design rules.
- $C_{VCC}$  and  $C_{BST}$ : The VCC and bootstrap (BST) bypass capacitors supply switching currents to the high-side and low-side gate drivers. These two capacitors must also be placed as close to the IC as possible, and the connecting trace length and loop area must be minimized (see Figure 35).
- The feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of the LM5160-Q1. Therefore, take care while routing the feedback trace to avoid coupling any noise into this pin. In particular, the feedback trace must be short and not run close to magnetic components, or parallel to any other switching trace.
- SW trace: The SW node switches rapidly between VIN and GND every cycle and is therefore a source of noise. The SW node copper area must be minimized. In particular, the SW node must not be inadvertently connected to a copper plane or pour.

### 10.2 Layout Example

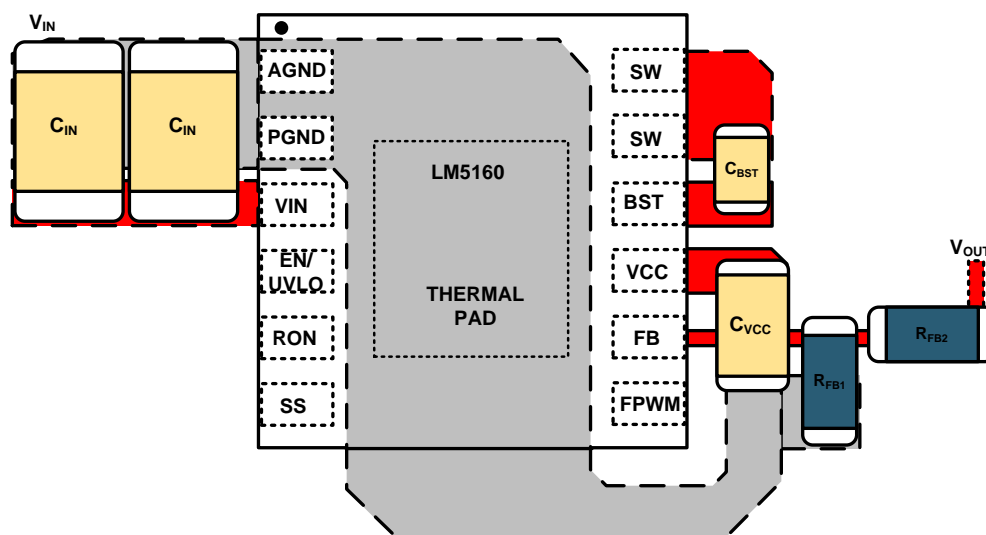


Figure 35. Placement of Bypass Capacitors

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 11.1.2 Development Support

For development support, see the following:

- [LM5160 Buck Converter Quick-start Calculator](#)
- [LM5160 Fly-Buck Converter Quick-start Calculator](#)
- [LM5160 PSpice Transient Model](#)
- [LM5160 Unencrypted PSpice Transient Model](#)
- [LM5160 TINA-TI Fly-Buck Reference Design](#)
- For TI's reference design library, visit [TIDesigns](#)
- For TI's WEBENCH Design Environment, visit the [WEBENCH® Design Center](#)
- To view a related device of this product, see the [LM5161-Q1](#) 100-V, 1-A synchronous buck converter

##### 11.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LM5160-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- [LM5160A, LM5160 Buck EVM User's Guide](#) (SNVU441)
- [LM5160 Fly-Buck \(Isolated Buck\) User's Guide](#) (SNVU408)
- [AN-2292 Designing an Isolated Buck \(Fly-Buck\) Converter](#) (SNVA674)
- [AN-1481 Controlling Output Ripple & Achieving ESR Independence in Constant ON-Time Regulator Designs](#) (SNVA166)
- TI Designs:
  - [High Resolution, Fast Startup Analog Front End for Air Circuit Breaker Reference Design](#) (TIDUB80)
  - [Wide-Input Isolated IGBT Gate-Drive Fly-Buck Power Supply for Three-Phase Inverters](#) (TIDU670)
  - [Input Protection and Backup Supply Reference Design for 25W PLC Controller Unit](#) (TIDUCC7)
  - [Non-Isolated RS-485 to Wi-Fi Bridge with 24 VAC Power Reference Design](#) (TIDUA48)
  - [Isolated RS-485 to Wi-Fi Bridge with 24 VAC Power Reference Design](#) (TIDUA49)

## Documentation Support (continued)

- [Dual-Output Isolated Fly-Buck Reference Design With an Ultra-Small Coupled Inductor](#) (TIDUC31)
- [2.5W Bipolar Isolated Fly-Buck Ultra-Compact Reference Design](#) (TIDUCA3)
- [Small Footprint Isolated DC/DC Converter for Analog Input Module Reference Design](#) (TIDUBR7)
- [2.3 nV/√Hz, Differential, Time Gain Control \(TGC\) DAC Reference Design for Ultrasound](#) (TIDUD38)
- [Leakage Current Measurement Reference Design for Determining Insulation Resistance](#) (TIDU873)
- [Class 3 Isolated Fly-Buck Power Module for PoE Application Reference Design](#) (TIDU779)
- [Thermal Protection Reference Design of IGBT Modules for HEV/EV Traction Inverters](#) (TIDUBJ2)
- White Papers:
  - [Designing Isolated Rails on the Fly With Fly-Buck Converters](#)
  - [Valuing Wide  \$V\_{IN}\$ , Low-EMI Synchronous Buck Circuits for Cost-Effective, Demanding Applications](#)
  - [An Overview of Conducted EMI Specifications for Power Supplies](#)
  - [An Overview of Radiated EMI Specifications for Power Supplies](#)
- Power House Blogs:
  - [Fly-Buck: Frequently Asked Questions \(FAQs\)](#)
  - [Lower EMI and Quiet Switching With the Fly-Buck Topology](#)
  - [Fly-Buck Converter PCB Layout Tips](#)
  - [When is Fly-Buck the Right Choice for Your Isolated Power Needs?](#)
  - [How to Design for EMC and Isolation With Fly-Buck Converters](#)
  - [Create a Fly-Buck Converter in WEBENCH® Power Designer](#)
- [AN-2162: Simple Success with Conducted EMI from DC-DC Converters](#) (SNVA489)
- [Automotive Cranking Simulator User's Guide](#) (SLVU984)
- [Using New Thermal Metrics](#) (SBVA025)
- [Semiconductor and IC Package Thermal Metrics](#) (SPRA953)

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.5 Trademarks

Fly-Buck, E2E are trademarks of Texas Instruments.  
 WEBENCH is a registered trademark of Texas Instruments.  
 All other trademarks are the property of their respective owners.

### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary




[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5160QPWPQ1	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1	
LM5160QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1	
LM5160QPWPTQ1	ACTIVE	HTSSOP	PWP	14	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LM5160-Q1 :**

- Catalog: [LM5160](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

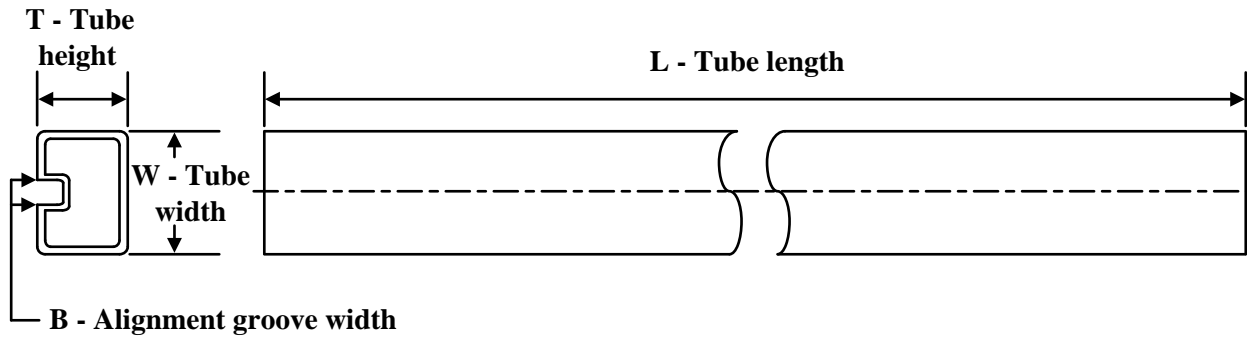
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5160QPWPRQ1	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5160QPWPTQ1	HTSSOP	PWP	14	250	178.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**

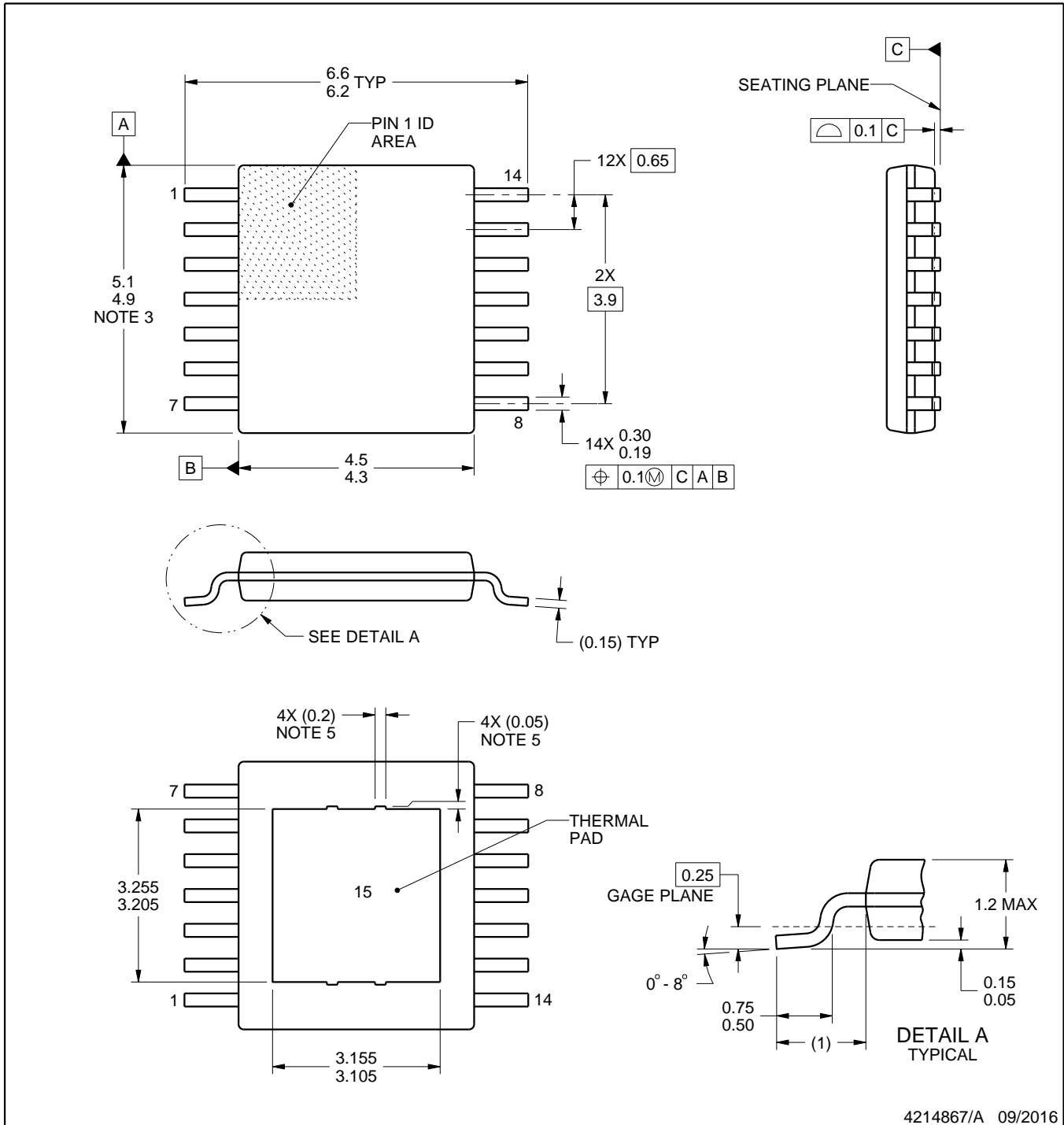
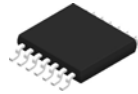

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5160QPWPRQ1	HTSSOP	PWP	14	2500	356.0	356.0	35.0
LM5160QPWPTQ1	HTSSOP	PWP	14	250	208.0	191.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM5160QPWPQ1	PWP	HTSSOP	14	94	495	8	2514.6	4.06



4214867/A 09/2016

NOTES:

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1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.

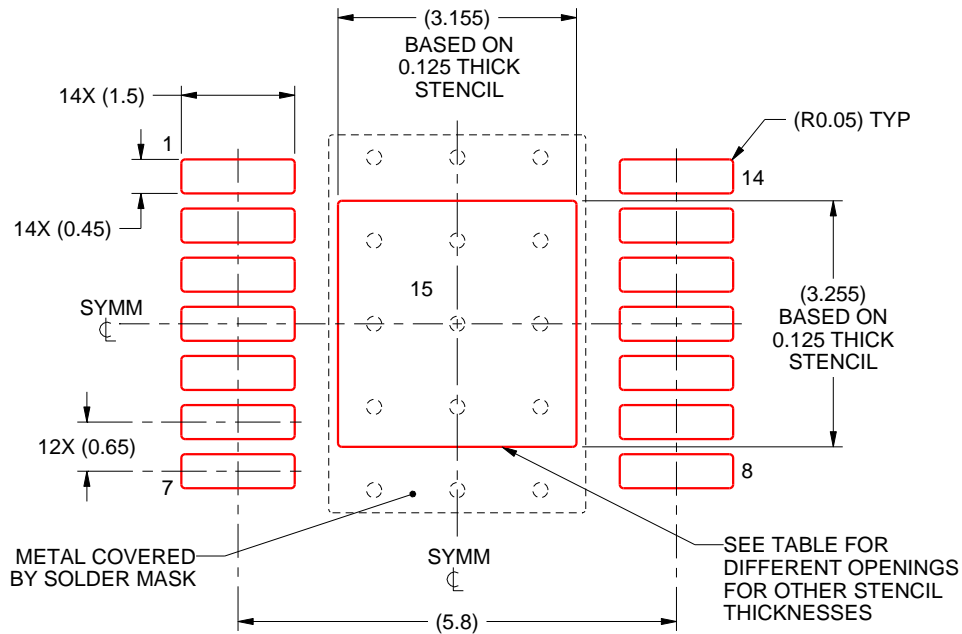


# EXAMPLE STENCIL DESIGN

PWP0014A

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
 EXPOSED PAD  
 100% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.53 X 3.64
0.125	3.155 X 3.255 (SHOWN)
0.15	2.88 X 2.97
0.175	2.67 X 2.75

4214867/A 09/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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