ON Semiconductor®

# Product Bulletin

Document # : PB21541X
Issue Date: 15 November 2016

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| **Title of Change:** | Introduction of two additional system clock (SYS_CLK) calibration settings for the Ezairo 7110 hybrid |
| **Effective date:** | 15 November 2016 |
| **Contact information:** | Contact your local ON Semiconductor Sales Office or <christophe.waelchli@onsemi.com> |
| **Type of notification:** | ON Semiconductor will consider this change accepted. |
| **Change category:** | ☐ Wafer Fab Change ☐ Assembly Change ☒ Test Change ☐ Other _____ |

**Change Sub-Category(s):**

☐ Manufacturing Site Change/Addition
☐ Manufacturing Process Change
☐ Material Change
☒ Product specific change
☐ Datasheet/Product Doc change
☐ Shipping/Packaging/Marking
☐ Other: _____

**Sites Affected:**

☐ All site(s) ☐ not applicable ☒ ON Semiconductor site(s) : ON Burlington, Canada ☐ External Foundry/Subcon site(s)

**Description and Purpose:**

We are introducing 2 additional system clock (SYS_CLK) calibration settings for 12.80 and 15.36 MHz. These 2 calibration settings are introduced through a modification of the production test program. The new test program is computing the calibration settings for these 2 SYS_CLK and writing them in the manufacturing area of the EEPROM in the "CLKCAL_ENTRY" area.

2 VDDC calibration values will be included:

- The default one, already available today, for VDDC = 0.82 V, is stored in the VDDC calibration entry located in the EEPROM at address 0x0064.
- A new calibration value, for VDDC = 0.88 V, will be stored in the manufacturing area of the EEPROM at address EEFS_VDDC_ALT_CAL_ADDR (0x00E8). This VDDC value should be used for SYS_CLK of 12.80 or 15.36 MHz.

In order to retrieve the calibration value for VDDC at 0.88V from EEPROM, the macro EELIB_ReadWord24 can be used.

Note that the default clock calibration settings (10.24 MHz) will not change. The default VDDC calibration settings (0.82 V) will not change either. This means that the proposed new calibrations settings will not impact an application that doesn't use these settings.

Implementation of the change will be controlled by work order number. Devices shipped after the Effective date will include the 2 additional system clock entries and exact order number will be communicated to customers individually. OPN will not change.

**List of affected Standard Parts:**

E7110-102A33-BPG
E7110-102A33-AG