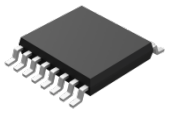
MLX91377 – High Performance Linear Hall Effect Sensor IC

Datasheet

Features and Benefits

- Linear Hall Effect Sensor IC
- On Chip Signal Processing for Robust and Accurate Sensing
- Programmable Measurement Range
- Programmable Linear Transfer Characteristic (4 or 8 Multi-points or 16 or 32 Piece-Wise-Linear)
- Selectable Short PWM Code (SPC) or Analog Output modes
- SAE J2716 APR2016 SENT
- ISO26262 ASIL READY BY MELEXIS
  ASIL-C Safety Element out of Context for SPC output, ASIL-B Safety Element out of Context capable for analog output
- 48-bit programmable ID Number
- Dual Die (Full Redundant) - TSSOP-16 package RoHS Compliant
- AEC Q-100 Grade 0 qualified



TSSOP-16

Application Examples

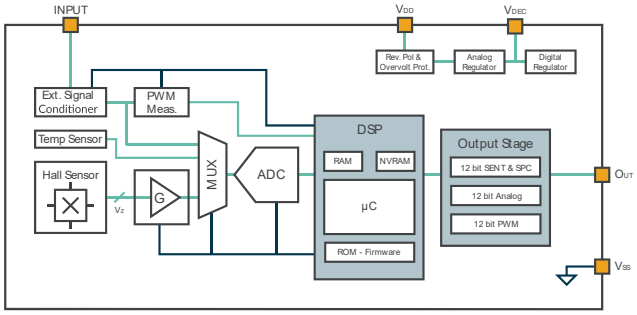
- Steering Torque Sensor
- Acceleration, Brake, or Clutch Sensor
- Absolute Linear Position Sensor
- Float-Level Sensor
- Non-Contacting Potentiometer
- Small Angle Position Sensor
- Small Stroke Position Sensor

Description

The MLX91377 is a monolithic magnetic position processor IC. It consists of a Hall effect magnetic front end, an analog to digital signal conditioner, a DSP for advanced signal processing and an output stage driver.

The MLX91377 is sensitive to the magnetic flux density applied perpendicular to the IC (i.e. Bz). This allows the MLX91377 with the correct magnetic circuit to decode the absolute position of any moving magnet or linear displacement, see Figure 2). It enables the design of non-contacting position sensors that are frequently required for both automotive and industrial applications.

The MLX91377 provides two output modes. Firstly, the IC supports SPC frames encoded according to a Secure Sensor format. Through programming, the MLX91377 can also be configured to output an analog signal.



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Ordering Information

Product	Temperature	Package	Option Code	Packing Form	Definition
MLX91377	G	GO	ADB-080	RE	SPC output, TSSOP-16 dual-die package
MLX91377	G	GO	ADB-010	RE	High speed analog output, TSSOP-16 dual-die package

Table 1 - Ordering Codes

Temperature Code:	G: from -40°C to 160°C
Package Code:	GO: TSSOP-16 package
Option Code - Chip revision	**ADB**-123 : **Chip Revision** ▪ ADB : Standard preferred revision
Option Code - Application	ADB-**1**23 : **1**-**Application - Magnetic configuration** ▪ 0: Linear Hall
Option Code - SW configuration: output mode, protocol	ADB-1**2**3 : **2**-**SW configuration: output mode, protocol** ▪ 1: high speed analog output mode ▪ 8: SPC output mode, 1.5µs tick time
Option Code - TSSOP-16 package configuration	ADB-12**3** : **3**-**TSSOP-16 package configuration** ▪ 0: TSSOP-16 dual-die package
Packing Form:	-RE : Tape & Reel ▪ GO: 4500 pcs/reel
Ordering Example:	MLX91377GGO-ADB-080-RE For a linear hall sensor with SPC protocol in TSSOP-16 dual-die package, delivered on a Reel of 4500pcs.

Table 2 - Ordering Codes Information

Contents

1. Functional Diagram and Application Modes

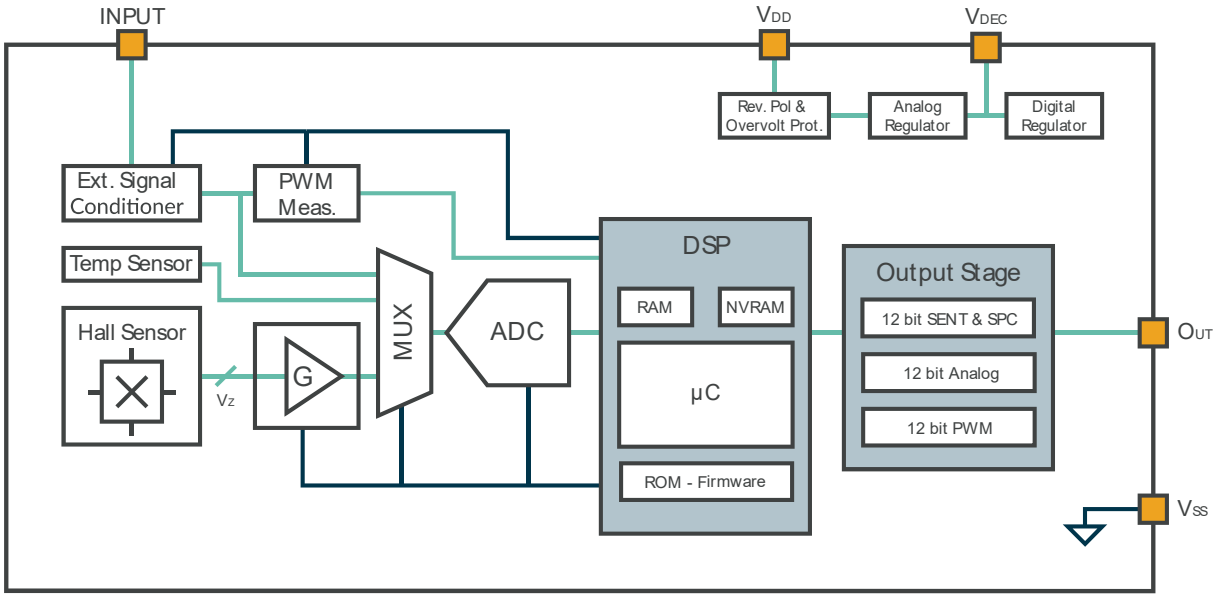


Figure 1 - MLX91377 Block diagram

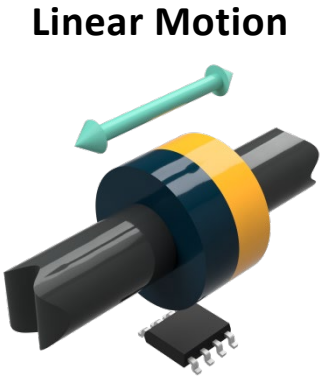


Figure 2 - Application Modes

2. Glossary of Terms

Name	Description
ADC	Analog-to-Digital Converter
AoU	Assumption of Use
ASP	Analog Signal Processing
AWD	Absolute Watchdog
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DC	Duty Cycle of the output signal i.e. T_{ON} /(T_{ON} + T_{OFF})
DMP	Dual Mold Package
DP	Discontinuity Point
DSP	Digital Signal Processing
DTI	Diagnostic Test Interval
ECC	Error Correcting Code
EMA	Exponential Moving Average
EMC	Electro-Magnetic Compatibility
EoL	End of Line
FIR	Finite Impulse Response
FHTI	Fault Handling Time Interval
Gauss (G)	Alternative unit for the magnetic flux density (10G = 1mT)
HW	Hardware
IMC	Integrated Magnetic Concentrator
INL/DNL	Integral Non-Linearity / Differential Non-Linearity
IWD	Intelligent Watchdog
LNR	Linearization
LSB/MSB	Least Significant Bit / Most Significant Bit
NC	Not Connected
NVRAM	Non Volatile RAM
POR	Power On Reset
PSF	Product Specific Functions
PWL	Piecewise Linear
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
SPC	Short PWM code
SCN	Status & Communication Nibble
SEooC	Safety Element out of Context
TC	Temperature Coefficient (in ppm/°C)
Tesla (T)	SI derived unit for the magnetic flux density (Vs/m2)

Table 3 - Glossary of Terms

3. Pin Definitions and Descriptions

3.1. Pin Definition for TSSOP-16 Dual-Die package

Pin #	Name	Description
1	V_{DEC1}	Decoupling pin die1
2	V_{SS1}	Ground die1
3	V_{DD1}	Supply die1
4	$Input_1$	For test
5	$Test_2$	For test
6	OUT_2	Output die2
7	N.C.	Not connected
8	N.C.	Not connected
9	V_{DEC2}	Decoupling pin die2
10	V_{SS2}	Ground die2
11	V_{DD2}	Supply die2
12	$Input_2$	For test
13	$Test_1$	For test
14	N.C.	Not connected
15	OUT_1	Output die1
16	N.C.	Not connected

Table 4 - TSSOP-16 dual-die package pin definition and description

Pins Input and Test are internally grounded. For optimal EMC behaviour always connect the unused pins to the ground of the PCB.

4. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage(1)	V_{DD}			28 37	V	< 48h < 60s
Reverse Voltage Protection(1)	V_{DD-rev}	-14 -18			V	< 48h < 1h
Positive Output Voltage(1)	V_{OUT}			28	V	< 48h
Reverse Output Voltage(1)	$V_{OUT-rev}$	-14 -18			V	< 48h < 1h
Internal Voltage	V_{DEC}			3.6	V	
	$V_{DEC-rev}$	-0.3			V	
Positive Input pin Voltage	V_{Input}			6	V	
Reverse Input pin Voltage	$V_{Input-rev}$	-3			V	
Operating Temperature	T_{AMB}	-40		+160	°C	
Junction Temperature	T_J			+175	°C	
Storage Temperature	T_{ST}	-55		+170	°C	
Magnetic Flux Density	B_{max}	-1		1	T	

Table 5 - Absolute maximum ratings

Exceeding any of the absolute maximum ratings may cause permanent damage.

Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

5. Isolation Specification

Only valid for the TSSOP-16 package dual die version (code GO).

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Isolation Resistance	R_{isol}	4	-	-	MΩ	Between dice, measured between V_{SS1} and V_{SS2} with +/-20V bias

Table 6 - Isolation specification

[1] *Valid for full operating temperature range*

6. General Electrical Specifications

General electrical specifications are valid for temperature range [-40; 160] °C and supply voltage range [4.5; 5.5] V unless otherwise noted.

Electrical Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	V_{DD}	4.5	5	5.5	V	For regulator
Supply Current[2]	I_{DD}	9	11	13.5	mA	Analog/SPC output
Start-up Level (rising)	$V_{DDstartH}$	3.95	4.1	4.25	V	
Start-up Hysteresis	$V_{DDstartHyst}$	-	200	-	mV	
PTC Entry Level (rising)	V_{PROV0}[3]	6.30	6.55	6.80	V	
PTC Entry Level Hysteresis	$V_{PROV0Hyst}$	400	500	600	mV	
Output Short Circuit Current	$I_{OUTshort}$	-35 10		-10 35	mA	Vout = 0 V Vout = 5 V
Output Load	R_L	5	10		kΩ	Analog pull-up/ down
		3	-	55	kΩ	Push-pull and improved emission modes [4]
		1	-	100	kΩ	Open drain pull-up/down[4]
Digital open drain output level	$V_{satLoOd}$	0		10	$\%V_{ext}$	Pull-up to any external voltage $V_{ext} \leq 18V$, $I_L \leq 3.4mA$
	$V_{satHiOd}$	90		100	%VDD	Pull-down to GND with any supply voltage $V_{DD} \leq 18V$, $I_L \leq 3.4mA$
Digital output Ron	R_{on}	27	50	100	Ω	Push-pull mode
Analog Saturation Output Level [5]	V_{satA_lo}		0.5 3.3 2.3	1.2 7.4 5	%VDD	Pull-up load $R_L \geq 10$ kΩ to 5 V Pull-up load $R_L \geq 5$ kΩ to 18 V Pull-up load $R_L \geq 2$kΩ to 5 V
	V_{satA_hi}	97 95 87.5	99 98 96		%VDD	Pull-down load $R_L \geq 10$ kΩ Pull-down load $R_L \geq 5$ kΩ Pull-down load $R_L \geq 2$ kΩ

[2] The chip can also be configured to have lower current consumption, at the cost of speed. Contact Melexis for more details

[3] Programming through Connector (PTC) requires raising supply voltage above Vprov0 or Vprov1. This is customer configurable by setting a bit in the NVRAM

[4] Output resistance should be selected together with the output capacitive load to correspondingly match the application, i.e. tick time, SPC ID, to allow appropriate time window for the trigger pulse reception. More details see section 10.2.3.

[5] For analog output, see section 13.1.1.

Electrical Parameter	Symbol	Min	Typ	Max	Unit	Condition
Digital Output Level in push-pull mode [6]	V_{satD_lopp}			0.2 0.5	V	Pull-up load $R_L \geq 10$ kΩ Pull-up load 10 kΩ > $R_L \geq 5$ kΩ
	V_{satD_hipp}	V_{DD}-0.2 V_{DD}-0.5			V	Pull-down load $R_L \geq 10$ kΩ Pull-down load 10 kΩ > $R_L \geq 5$ kΩ
Digital Output Level in improved emission mode [6]	V_{satD_loie}			0.5	V	Pull-up load $R_L \geq 10$ kΩ
	V_{satD_hiie}	4.1			V	Pull-down load $R_L \geq 10$ kΩ
Active Diagnostic Output Level	Diag_lo		0.5 3.3 2.3	1.2 7.4 5	%V_{DD}	Pull-up load $R_L \geq 10$ kΩ to 5 V Pull-up load $R_L \geq 5$ kΩ to 18 V Pull-up load $R_L \geq 2$ kΩ to 5 V
	Diag_hi	97 95 87.5	99 98 96		%V_{DD}	Pull-down load $R_L \geq 10$ kΩ Pull-down load $R_L \geq 5$ kΩ Pull-down load $R_L \geq 2$ kΩ
Passive Diagnostic Output Level V_{SS} Broken-Wire Detection [7]	$BV_{SS}PD$		2.5 1	4 1.6	%V_{DD}	Pull-down load $R_L \leq 25$ kΩ Pull-down load $R_L \leq 10$ kΩ
	$BV_{SS}PU$	99.5	100		%V_{DD}	Pull-up load $R_L \geq 1$ kΩ
Passive Diagnostic Output Level V_{DD} Broken-Wire Detection [7]	$BV_{DD}PD$		0	0.5	%V_{DD}	Pull-down load $R_L \geq 1$ kΩ
	$BV_{DD}PU$	92.5 97	97.5 99		%V_{DD}	Pull-up load $R_L \leq 25$ kΩ Pull-up load $R_L \leq 10$ kΩ

Table 7 – Electrical Specifications

[6] *See section 13.1.1.*

[7] *Valid for dual-die configuration as well, i.e. TSSOP-16 package, where the two dies have the same supply and ground level, while the output of one die is connected with PU and the output of the other one is connected with PD. For detailed information, see also section 14.2.*

7. Timing Specification

Timing specifications are valid for temperature range [-40; 160] °C and supply voltage range [4.5; 5.5] V unless otherwise noted.

7.1. General Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Main Clock Frequency	F_{CK}	22.8	24	25.2	MHz	Including thermal and lifetime drift
Main Clock Frequency Thermal Drift	$\Delta F_{CK,T}$	-2.5	-	2.5	$\%F_{ck}$	Relative to 35°C
Main Clock Frequency Total Drift	$\Delta F_{CK,\ TOT}$	-3.5	-	3.5	$\%F_{ck}$	Relative to 35°C after factory trimming at Melexis, including thermal and lifetime drift
1MHz Clock Frequency	F_{1M}		1		MHz	
Intelligent Watchdog Timeout	T_{IWD}		4	(8)	ms	F_{CK} = 24MHz
Absolute Watchdog Timeout	T_{AWD}		2.7	(8)	ms	F_{1M} = 1MHz
Analog Diagnostics Test Interval (9)	DTI_{ANA}			3	ms	Diagnostics response time, detailed description see section 14.2, Table 40, for analog output
				9	SPC triggers	Diagnostics response time, detailed description see section 14.2, Table 40, for SPC output, e.g. with 500µs ECU frame time, the max. value is 4.5ms
Digital Diagnostics Test Interval (9)	DTI_{DIG}			4.5	ms	Diagnostics response time, detailed description see section 14.2, Table 40, for analog output
				9	SPC triggers	Diagnostics response time, detailed description see section 14.2, Table 40, for SPC output, e.g. with 500µs ECU frame time, the max. value is 4.5ms

Table 8 - General Timing Specifications

[8] *Maximum value is defined by the clock frequency tolerance, see parameter "Main Clock frequency".*

[9] *Only the Diagnostics response time is specified. The fault tolerance time interval (FTTI) should take into account the response time of the ECU additionally, i.e. on the item level, which is independent of the MLX91377.*

7.2. Timing Definitions

7.2.1. Startup Time

In SPC mode, during startup, the sensor transmits frames with status bit defined by the parameter SPC_SCN_INIT, until it is able to transmit valid magnetic measurements. These initialisation frames content can be chosen by user with the parameter SENT_INIT_GM (see chapter 11 for more detail).

7.2.2. Latency (average)

Latency is the average lag between the movement of the detected object (magnet) and the response of the sensor output, as shown in Figure 3, where theta_ECU(t) is sampled as the beginning of the synchronization pulse. This value is representative of the time constant of the system for regulation calculations.

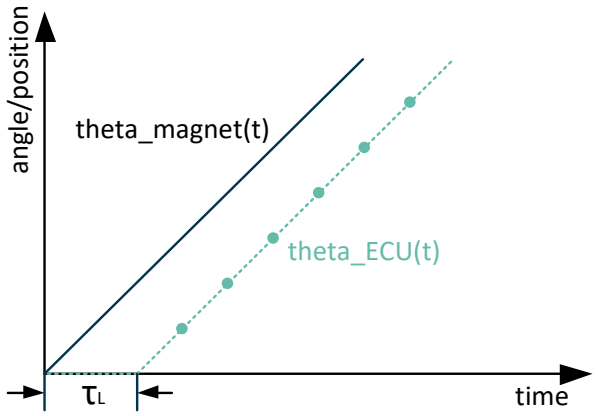


Figure 3 - Definition of Latency

7.2.3. Step Response (worst case)

The step response is a suitable metric for the "delay" of the sensor in case of an abrupt step in the magnetic change, considering 100% settling time without any DSP filter. Full settling is typically achieved in just two steps. The sensor is asynchronous with the magnetic step change: the 100% settling time will fall in a time window; worst case is illustrated in the figure below.

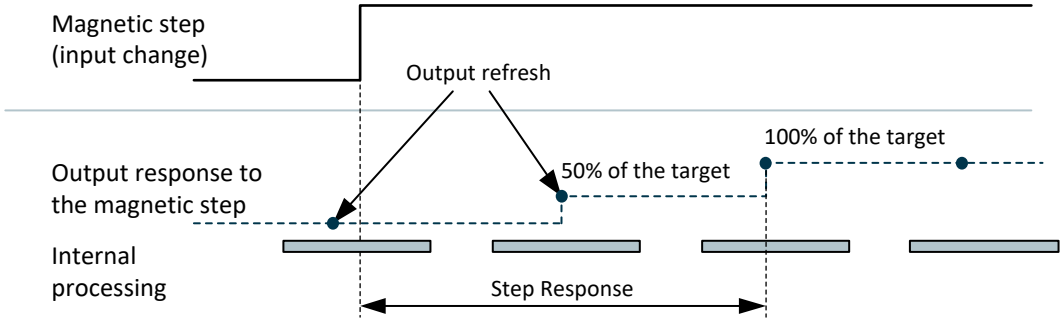


Figure 4 - Step Response Definition

Figure 4 is not valid for the SPC output, since the output is depending on the trigger pulse. The definition of the step response in SPC mode is clarified in Table 10.

7.3. Analog Output Timing Specification

For the analog output configurations, specifications are valid under the corresponding minimum and typical conditions defined in section 6. The timing specifications are listed in Table 9.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Output refresh period	τ_R		160		µs	
Latency	τ_L		70		µs	no external load
Step response	τ_S			250	µs	no external load
Start-up time	τ_{SU}		3.2		ms	
Slew Rate	SR		120 200		V/ms	capacitive load at output is 100nF capacitive load at output is 10nF

Table 9 - Analog General Timing Specifications

7.4. SPC Timing Specifications

In SPC mode, the MLX91377 starts data acquisition once the trigger pulse has been received, regardless of the configured mode. It will send the acquired data in the same SENT frame. This feature is available for any tick time greater than or equal to 1.5µs. Please check the section 10.2 for more details on the configuration options.

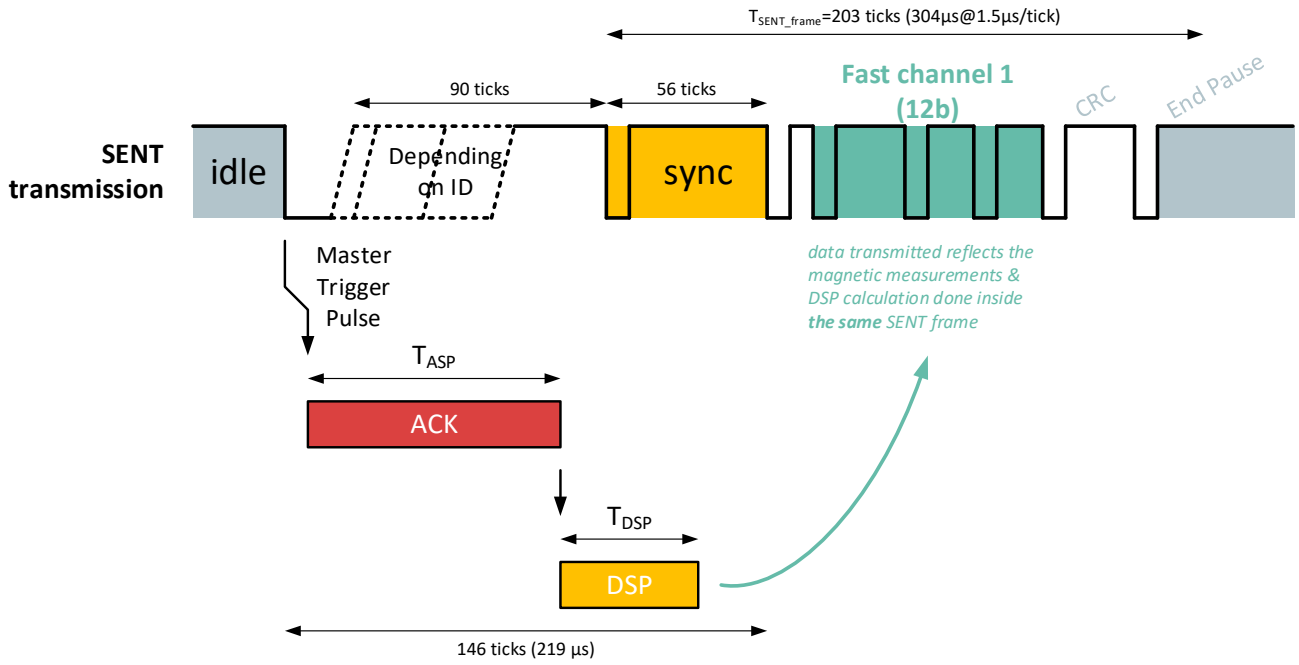


Figure 5 – SPC timing illustration in 1.5µs tick time mode and H.2 format

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Time between trigger received & acquisition started	T_{tr2acq}		10	(8)	µs	Tick: 1.5 µs SPC_RX_FILT_TIME [10]: 6 SPC_TRIG_TH: 0
Startup time (ability to	$T_{stupspc}$		3.5	3.9	ms	

[10] *SPC_RX_FILT_TIME is the parameter for the SPC trigger pulse filtering. Its unit is tick time. It must be aligned with the longest NIBBLE low time on the bus, in order to separate SENT pulses from SPC trigger pulses (NIBBLE_PULSE_FIXED[]).*

Parameter	Symbol	Min	Typ	Max	Unit	Condition
receive the 1st trigger pulse)						
Latency	T_{latcy}		450		µs	
Step Response (worst case)	T_{wcStep}			1	ms	The worst-case step response time is equal to twice a SPC trigger plus its SENT response time, when the field change happens right after the trigger pulse, see Figure 6. It is then 1 ms if the SPC trigger period is 0.5 ms.
Jitter between the acquisition	J_{acq}			5	µs	
Inter-die synchronicity		8.45	9.08	9.71	µs	The absolute time difference of the magnetic information acquisition between the two dice in bus transmission mode, see section 0, based on 1.5 µs tick time

Table 10 - SPC Mode Timing Specifications

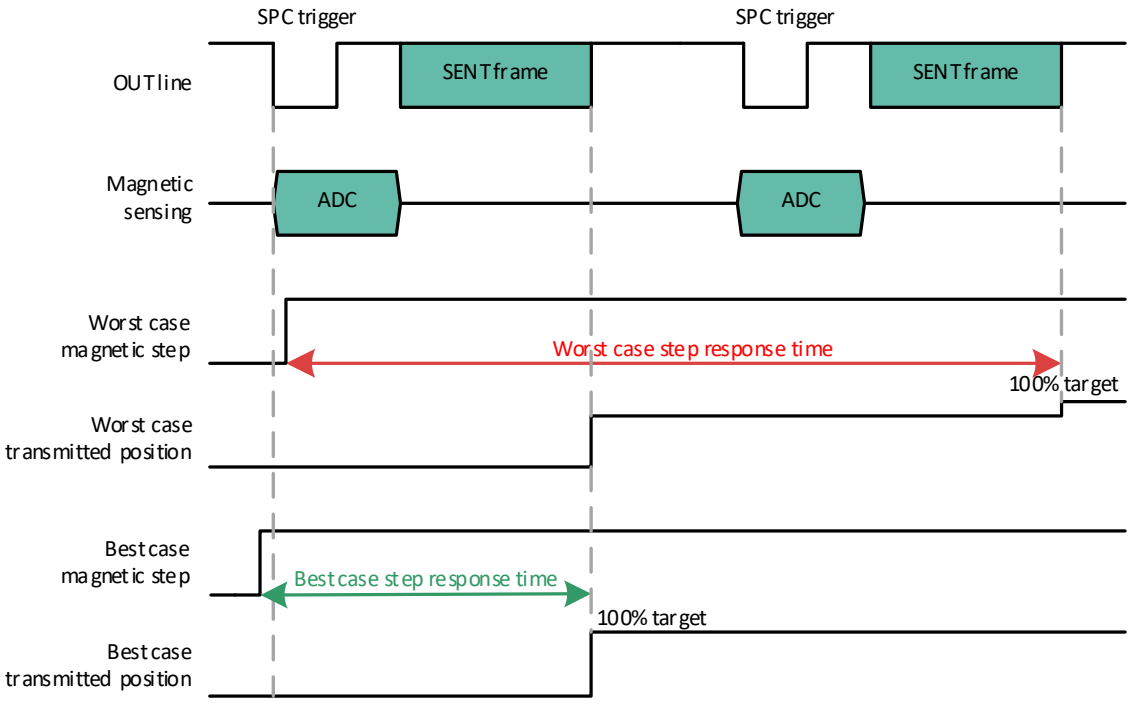


Figure 6 – Illustration of the best and worst case step response in SPC mode

8. Accuracy Specifications

Accuracy specifications are valid for temperature range [-40; 160] °C and supply voltage range [4.5; 5.5] V unless otherwise noted.

8.1. Definitions

This section defines several parameters, which will be used for the magnetic specifications.

8.1.1. Intrinsic Linearity Error

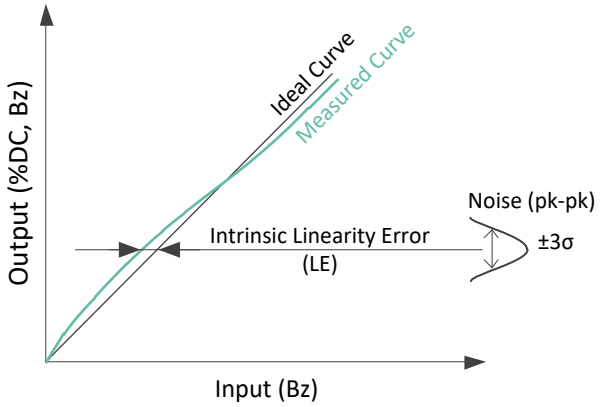


Figure 7- Sensor accuracy definition

The Illustration of Figure 7 depicts the intrinsic linearity error in new parts. The Intrinsic Linearity Error refers to the IC itself (offset, sensitivity) taking into account an ideal magnetic field. Once associated to a practical magnetic construction and the associated mechanical and magnetic tolerances, the output linearity error increases. However, it can be improved with the multi-point end-user calibration (see chapter 11). As a consequence, this error is typically negligible because it is calibrated away.

8.1.2. Total Drift

After calibration, the output field of the sensor might still change due to temperature change, aging, etc.. This is defined as the total drift ∂B_{TT} :

$$\partial B_{TT} = \max\{B(B_{IN}, T, t) - B(B_{IN}, T_{RT}, t_0)\}$$

where B_{IN} is the input field, T is the temperature, T_{RT} is the room temperature, and t is the elapsed lifetime after calibration. t_0 represents the status at the start of the operating life. Note the total drift ∂B_{TT} is always defined with respect to field at room temperature. In this datasheet, T_{RT} is typically defined at 35°C, unless stated otherwise. The total drift is valid for all fields along the full mechanical stroke.

8.2. Magnetic Field Specification for the Sensor Accuracy

The accuracy of the MLX91377 is valid with the external magnetic field specified in the below, and are valid for temperature range [-40; 160] °C unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Magnetic Input Span [11]		10	25	100	mT	|Bz|
System thermal drift	TCm	-3000			ppm/°C	

Table 11 - Magnetic field specification for the sensor accuracy

8.3. Accuracy Specifications

Offset, noise & sensitivity accuracy specifications enable quantification of the system's accuracy. Sensitivity drift is the IC thermal drift and the variation of the magnet drift.

8.3.1. Magnetic Accuracy

Please note the offset and noise are specified referring to the sensor output in Table 12. Therefore the specified values are based on the condition that the gain of the device (parameters GAIN and DIG_GAIN in Table 20) is properly adjusted to map the magnetic input span and chip output.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Thermal Output Offset Drift in full temperature range	$\Delta^T V_{OQ}$			11.2	LSB_{12}	± 10mT magnetic input span
				6.0		± 25mT magnetic input span
				3.9		± 40mT magnetic input span
				3.0		± 80mT magnetic input span
Initial Output Offset for room temperature 35°C [12]	V_{OQ}			10.0	LSB_{12}	± 25mT magnetic input span
Output Noise digital output RMS for room temperature 35°C [13]				2.85	LSB_{12}	± 10mT magnetic input span
				2.0		± 25mT magnetic input span
				2.0		± 40mT magnetic input span
				2.8		± 80mT magnetic input span
Output Noise analog output RMS for room temperature 35°C [13][14]				3.5	mV	± 10mT magnetic input span
				2.5		± 25mT magnetic input span
				2.5		± 40mT magnetic input span
				3.4		± 80mT magnetic input span

[11] This parameter indicates the magnetic field span which can be sensed at the device input. This parameter has an unsigned value, i.e. a device with magnetic input span of 10mT can detect a magnetic sensing field from -10mT to 10mT range. This parameter is mapped to the device gain, assuming the full scale of the output is used. For instance, a magnetic input span of 25mT reflects a device gain of 82LSB/mT (digital output) or 0.1V/mT (analog output). Therefore the device should be programmed with a gain which matches the magnetic span. Consequently, the condition for the accuracy specification in section 8.3 will also be changed accordingly.

[12] At time zero.

[13] RMS Noise. Valid for no filter.

[14] For the analog output, MLX91377 has the flexibility to offer a low noise product version (ASIC) via another product code, at the cost of speed reduction (see the parameter DTI_{ANA} in section 7.1 and the parameters in section 7.3). For the detailed performance and ordering information, please contact your Direct Sales Team.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Output Noise digital output RMS in full temperature range [13]				4.8 2.2 2.2 3.5	LSB_{12}	± 10mT magnetic input span ± 25mT magnetic input span ± 40mT magnetic input span ± 80mT magnetic input span
Output Noise analog output RMS in full temperature range [13][14]				6.0 2.7 2.7 4.3	mV	± 10mT magnetic input span ± 25mT magnetic input span ± 40mT magnetic input span ± 80mT magnetic input span
IC Sensitivity Drift	$\Delta^T S$	-1.5		1.5	%	Related to 35°C
Sensitivity Thermal Hysteresis		-0.5		0.5	%	Temperature cycling will impact sensitivity. Spec is for dry parts.
Integral non-linearity [15]	INL	-0.12 -0.25		0.12 0.25	%	35°C from -40 to 160°C
Temperature Sensor Variation [16]		-8 -2		8 6	°C	from -40 to 160°C from 35 to 125°C

Table 12 - Magnetic specification for Linear Hall Sensor

[15] Before end user calibration, measured at magnet span ±25mT, with 1mT resolution.

[16] Part to part variation of the temperature sensor

9. Memory Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
ROM	ROMsize		32		KB	1 bit parity check (single error detection)
RAM	RAMsize		1024		B	1 bit parity check (single error detection)
NVRAM	NVRAMsize		256		B	6 bits ECC (single error correction, double error detection)

Table 13 - Memory Specifications

10. Output Characteristic and Accuracy

10.1. Analog Output

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Thermal analog output Drift				0.2 0.3	%V_{DD}	up to 125°C up to 160°C
Analog Output Resolution	R_{DAC}		12		bit	12bit DAC (Theoretical)
		-4		+4	LSB_{12}	INL (before EoL calibration), output clamped between 3-97%VDD
		0.05	1	3	LSB_{12}	DNL
Ratiometric Error		-0.1		0.1	%V_{DD}	

Table 14 – Analog output accuracy

10.2. Digital Output

10.2.1. General Definition

The MLX91377 provides a digital output signal compliant with SAE J2716 Revised APR2016.

By default, the MLX91377 outputs the SPC (Short PWM Code). It is an extension of the SAE J2716 SENT protocol. It allows on-demand transmission of one data frame where the master triggers the transfer of data. The transmission of the SPC frame is always triggered by the master in every mode (synchronous and with ID selection). Both modes are described further in this chapter.

Optionally, the MLX91377 supports also the typical SENT revision 2016 (SAE J2716 APR2016) and compatible to the previous revisions [17].

The digital output of the MLX91377 transmits a sequence of data nibbles, according to the following configurations:

Description	Symbol	Min	Typ	Max	Unit	Description
Clock tick time	tickTime	0.5	1.5[17]	12	µs	Main use cases : SPC, 1.5µs tick time (default) Normal SENT, 3µs tick time Slow SENT, 6µs tick time (see section 7.4)
Number of data nibbles	Xdn	3		6		
Frame duration (no pause pulse)	Npp	154		270	ticks	6 data nibbles

[17] *Please contact our Direct Sales Team if other options then main use cases is required.*

Description	Symbol	Min	Typ	Max	Unit	Description
Frame duration with pause pulse	Ppc	282	320	922	ticks	
Sensor type	A.3					Single Secure sensors

Table 15 - SENT Protocol Frame Definition

10.2.2. Tick Time requirements

The basic SPC protocol unit time is defined as 3 µs. The protocol standard requires a tick time variation of no more than 20% for legacy applications and 10% for general applications. The lowest tick time that can be programmed in the MLX91377 is 0.5 µs. Improved Emission Mode will only be possible for tick time equal or greater to 1.5 µs.

10.2.3. Output Configuration

In SPC mode, the MLX91377 can be configured in open drain mode, normal push-pull mode, as well as an enhanced emission mode, see also section 13.1.1.

The default output driver configuration is to send the SENT frame in push-pull mode.

Users can select three options (see parameter SPC_PP_Option, Table 20 in chapter 11):

1. IC is always in open drain
2. IC sends the SENT frame from a pre-defined timer (SPC_OUT_ON_TH) to CRC in push-pull. It then returns to high-Z
3. IC sends the SENT frame from a pre-defined timer (SPC_OUT_ON_TH) until end of a pre-defined timer (SPC_OUT_OFF_TH). It then returns to high-Z.

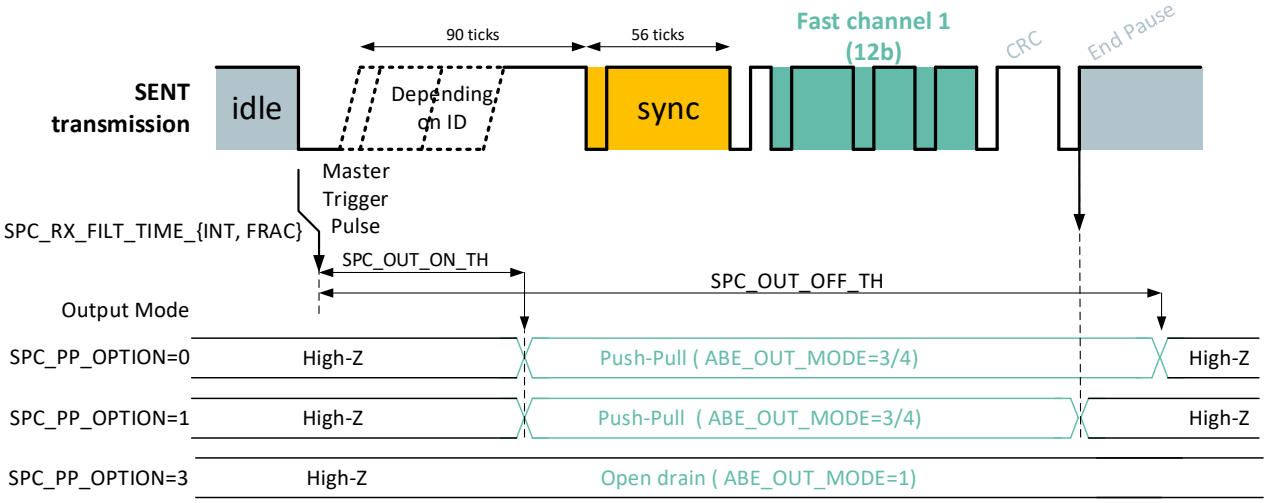


Figure 8 – SPC output driver state switching

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Push-Pull Duration	$T_{push-pull}$	280		550	µs	Configurable Duration how long IC stays in push-pull once sync pulse of SENT frame starts.

Table 16: Push-pull duration in SPC mode

The sensor output driver can also be configured as open-drain to enable the master to drive the line. Initially the line is at high level, the chip is waiting for the master to pull it low. This state is called 'Idle

state', meaning the sensor is not transmitting any data. At a given time, the master will send a trigger low pulse along the line. The embedded CPU of the sensor will measure this master pulse length. If it is recognized as a valid trigger, the chip will answer by sending back an SPC frame containing the current data. Several configurations of the SPC frame are available. If the trigger pulse is not valid, the chip will not transmit any data, keeping the line free.

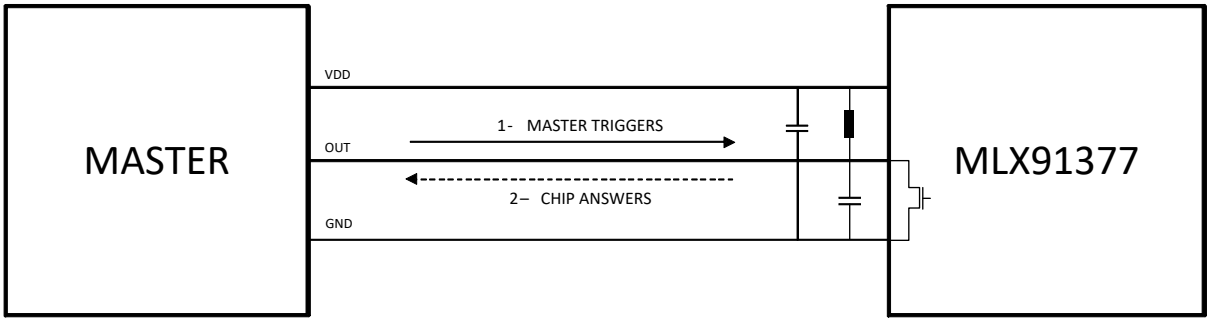


Figure 9 – SPC standard master-slave configuration

Like in SENT, the tick time is the unit reference for SPC. It can be as low as 0.5µs enabling fast transmission rate and short frames. However, the default tick time value is 1.5µs in SPC mode, to benefit from the fast acquisition and magnetic processing of the device.

For the MLX91377, the output resistance, e.g. the external pull-up or pull-down resistor should be carefully selected, because the MLX91377 has a built-in high order low pass filter, too heavy resistive load will deteriorate the generated SPC signal, and could make the output signal not comply to the SPC specifications, such as the fall times and the minimum output voltages, i.e. parameters $V_{satD\_lopp}/V_{satD\_hipp}$ and $V_{satD\_loie}/V_{satD\_hiie}$ in Table 7 in chapter 6. In principle, the values in Table 7 in chapter 6 should be considered, which means it is not recommended to have a resistive load value smaller than 10kΩ, and a resistive load value smaller than 3kΩ should be avoided. The maximum output resistive load value should be less than 55kΩ to avoid unexpected impact from leakage current.

Furthermore, the output capacitance should also be properly chosen together with the output resistive load to correspondingly match the application, e.g. tick time, SPC ID, etc. to allow appropriate time window for the trigger pulse reception. The worst case scenario occurs for SPC ID0, where the trigger pulse should be recognized within only 4 ticks (refer to Table 19 and Figure 14 in section 0), resulting in 6 µs time window for 1.5 µs tick time SPC protocol. Therefore, RC time constant should be less than 6 µs in such application. When the time window for the trigger pulse reception changes, the resistive and capacitive load on output can be scaled correspondingly. It is also important to note that the mentioned capacitive load refers to the total load on the bus, meaning the value should be equally divided if there are multiple sensors connected, also the load on the ECU side should be taken into account and scaled properly.

10.2.4. Frame Content

10.2.4.1. Global Definition

A message frame consists of the following sequence:

1. Trigger pulse
2. Synchronization pulse
3. Status and communication nibble

4. Data nibbles
5. Checksum nibble
6. End Lone pulse

The overall scheme of the SPC frame transmission is described in the following figure.

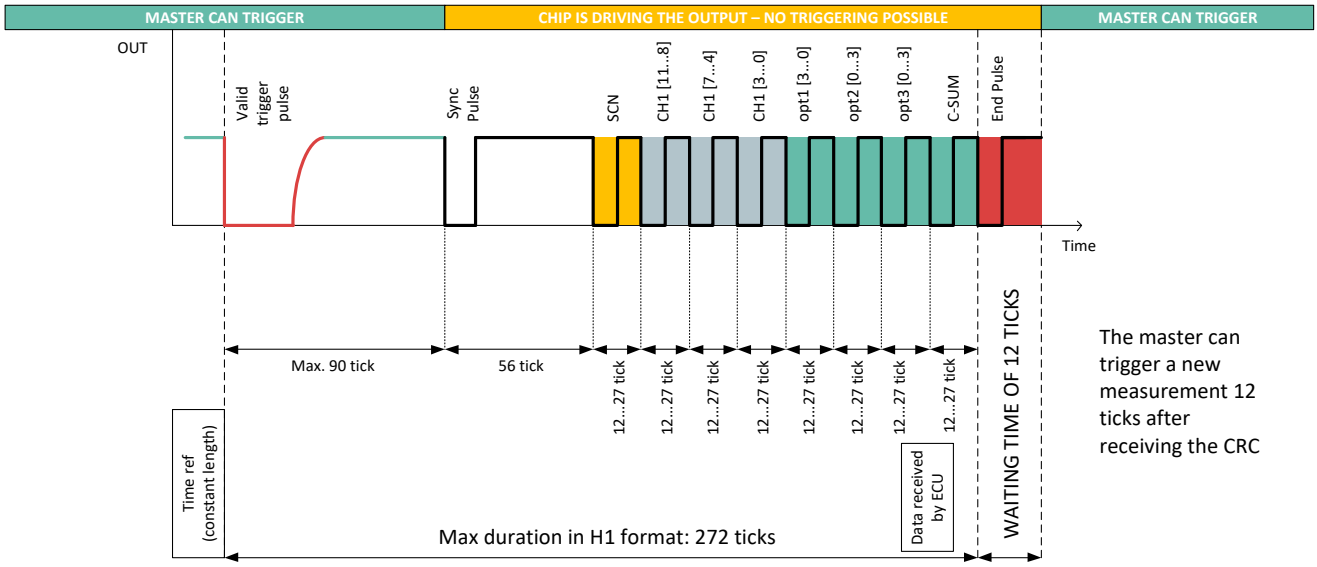


Figure 10 - SPC Frame description

10.2.4.2. Trigger Pulse

The trigger pulse is considered to be part of the SPC frame. The timing related to this trigger pulse is critical as it is initializing the data transfer. The sensor is monitoring the line and computes the duration the line is kept low by the master. This time is called “master low time”.

Parameter	Symbol	Min	Typ	Max	Unit
Falling edge threshold	V_{thfSPC}	1.1	1.32	1.7	V
Rising Edge Threshold	V_{thrSPC}	1.25	1.52	1.8	V

Table 17 – SPC Master Trigger Pulse Specifications

The falling edge of the trigger pulse is considered to be the reference of the protocol. The master low time is quantized using clock ticks.

After a non-valid trigger detected, a blanking time of five unit times (counted from the detected rising edge of the trigger pulse) is used by the sensor, before the next trigger measurement is performed. This concept improves EMC robustness and avoids unwanted answer from the chip if the line is subject to spikes.

After detection of a valid trigger and expiration of the trigger pulse time according to the selected transmission mode the sensor starts with the remaining protocol frame.

10.2.4.3. Status and communication nibble (SCN)

The status nibble contains information for error reporting and some optional information like the chip ID or slow channel data.

The position of the 2 status bits and 2 ID bits in SPC mode of MLX91377 complies with the one specified in the SPC standard, but can be reversed if the SENT-standard definition is preferred.

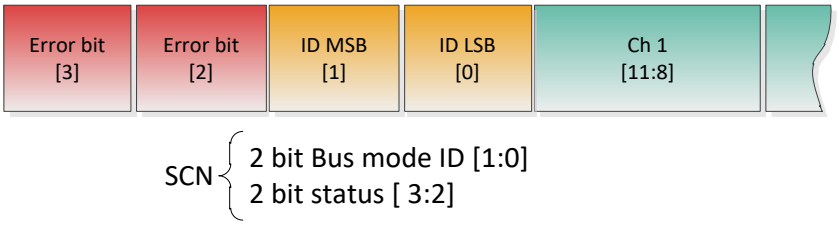


Figure 11 – SPC Bus Transmission Mode Multiplex Example (SPC_SCN_BIT_ORDER=1)

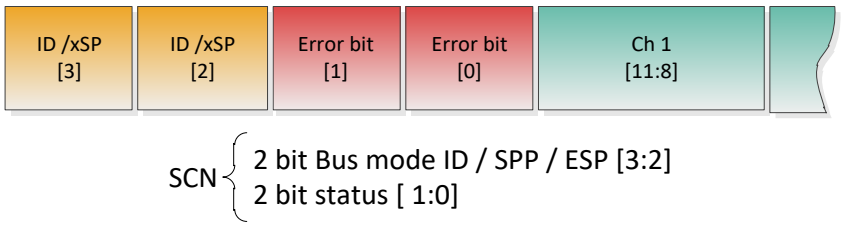


Figure 12 – SENT Transmission Mode Multiplex Example (SPC_SCN_BIT_ORDER=0)

10.2.4.4. Data Nibble

The definition of the data nibbles in SPC matches with SENT. The number of data nibbles transmitted is determined by frame format configured. The data content is programmable. By default, 12 bits of data are transmitted in 3 nibbles.

10.2.4.5. Checksum Nibble

SPC protocol allows transmission of error/warning flags in the status and communication nibble. Then it is highly recommended to take this nibble into the checksum calculation. This option is programmable in the MLX91377. Nevertheless, to be SENT compatible, it is possible to limit the checksum input data to data nibbles only.

MLX91377 also supports the SPC improved nibble checksum algorithms (for the SENT nibbles), method-E and method-O.

10.2.4.6. End Lone Pulse

The MLX91377 generates a pulse with a length of 12 clock ticks after transmission of checksum nibble. In that case the master cannot trigger the chip. During that period, MLX91377 is still holding the line. The blanking time is programmable, see parameters SPC_OUT_ON_TH, SPC_OUT_OFF_TH in chapter 11.

10.2.5. Synchronous Transmission Mode

In the SPC synchronous mode, the sensor responds to a low pulse of duration between 1.5 and 4 tick times. The SENT data frame shall be transmitted with a delay of 10 tick times such that the allowed total

trigger time range specified in Table 18 is met. This configuration ensures synchronisation between the master and the chip, and the data gets acquired in the same frame.

Parameter	Symbol	Min	Typ	Max	Unit
SPC Synchronous Mode Trigger Low Time	$t_{mlowSPC}$	1.5	2.75	4	ticks
Total trigger time	t_{mtrSPC}	10.8	13.5	16.3	ticks

Table 18 – SPC Synchronous Timings

10.2.6. Bus Transmission Mode

In the on-demand timing modes, the sensor responds to SPC trigger pulses from the master when its low pulse time corresponds to its pre-programmed ID. The selection of the ID is done with the parameter SPC_ID.

Parameter	Symbol	SPC_CHIP_ID	Min	Typ	Max	Unit	Remark
Bus Mode Master Low Time	$t_{mlowSPC}$	0	8		15	ticks	
		1	16		28	ticks	
		2	29		49	ticks	
		3	50		82	ticks	
Total trigger time	t_{mtrSPC}	-	-	90	-	ticks	master trigger pulse, independent of SPC_ID, not programmable

Table 19 – Bus Transmission Mode Timings

The ECU is able to trigger only one chip on a bus. The maximum amount of chip on the bus line is 4. Each chip must have its output configured to open-drain with a different ID.

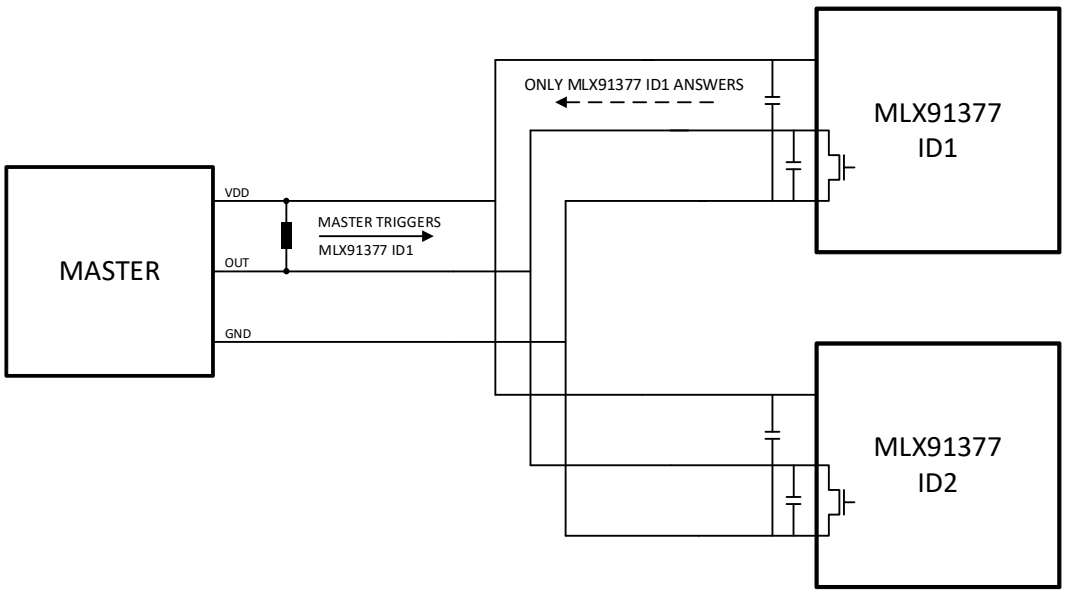


Figure 13 – SPC Bus Transmission Mode Multiplex Example

Figure 14 shows the timing diagram of the trigger pulse reception depending on the SPC ID.

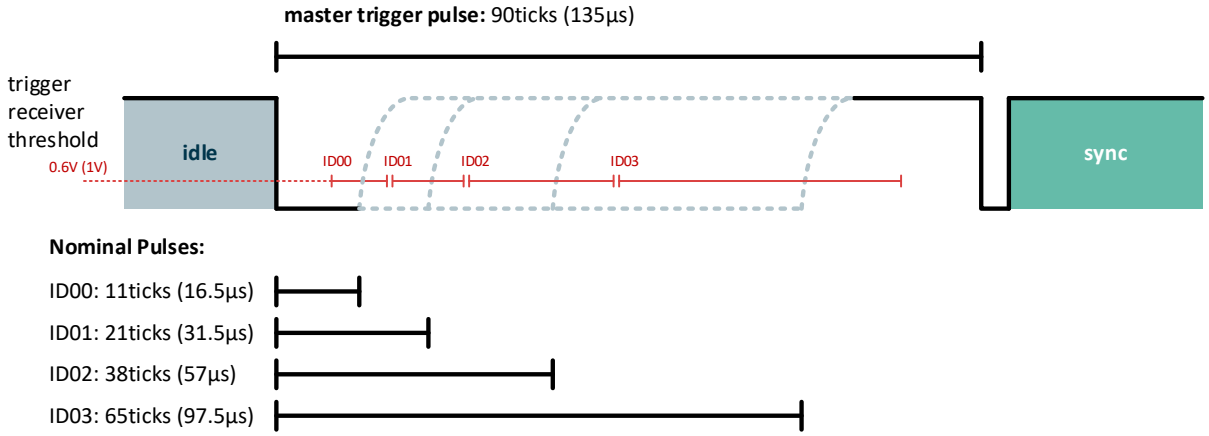


Figure 14 – Time Window for the Trigger Pulse Reception

Notes:

- ID01 and ID03 are advised when only 2 sensors are on the bus
- For correct trigger pulse reception, the clock tolerance of the sensor, the time constant of the rising edge and the receiver threshold shall be considered
- The ECU may adjust the low trigger time to account for the time constant of the rising edge
- Example timings are calculated for the default 1.5µs tick time

Bus Transmission Mode allows two configurations for acquiring data and sending data:

1. The IC for which SPC ID matches acquires its data and sends in the same frame the data.
2. All IC's on the bus acquire the data when a specific SPC ID is sent. Each IC buffers and transmits when called upon, see Figure 15.

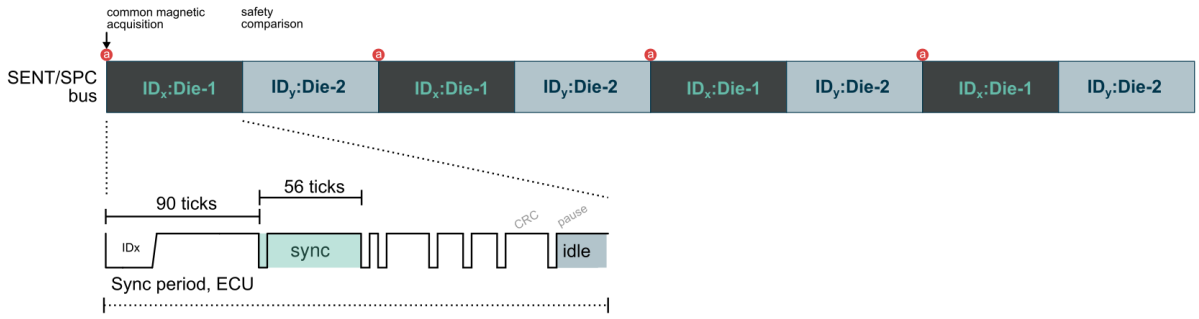


Figure 15 – Acquire Data during one SPC ID on all ICs on the same bus. Buffer and send when SPC ID matches.

10.2.7. Programming in Bus Mode

The EoL programming can be executed even if 4 chips are connected to the same bus. The protocol is capable of selective communication with one chip connected in bus configuration together with other chips (up to 4 on the same line). It uses the MUPET_ADDRESS stored in NVRAM to select the chip to be programmed. When programming 4 chips in parallel, external serial resistors shall be avoided, and are in fact not needed, as the improved emission mode is addressing the additional filtering via a resistance implemented on chip. It enables EoL programming even if 4 chips are connected to the same bus. The SPC ID must be programmed up front. Discuss with your local sales representative for this option.

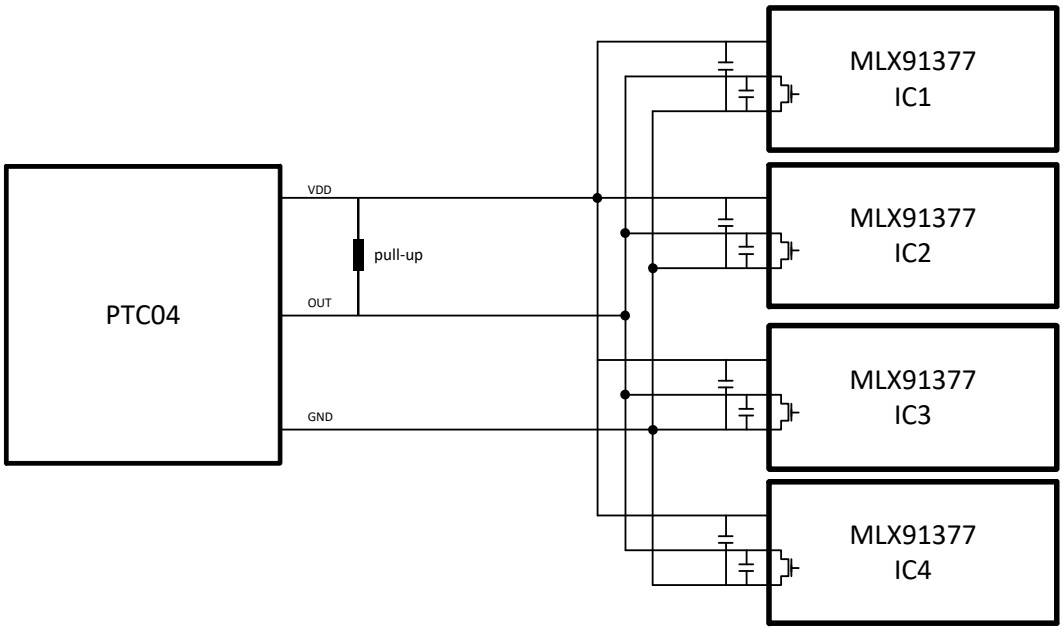


Figure 16 – Example of multiple units programming

11. End-User Programmable Items

Parameter	Description	Default Values SPC	Analog	#bits
	GENERAL CONFIGURATION			
USER_ID[0..5]	User Id. Reference, details see Table 21 in chapter 12	see Table 21 in chapter 12		8
WARM_TRIGGER_LONG	Add delay for PTC Entry Level	0	0	1
WARM_ACT_HIGHV	Select PTC Entry Level Default 0 = V_{PROV0}	0	0	1
ROUT_LOW	Select output impedance for PTC communication	1	1	1
MUPET_ADDRESS_MODE	Configuration for PTC address. Do not modify!	0	0	1
MUPET_ADDRESS	PTC address for which the slave will communicate	0/1	0/1	2
MEMLOCK	Enable NVRAM write protection	0	0	2
	SENSOR FRONT END			
MAGNET_SREL_TC	Linear magnet TC correction: -1525ppm/(°C * 100LSB)	0	0	8
MAGNET_SREL_DT [1..7]	Piecewise linear magnet TC correction, delta vs Linear magnet TC correction (MAGNET_SREL_TC)	0	0	8
GAIN	Analog Virtual gain code [0..63]	29	29	8
SENSING_MODE	Sensing mode: Bz = Fixed for Linear Hall application	7	7	3
	FILTERING			
FILTER	FIR filter bandwidth selection	0	0	2
HYST	Hysteresis of the denoising filter (hides the small variations but lowers the resolution) Denoising and FIR filtering are applied before the linearization step.	0	0	8
DENOISING_FILTER_ALPHA_SEL	Select the alpha parameter of the EMA (IIR) filter	0	0	2
SPC_RX_FILT_TIME_INT SPC_RX_FILT_TIME_FRACT	Filtered SPC trigger pulse: Min pulse tick time = (8* SPC_RX_FILT_TIME_INT + SPC_RX_FILT_TIME_FRACT)/8	6 0	N/A	4 3
SPC_BLANKING_TIME	SPC blanking time (= 5+2*SPC_BLANKING_TIME tick) in case of invalid SPC -ID pulse detected, counted from the rising edge of the trigger pulse. Any other (parasitic) pulse occurring during that time will be ignored.	0	N/A	2
	LINEAR TRANSFER CHARACTERISTIC			
OFFSET	Quiescent position for PWL linearization, default 50%	32768	32768	16
Polarity	Enable reverse output polarity selection	0	0	1
4POINTS	Enable 4 points PWL linearization	0	0	1
DSP_LNR_RESX2	Enable a doubled LNR method 0: 4-points or 16-segments 1: 8-points or 32-segments	0	0	1

Parameter	Description	Default Values		
		SPC	Analog	#bits
DIG_GAIN	Post DSP Gain stage, input range for PWL linearization FS: +/- 2^15 *16/DIG_GAIN [typ +/- 100 mT *16/ DIG_GAIN]	16	16	8
GAIN_ANCHOR_MID	Select 50% position as anchor point Post DSP Gain stage	1	1	1
USEROPTION_SCALING	Enables output scaling x2 0 = [0..100%] 1 = [-50%..150%]	1	1	1
LNR_S0	4-pts – Slope coefficient before reference point A	N/A	N/A	16
LNR_A_X, LNR_B_X, LNR_C_X, LNR_D_X	4-pts - X coordinate for reference points A,B,C,D	N/A	N/A	16
LNR_A_Y, LNR_B_Y, LNR_C_Y, LNR_D_Y	4-pts - Y coordinate for reference points A,B,C,D	N/A	N/A	16
LNR_A_S, LNR_B_S, LNR_C_S, LNR_D_S	4-pts – Slope coefficient for reference points A,B,C,D	N/A	N/A	16
LNR_Y00	8-pts / 16 segments - Y coordinate point 0	0x4009	0x4CCD	16
LNR_Y01	8-pts / 16 segments - Y coordinate point 1	0x4804	0x5334	16
LNR_Y02	8-pts / 16 segments - Y coordinate point 2	0x5000	0x599A	16
LNR_Y03	8-pts / 16 segments - Y coordinate point 3	0x57FC	0x6000	16
LNR_Y04	8-pts / 16 segments - Y coordinate point 4	0x5FF8	0x6667	16
LNR_Y05	8-pts / 16 segments - Y coordinate point 5	0x67F4	0x6CCD	16
LNR_Y06	8-pts / 16 segments - Y coordinate point 6	0x6FF0	0x7334	16
LNR_Y07	8-pts / 16 segments - Y coordinate point 7	0x77EC	0x799A	16
LNR_Y08	8-pts / 16 segments - Y coordinate point 8	0x7FE8	0x8000	16
LNR_Y09	8-pts / 16 segments - Y coordinate point 9	0x87E4	0x8667	16
LNR_Y10	8-pts / 16 segments - Y coordinate point 10	0x8FE0	0x8CCD	16
LNR_Y11	8-pts / 16 segments - Y coordinate point 11	0x97DC	0x9333	16
LNR_Y12	8-pts / 16 segments - Y coordinate point 12	0x9FD8	0x999A	16
LNR_Y13	8-pts / 16 segments - Y coordinate point 13	0xA7D4	0xA000	16
LNR_Y14	8-pts / 16 segments - Y coordinate point 14	0xAFD0	0xA667	16
LNR_Y15	8-pts / 16 segments - Y coordinate point 15	0xB7CC	0xACCD	16
LNR_Y16	8-pts / 16 segments - Y coordinate point 16	0xBFC8	0xB333	16
LNR_X[00..07]	8-pts - X coordinate point 0..7	N/A	N/A	16
LNN_DELTA_Y[00..32]	32 segments - Delta Y coordinate point 0..32	N/A	N/A	8
LNR_DELTA_Y_EXPAND_LOG2	Adjust the span of 32 segments NV_LNR_DELTA_Y{n} offsets	0	0	2
CLAMPLOW	Low clamping value of field data	16	32767	16
CLAMPHIGH	High clamping value of field data	65408	32767	16
OUTSLOPE_SEL	Possible output offset correction within the post-DSP chain:	0	0	2

Parameter	Description	Default Values		
		SPC	Analog	#bits
	0: disabled (default) 1: enabled, applied after discontinuity point stage 2: enabled, applied before clamping stage 3: disabled (unused)			
OUTSLOPE_COLD	Slope coefficient at cold of the programmable temperature-dependent offset. Used only if NV_OUTSLOPE_SEL enabled	0	0	8
OUTSLOPE_HOT	Slope coefficient at hot of the programmable temperature-dependent offset. Used only if NV_OUTSLOPE_SEL enabled	0	0	8
	DIAGNOSTICS			
DIAG_GLOBAL_EN	Diagnostics global enable. **Do not modify!** (see section 14.2 Safety Mechanisms)	1	1	1
DIAG_TEMP_THR_LOW	Temperature threshold & limiter for lower-temperature diagnostic. Default=08 -> -57 deg.C	8	8	8
DIAG_TEMP_THR_HIGH	Temperature threshold & limiter for over-temperature diagnostic. Default=128 -> 183 deg.C	128	128	8
DIAG_FIELDTOOHIGHTHRES	Field strength limit over which a fault is reported. (see 13.5.4)	255	255	8
DIAG_DEBOUNCE_STEPDOWN	Diagnostic debouncing stepdown time used for recovery time setting	1	1	4
DIAG_DEBOUNCE_STEPUP	Diagnostic debouncing stepup time used for hold time setting	1	1	4
DIAG_DEBOUNCE_THRESH	Diagnostic debouncing threshold	1	1	6
COLD_SAFE_STARTUP_EN	Normal (0) or safe start-up (1) after power-on reset	0	0	1
OUT_ALWAYS_HIGHZ	Forces the OUT pin in high-Z mode (for test mode, **Do not modify!)**	0	0	1
SENT_REPORT_MODE_ANA	1: Enables the error message within SENT/SPC frame in ANA diagnostic mode. See DIAG_FAULT_CODE	0	N/A	2
DIAG_FAULT_CODE	Defines the error message = DIAG_FAULT_CODE + FF8	6	N/A	3
DAC_REPORT_MODE_ANA	Defines the DAC state in analog-fault report mode	N/A	0	2
SENT_INIT_GM	Initialization frame definition until first valid data 0: 000 1 : DIAG_FAULT_CODE + FF8	0	N/A	1
SPC_SCN_INIT	SCN nibble Initialization contents until first valid data	0	N/A	0
OUT_DIAG_HIZ_TIME	Output Digital failure (HiZ) recovery time. = 6 + OUT_DIAG_HIZ_TIME ms	0	0	5
	OUTPUT CONFIGURATIONS			
PROTOCOL	Output protocol selection 3: SPC (with or without ID) 4: Analog output	3	4	3
ABE_OUT_MODE	HW backend output-amplifier mode selection 0: Analog output (12 bit) 4: Digital output with improved emission	4	0	3
ABE_DAC_SEQ_BYPASS	DAC sequencer bypass option	0	1	1

Parameter	Description	Default Values		
		SPC	Analog	#bits
DAC_SEQ_LUT_SEL	DAC Sequence LUT, default for 1.5 usec. **Do not modify!**	1	N/A	4
NV_DAC_SEQ_CLK_DIV	DAC Sequence Clock, default for 1.5 usec. **Do not modify!**	0	N/A	3
NIBBLE_PULSE_CONFIG	Sets the SENT nibble high/low-time configuration 2: 5 fixed ticks low time (Default) 3: 6 fixed ticks high time	2	N/A	2
SPC_PP_OPTION	SPC push-pull and high-Z switching option 0: switch on Push-pull mode @ SPC_OUT_ON_TH , switch it off @ SPC_OUT_OFF_TH (PROTOCOL = 3) 1: switch on Push-pull mode @ SPC_OUT_ON_TH, switch it off right after the last rising edge of the pause pulse. (PROTOCOL = 3) 2: Permanent High-Z (do not use) 3: Permanent state defined by NV_ABE_OUT_MODE (to be used for analog , PWM & SENT)	0	3	2
SPC_OUT_ON_TH	Tick delay between the SPC trigger falling edge and the output mode switch: open-drain -> push-pull. Note: tmlowSPC - SPC_RX_FILT_TIME_INT < SPC_OUT_ON_TH < 90	0x32	N/A	9
SPC_OUT_OFF_TH	Tick delay between the SPC trigger falling edge (filtered) and the output mode switch: push-pull -> open-drain.	450	N/A	9
	SPC PROTOCOL OPTIONS			
SENT_TICK_TIME	SENT tick duration 3 = 1.5 µs	3	N/A	3
SPC_ID_EN	0: SPC without ID selection 1: SPC with ID selection. See SPC_CHIP_ID (default)	1	N/A	1
SPC_CHIP_ID	SPC trigger ID upon which the SENT response will be transmitted on the bus.	0: Die1 1: Die2	N/A	2
SPC_MEAS_ID	SPC trigger ID upon which the ADC measurement will be done	1	N/A	2
SERIAL_CONFIG	Used for SCN configuration, **do not modify! See ID_IN_STATUS** 1: NSP, 2 bits are overlaid with SPC_CHIP_ID 2: SSP 3: ESP	1	N/A	2
ID_IN_STATUS	Enable SPC ID in SCN (status and communication nibble)	1	N/A	1
SPC_SCN_BIT_ORDER	Enables SCN bit order according to SPC 1: [b3:2] = Error indication , [b1:0] = SPC_CHIP_ID	1	N/A	1
SPC_TRIGGER_MODE	SPC trigger pulse treatment mode: 0: Synchronous Transmission Mode 1: Bus mode with constant length trigger pulse (default)	1	N/A	2
SPC_FORMAT	SPC frame sequence: 0: data + checksum (default) 8: see NV_SENT_FC_FORMAT[2:0]	0	N/A	4

Parameter	Description	Default Values		
		SPC	Analog	#bits
SPC_FC_CSUM_CFG	Fast-channel checksum calculation method 0: checksum in line with SAE J2716 (default) 1: Method "O" in line with SPC2014 Specification 2: Method "E" in line with SPC2014 Specification	0	N/A	2
SENT_LEGACY_CRC	Enable legacy CRC calculation 0: The SAE J2716 recommended CRC is calculated	0	N/A	1
STATUS_IN_CRC	1: Add SCN in checksum calculation	1	N/A	1
SPC_CSUM_MODE	Checksum nibble calculation mode in SPC: 0: checksum only (default) 1: Add ID in checksum 2: Add ID & RC in checksum	0	N/A	2
SPC_BLANK_SENT_FRAME	reserve	0	N/A	1
SPC_TRIG_TH	Delay between the filtered SPC trigger falling edge and the ADC start of sequence, given in number of tick.	0	N/A	9
	SENT PROTOCOL OPTIONS			
SENT_FC_FORMAT	SENT format option (only if NV_SPC_FORMAT = 8) 1: Format H.1 (A.1 , Two 12-bit Fast Channels) 2: Format H.2 (One 12-bit Fast Channel, 3 x 4 bit) 3: Format H.3 (One 12-bit fast channel, 4 x 3 bit) 4: Format H.4 (A.3, 12-bit Fast Channel & Single secure) 5: Format H.5 (12-bit Fast Channel & zero values) 6: Format H.6 (14-bit Fast Channel1 & 10-bit Fast Channel2) 7: Format H.7 (16-bit Fast Channel & 8-bit Fast Channel2)	N/A	N/A	3
TWO_ANGLES_FRAME	Enable 2 fields measure per output frame (SENT with pulse)	N/A	N/A	1
T_FRAME	SENT w/ PP frame length (overlaid w/ SPC_OUT_ON_TH)	N/A	N/A	12
T_SYNC_DELAY	SENT - ADC synchronization delay - used in SENT-with-pause only	N/A	N/A	12
SENT_FAST_CHANNEL_2	Definition of data transmitted in the SENT fast channel 2 in case SENT_FC_FORMAT=1, 6 or 7 0 Temperature sensor (SP ID 0x23) 1 0xFF9(d4089) - CH1 2 RAM data (RAMPROBE_PTR) 3 0xFFF(d4095) - CH1	N/A	N/A	2
SENT_SLOW_EXTENDED	ESP length configuration, Not used for this order code	N/A	N/A	1
SENT_SLOW_EXTENSION	ESP length configuration, Not used for this order code	N/A	N/A	2
SENT_DIAG_STRICT	ESP error configuration, Not used for this order code	N/A	N/A	1

Table 20 - MLX91377 End-User Programmable Items Table

Performances described in this document are only achieved by adequate programming of the device. To ensure desired functionality, Melexis recommends to follow its programming guide and to contact its technical or application service.

12. End-User Identification Items

Parameter	Description	Default Values		
		SPC	analog	#bits
USER_ID0	Bin1 from production test, can also be reserved for end-user to program information to keep traceability		1	8
USER_ID1	Free for end-user to program information to keep traceability	N/A	N/A	8
USER_ID2	Free for end-user to program information to keep traceability		N/A	8
USER_ID3	Free for end-user to program information to keep traceability		N/A	8
USER_ID4	Free for end-user to program information to keep traceability		N/A	8
USER_ID5	Free for end-user to program information to keep traceability		N/A	8
IMC_VERSION	IMC / application type: 3: no IMC (linear Hall)		3	6
TEST_STATUS	Bin 1 verification bit		1	1
MLX_ID0	X-Y position on the wafer (8 bit each)		MLX	16
MLX_ID1	Wafer ID [b15..11] Lot ID [b10..0]		MLX	16
MLX_ID2	Fab ID (4 bits) Test Database ID (6 bits)		MLX	16

Table 21 - Melexis and Customer ID fields description

User identification numbers (48 bits) are freely usable by customers for traceability purpose. Other IDs are read only.

13. Description of End-User Programmable Items

13.1. Output modes

13.1.1. OUT mode (ABE_OUT_MODE and ABE_DAC_SEQ_BYPASS)

Defines the Output Stage mode (outside fail-safe state) in application.

ABE_OUT_MODE	ABE_DAC_SEQ_BYPASS	Description
0	1	Analog output (12-bit DAC)
1	1	Digital output with open-drain-NMOS (requires a pull-up resistor on output)
2	1	Digital output with open-drain-PMOS (requires a pull-down resistor on output)
3	1	Digital output with Push-Pull
4	0	Digital output with improved emission

Table 22 - Output Mode Selection

13.1.2. Digital OUT Protocol (PROTOCOL)

Selection of the measurement timing mode and the corresponding output protocol.

PROTOCOL	Descriptions
0	Continuous asynchronous field acquisition, SENT without pause
1	Continuous asynchronous field acquisition, PWM
2	Continuous synchronous field acquisition, SENT with pause
3	Master-triggered field transmission, SPC (with or without ID)
4	Continuous asynchronous field acquisition, analog output (DAC)

Table 23 - Protocol Selection

13.1.3. SPC Frame Formats

The MLX91377 revision provides the full choice of SPC & SENT frame selection according to SPC2013 frame configuration & SAE J2716, appendix H1-7.

Below is an overview of the SPC_FORMATS:

Figure 17 – SPC Frame Format details

13.2. Sensor Front-End

Parameter	Value
SENSING MODE	[0..7]
GAIN	[0..63]

Table 24 - Sensing Mode and Front End Configuration

13.2.1. SENSING MODE

The SENSING_MODE parameter defines which Hall Elements are used to measure the Bz field. The different possibilities are described in the tables below, although it is advised to keep the default setting.

MAPXYZ	B	Angular
0-4, 6	N/A	Reserved (do not use)
5	$Z_{HEcenter}$	reserved mode, not recommended to use
7	Z_{HEedge}	Linear hall mode

Table 25 - Sensing Mode Description

13.2.2. GAIN Parameters

The GAIN parameter defines the amplification in the analog gain chain of the Hall plate, which is then converted to a digital signal. To minimize the quantization errors occurring at the A/D converter, the highest possible analog gain shall be selected, and the digital gain (see parameter DIG_GAIN) capability shall be used to trim the circuit sensitivity in a fine manner.

13.3. Sensor DSP Configuration

Figure 18 gives the simplified Digital Signal Processing Chain from Position after ADC to output. This section explains the compensation capability of the IC. Table 26 explains every parameter in more detail.

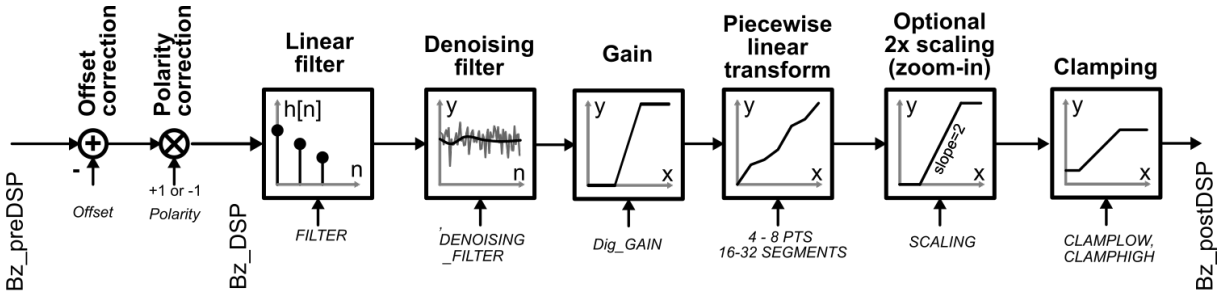


Figure 18 – Digital Signal Process Chain from ADC to the Output of MLX91377

Parameter	Range (FS)	Comment
Bz_preDSP	+/- 15 bit +/- ~100 mT	Normalised Bz value 2's complimentary 16 bit
Bz_DSP	16 bit 200 mT	Input signal for LNR Full scale, to be re-scaled by DIG_GAIN
Bz_postDSP	16 bit 0..100 %	12 MSB used for DAC, SENT, SPC

Table 26 – Parameters for DSP configuration

13.3.1. OFFSET (or Quiescent Point)

The OFFSET defines the quiescent position and can be placed at any location on the transfer function (LNR). A default OFFSET is chosen to center the quiescent point, corresponding with a full output span equal to ± ~100 mT.

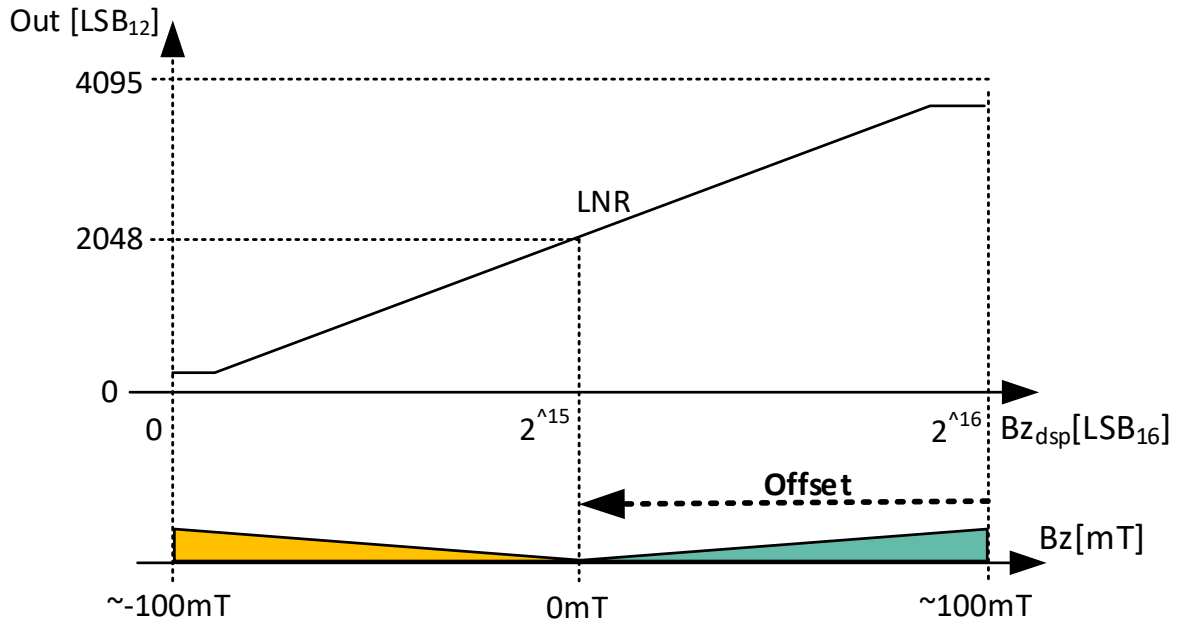


Figure 19 – Default OFFSET positioning

13.3.2. POLARITY Parameter

The POLARITY parameter defines the sensor output polarity vs. magnetic field polarity.

This parameter is not mandatory to be used, as the sign can also be modified through the slope of the transfer function (LNR).

13.3.3. LNR Parameters

There are 4 different possibilities to define the transfer function (LNR) as specified in the Table 27:

- With 4 arbitrary points (defined by X and Y coordinates) and 5 slopes
- With 8 arbitrary points (defined by X and Y coordinates)
- With 16 equidistant segments for which only the Y coordinates are defined
- With 32 equidistant segments for which only offset of Y compared to the average value is defined

Output Transfer Characteristic	DSP_SEL_4PTS	DSP_LNR_RESX2
4 Arbitrary Points	1	0
8 Arbitrary Points	1	1
16 Equidistant Segments	0	0
32 Equidistant Segments	0	1

Table 27 - Output Transfer Characteristic Selection Table

Parameter	LNR type	Value	Unit
LNR_A_X LNR_B_X LNR_C_X LNR_D_X	4-pts, X coordinates	0 … FFFFh	LSB_{16}
LNR_A_Y LNR_B_Y LNR_C_Y LNR_D_Y	4-pts, Y coordinates	0 … 100 -50 … + 150 0 … 4095 -2048…6144	% LSB_{12}
LNR_S0 LNR_A_S LNR_B_S LNR_C_S LNR_D_S	4-pts, slopes	-4.7 … 0 … 4.7	%/mT
LNR_X00..X07	8-pts, X coordinates	0 … FFFFh	LSB_{16}
LNR_Y00..Y16	8-,17-pts, Y coordinates	0…100 -50 … + 150 0…4095 -2048…6144	% LSB_{12}
LNN_DELTA_Y00..Y32	33-pts offsets	± 3.125% ± 6.25% ± 12.5% ± 25%	%
DIG_GAIN	17/33-pts	1/256…1	ratio
CLAMPLOW	All	0…100 0…4095	% LSB_{12}
CLAMPHIGH	All	0…100 0…4095	% LSB_{12}

Table 28 - Output linearization and clamping parameters

13.3.4. Enable Scaling Parameter

This parameter enables to double the scale of Y coordinates linearization parameters from [0…100] % to [-50…150]% according to the following table (Table 29). This is valid for all linearization schemes except the 32 points.

USEROPTION_SCALING	LNR_Y min value	LNR_Y max value
0	0%	100%
1	-50%	150%

Table 29 - USEROPTION_SCALING parameter

13.3.5. 4-pts LNR Parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital field and the output signal.

The four-point transfer function of the MLX91377 from the digital field value to the digital output is described in Figure 20 below. Seven segments can be programmed but the clamping levels are necessarily flat.

Two, three, or even six calibration points are then available, reducing the overall non-linearity of the IC by almost an order of magnitude each time. Three or six calibration points will be preferred by customers looking for excellent non-linearity figures. Two-point calibrations will be preferred by customers looking for a lower cost calibration set-up and shorter calibration time.

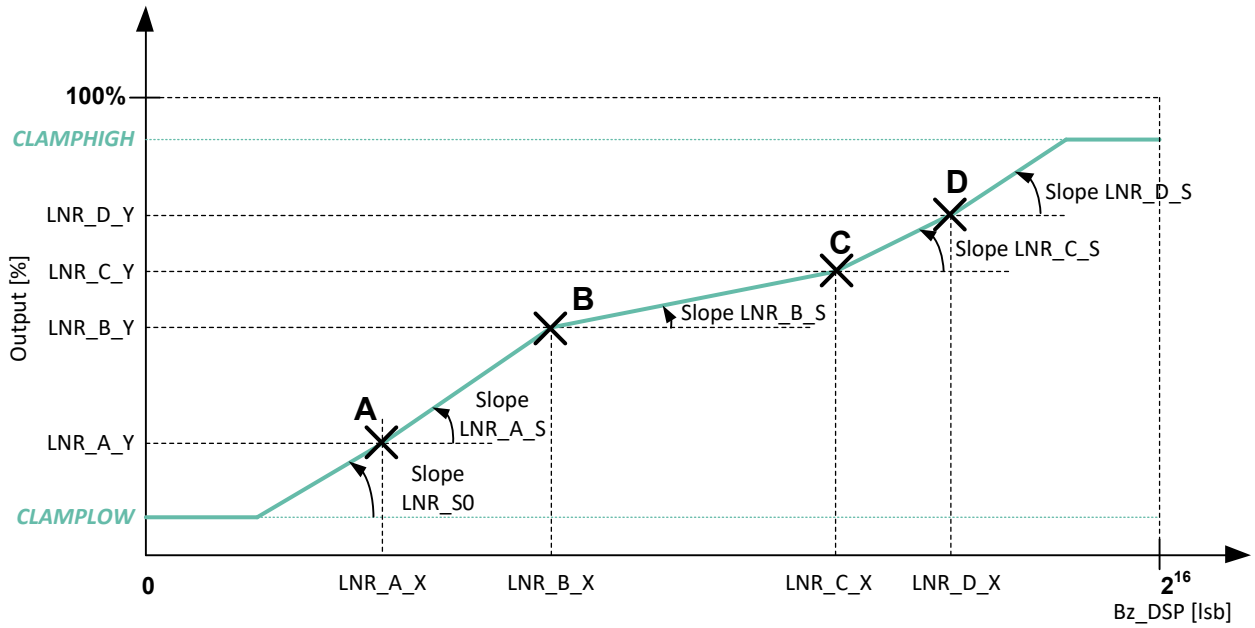


Figure 20 – 4-pts Linearization Parameters Description

13.3.6. 8-pts LNR Parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital field and the output signal.

The eight-point transfer function of the MLX91377 from the digital field value to the output voltage is described in Figure 21 below. Eight calibration points [LNR_X0...7, LNR_Y0...7] together with 2 fixed

points at the extremity of the range ([0°, 0%] ; [360°, 100%]) divides the transfer curve into 9 segments. Each segment is defined by 2 points and the values in between is calculated by linear interpolation.

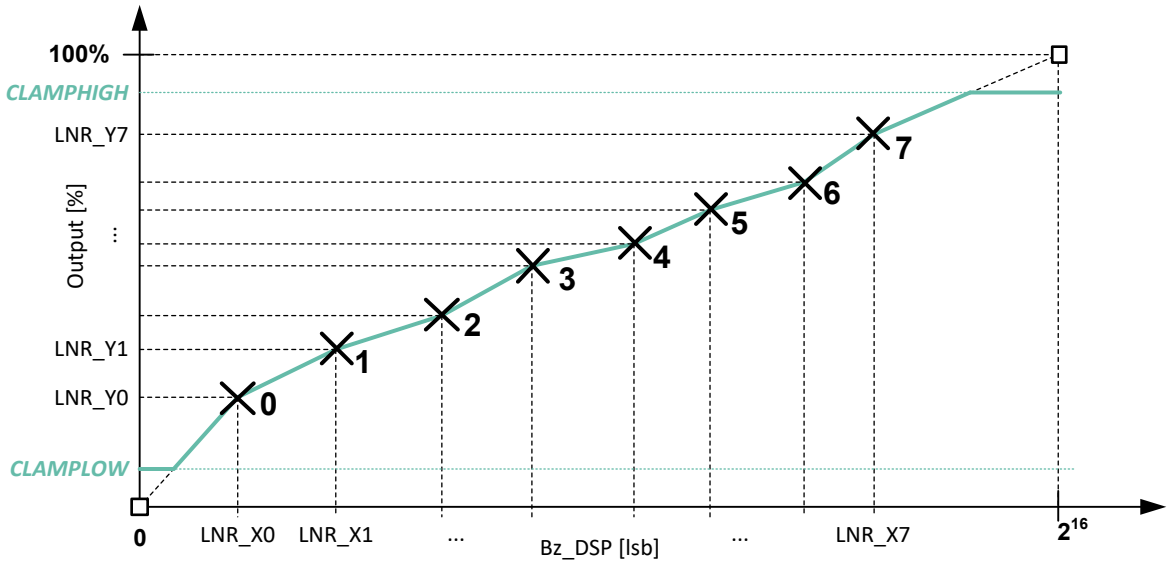


Figure 21 – 8-pts Linearization Parameters Description

13.3.7. 17-pts LNR Parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital field and the output signal.

The shape of the MLX91377 seventeen points transfer function from the digital field value to the output voltage is described in Figure 22 below. In the 17-pts mode, the output transfer characteristic is Piece-Wise-Linear (PWL).

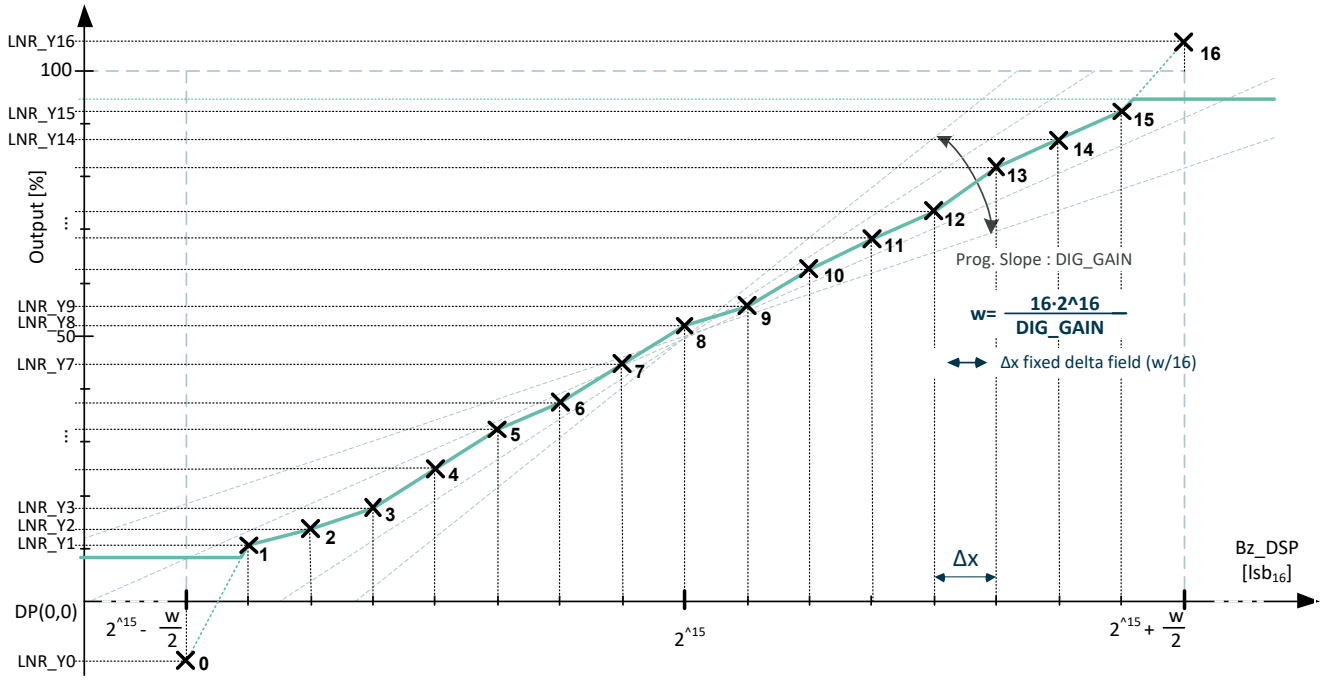


Figure 22 – 17-pts Linearization Parameters Description

All the Y-coordinates can be programmed from -50% up to +150% to allow clamping in the middle of one segment (like on the figure), but the output value is limited to CLAMPLOW and CLAMPHIGH values.

Between two consecutive points, the output characteristic is interpolated.

13.3.8. 33-pts LNR parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital field and the output signal.

The 33-point transfer function of the MLX91377 from the digital field value to the output voltage is described in Figure 23 below. In the 33-pts mode, the output transfer characteristic is Piece-Wise-Linear (PWL).

The Y-coordinates can be offset from the ideal characteristic within an adjustable range defined by LNR_DELTA_Y_EXPAND_LOG2. The available values are summarized in Table 30. All LNR_delta_Y## parameters are encoded in a fractional signed 8-bit value.

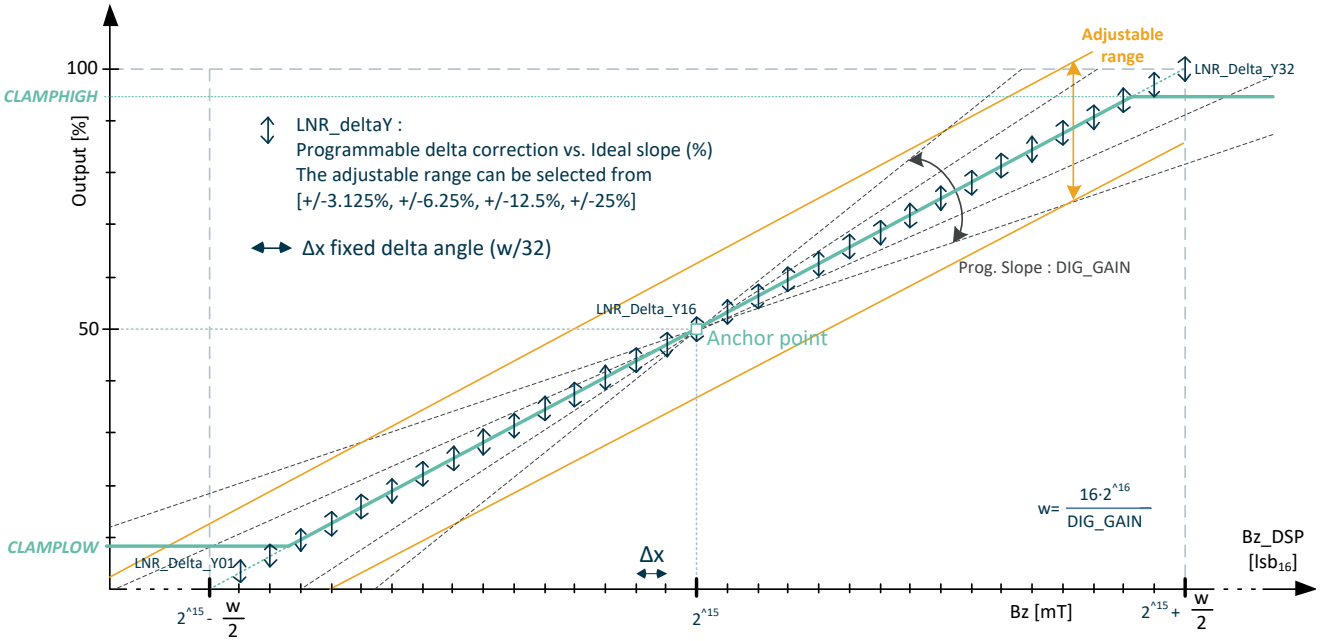


Figure 23 – 33-pts Linearization Parameters Description

LNR_DELTA_Y_EXPAND_LOG2	Adjustable Range	Correction resolution
0	±3.125%	0.024%
1	±6.25%	0.049%
2	±12.5%	0.098%
3	±25%	0.20%

Table 30 - LRN_DELTA_Y_EXPAND_LOG2 values and correction resolution

13.3.9. Thermal Sensitivity Drift Correction

The parameters, MAGNET_SREL_TC and MAGNET_SREL_DT [1..7] can trim the system's sensitivity drift. The drop of the magnetic sensitivity shall be described by a linear magnet TC slope (MAGNET_SREL_TC), and optionally 7 deviation points (MAGNET_SREL_DT [1..7]), placed at equally distributed temperatures, forming a piece-wise-linear transfer curve.

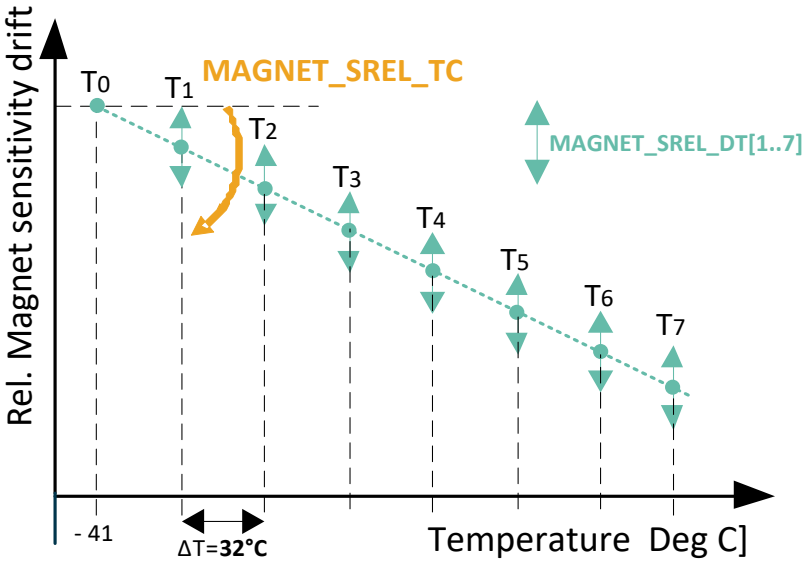


Figure 24 - Temperature compensated magnet sensitivity

By convention, the magnet relative sensitivity @-41°C (Tlin= 0x100) = 1.0.

Parameter	Min	Typ	Max	Unit	Condition
MAGNET_SREL_TC	0	-	-3906.25	ppm/°C	
MAGNET_SREL_DT1	-0.125	0	0.125		Tlin= 0x200
MAGNET_SREL_DT2	-0.125	0	0.125		Tlin= 0x300
MAGNET_SREL_DT3	-0.125	0	0.125		Tlin= 0x400
MAGNET_SREL_DT4	-0.125	0	0.125		Tlin= 0x500
MAGNET_SREL_DT5	-0.125	0	0.125		Tlin= 0x600
MAGNET_SREL_DT6	-0.125	0	0.125		Tlin= 0x700
MAGNET_SREL_DT7	-0.125	0	0.125		Tlin= 0x800

Table 31 - Temperature compensated magnet sensitivity parameters

13.3.10. Thermal OUTSLOPE Offset Correction

Two parameters, OUTSLOPEHOT and OUTSLOPECOLD, are used to add a temperature dependent offset. This feature is enabled by the parameter OUTSLOPE_SEL that apply this modification either directly to the field or after the linearization function. The MLX91377 uses its internal linearized temperature to compute the offset shift as depicted in the figure below (Figure 25).

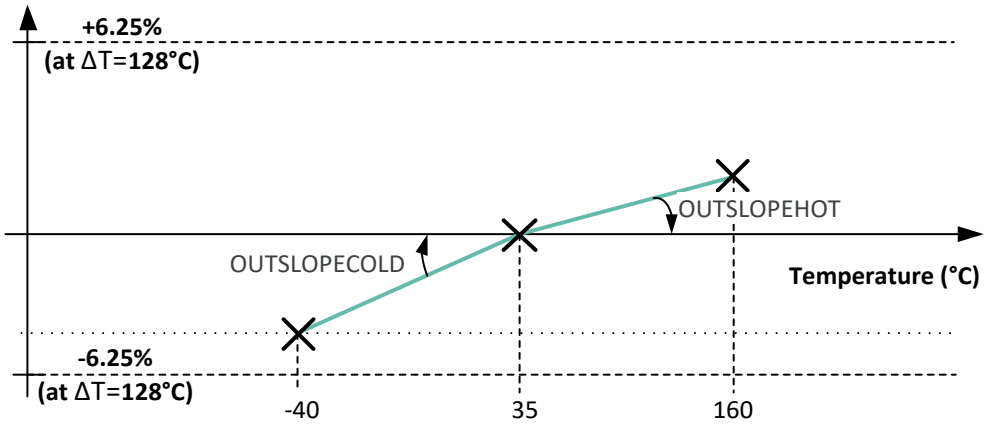


Figure 25 - Temperature compensated offset

The thermal offset can be added or subtracted before the clamping, either to the field or output. The span of this offset is ±6.25% of the full output scale for a temperature difference of 128°C. The added thermal offset varies with temperature following the equations below. The two thermal coefficients are encoded in signed two's complement 8bit format (-128…127) and defined separately below 35°C (OUTSLOPECOLD) and above 35°C (OUTSLOPEHOT).

OUTSLOPE_SEL	Description
0	No thermal offset correction
1	Thermal offset enabled, applied after field calculation, i.e. after discontinuity point (B_{zr2p}, 0x8000 by default)
2	Enabled, applied after output calculation and before clamping (B_{zout})

Table 32 - Temperature compensated offset selection parameter

If IC internal temperature is higher than 35°C then:

$$B_{zTcomp} = B_{zin} - \Delta T \cdot \text{OUTSLOPEHOT}$$

If IC internal temperature is lower than 35°C then:

$$B_{zTcomp} = B_{zin} - \Delta T \cdot \text{OUTSLOPECOLD}$$

where B_{zin} is either B_{zr2p} or B_{zout} depending on OUSLOPE_SEL value.

13.3.11. CLAMPING Parameters

The clamping levels are two independent values to limit the output voltage range. The CLAMPLOW parameter adjusts the minimum output level. The CLAMPHIGH parameter sets the maximum output. Both parameters have 16 bits of adjustment and are available for all four LNR modes. As output data resolution is limited to 12 bits, the 4 LSB of this parameter will have no significant effect on the output. The value is encoded in fractional code, from 0% to 100%

13.4. Filtering

The MLX91377 includes 2 types of filters:

- Exponential moving average (EMA) Filter: programmable by the HYST parameter
- Low Pass FIR Filters controlled with the DSP_FILTER parameter

Parameter	Value
HYST	0 … 255
DSP_FILTER	0 … 2

Table 33 - Filtering configuration

13.4.1. Exponential Moving Average (IIR) Filter

The HYST parameter is a hysteresis threshold to activate / de-activate the exponential moving average filter. The output value of the IC is updated with the applied filter when the digital step is smaller than the programmed HYST parameter value. The output value is updated without applying the filter when the increment is bigger than the hysteresis. The filter reduces therefore the noise but still allows a fast step response for bigger field changes. The hysteresis must be programmed to a value close to the internal magnetic field noise level (1 LSB ~ 0.024 mT).

$$y_n = a * x_n + (1-a) * y_{n-i} \qquad \begin{matrix} x_n = Bz \\ y_n = Output \end{matrix}$$

The filters characteristic is given in the following table (Table 34):

DENOISING_FILTER_ALPHA_SEL	0	1	2	3
Coefficients a	0.75	0.5	0.25	0.125
Efficiency RMS (dB)		2.4	4.2	

Table 34 - IIR Filter characteristics

13.4.2. FIR Filters

The MLX91377 features 2 FIR filter modes controlled with Filter = 1…2. Filter = 0 corresponds to no filtering. The transfer function is described by:

$$y_n = \frac{1}{\sum_{i=0}^{j} a_i} \sum_{i=0}^{j} a_i x_{n-i}$$

This filter characteristic is given in the Table 35.

FILTER value	0	1	2
Type	Disable	Finite Impulse Response (FIR)	
Coefficients a_i	1	11	1111
Title	No filter	ExtraLight	Light
DSP cycles (#taps)	1	2	4
Efficiency RMS (dB)	0	3.0	6.0

Table 35 - FIR Filter Characteristics

13.5. Programmable Diagnostics Settings

13.5.1. Diagnostics Global Enable

DIAG_EN should be kept to its default value (1) to retain all functional safety abilities of the MLX91377. This feature should not be disabled.

13.5.2. Diagnostic Debouncer

A debouncing algorithm is available for analog diagnostic reporting (see chapter 14.2). Enabling this debouncer will increase the diagnostic reporting time of the device. Therefore, Melexis recommends keeping the debouncing of analog faults off by not modifying below described values (see Table 20 for factory defaults).

NVRAM Parameter	Description
DIAGDEBOUNCE_STEPDOWN	Decrement values for debouncer counter
DIAGDEBOUNCE_STEPUP	Increment value for debouncer counter
DIAG_DEBOUNCE_THRESH	Threshold for debouncer counter to enter diagnostic mode

Table 36 - Diagnostic debouncing parameters

Once an analog monitor detects an error, it takes control of the debouncing counter. This counter will be incremented by STEPUP value each time this specific monitor is evaluated and the error is still present. When the debouncing counter reaches the value defined by DEBOUNCE THRESHOLD, an error is reported on the error channel, and the debouncing counter stays clamped to this DEBOUNCE THRESHOLD value. Once the error disappears, each time its monitor is evaluated, the debouncing counter is decremented by STEPDOWN value. When the debouncing counter reaches zero, the error disappears from the reporting channel and the debouncing counter is released. To implement proper reporting times, the DTI defined in the Table 8 should be referred. The reporting and recovery time are defined in the table below (valid for THRESH≠0).

Parameter	Min	Max
Reporting Time	$DTI \cdot \left(\left\lceil \frac{THRESH}{STEPUP} \right\rceil - 1\right)$	$DTI \cdot \left(\left\lceil \frac{THRESH}{STEPUP} \right\rceil\right)$
Recovery Time	$DTI \cdot \left(\left\lceil \frac{THRESH}{STEPDOWN} \right\rceil\right)$	$DTI \cdot \left(\left\lceil \frac{THRESH}{STEPDOWN} \right\rceil + 1\right)$
	$\left\lceil \frac{x}{y} \right\rceil$	is the ceiling function of x divided by y

Table 37 - Diagnostic Reporting and Recovery times

13.5.3. Over/Under Temperature Diagnostic

DIAG_TEMP_THR_HIGH defines the threshold for over temperature detection and is compared to the linearized value of the temperature sensor T_{LIN}. DIAG_TEMP_THR_LOW defines the threshold for under temperature detection and is compared to the linearized value of the temperature sensor T_{LIN}

T_{LIN} is encoded using the SENT standard for temperature sensor. Its linearity error can be referred to Table 12. One can get the physical temperature of the die using following formula:

$$T_{PHY}[°C] = \frac{T_{LIN}}{8} - 73.15$$

DIAG_TEMP_THR_LOW/HIGH are encoded on 8-bit unsigned values with the following relationship towards T_{Lin}

$$DIAG\_TEMP\_THR\_(LOW/HIGH) = \frac{T_{LIN}}{16}$$

Following table summarizes the characteristics of the linearized temperature sensor and the encoding of the temperature monitor thresholds.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
T_{LIN} resolution	Res_{TLIN}	-	0.125	-	°C/LSB	
T_{LIN} refresh rate	$F_{S,TLIN}$	-	200	-	Hz	
High temperature threshold	DIAG_TEMP_THR_LOW	-	8	-	LSB	Recommended value, corresponds to -57°C
Low temperature threshold	DIAG_TEMP_THR_HIGH	-	128	-	LSB	Recommended value, corresponds to 183°C
High/low temperature threshold resolution	Res_{Tthr}		2		°C/LSB	

Table 38 - Linearized Temperature Sensor characteristics

13.5.4. Field Strength and Field Monitoring Diagnostics

Field Strength is compensated over the circuit operating temperature range and represents a reliable image of the field intensity generated by the magnet.

Field Strength value is optionally available in SENT secondary fast channel.

14. Functional Safety

14.1. Safety Manual

The safety manual, available upon request, contains the necessary information to integrate the MLX91377 component in a safety related item, as Safety Element Out-of-Context (SEooC).

In particular, it includes:

- The description of the Product Development lifecycle tailored for the Safety Element.
- An extract of the Technical Safety concept.
- The description of Assumptions-of-Use (AoU) of the element with respect to its intended use, including:
  - assumption on the device safe state;
  - assumptions on fault tolerant time interval and multiple-point faults detection interval;
  - assumptions on the context, including its external interfaces;
- The description of safety analysis results at the device level useful for the system integrator; HW architectural metrics and description of dependent failures initiators.
- The description and the result of the functional safety assessment process; list of confirmation measures and description of the independency level.

14.2. Safety Mechanisms

The MLX91377 provides numerous self-diagnostic features (safety mechanisms). Those features increase the robustness of the IC functionality by either preventing the IC to provide an erroneous output signal or reporting the failure according to the SENT protocol definition.

Legend
● High coverage
O Medium coverage
ANA : Analog hardware failure reporting, described in the safety manual
High-Z : Special reporting, output is set in high impedance mode (no HW fail-safe mode/timeout, no SW safe startup)
DIG : Digital hardware failure reporting, described in the safety manual
DTI: Diagnostic Test Interval (see section 7.1 for values)
At Startup : HW fault present at time zero is detected before a first frame is transmitted.
DIAG_EN : This safety mechanism can be disabled by setting DIAG_EN = 0 (see 11 End-User Programmable Items). This option should not be used in application mode!

Table 39 - Self Diagnostic Legend

Category and safety mechanism name	Front-end	ADC	DSP	Back-end	Support. Func.	Module & Package	Reporting mode	At startup	DIAG EN
Signal-conditioning (AFE, External Sensor) Diagnostic									
Magnetic Signal Conditioning Voltage Test Pattern	●	○	○				ANA	NO	●
Magnetic Signal Conditioning Rough Offset Clipping check	●		○				ANA	NO	●
Mag. Sig. Cond. Failure control by the chopping technique	●						n/a	YES	
External Sensor Sig. Cond. Voltage Valid Range Check	●					●	ANA	YES	●
External Sensor Sig. Cond. Frequency Valid Range Check	●					●	ANA	YES	●
A/D Converter Test Pattern		●					ANA	NO	●
ADC Conversion errors & Overflow Errors		●					ANA	YES	●
HE Switching Circuitry Symmetry Check	●						ANA	YES	●
HE Bias Current Supply Monitor	●						ANA	YES	●
Stress Sensor Valid Range Check	●						ANA	YES	●
Digital-circuit Diagnostic									
RAM Parity, 1 bit per 16 bits word, ISO D.2.5.2			●				DIG	YES	●
ROM Parity, 1 bit per 32 bits word, ISO D.2.5.2			●				DIG	YES	●
NVRAM 16 bits signature (run-time) ISO D.2.4.3, by means of SW CRC-CCITT16			●				DIG	NO	●
NVRAM Double Error Detection ECC ISO			●				DIG	YES	
Logical Monitoring of program sequence ISO D.2.9.3 via Watchdog "IWD" (cpu clock) ISO D2.9.2			●		○		DIG	NO	●

Category and safety mechanism name	Front-end	ADC	DSP	Back-end	Support. Func.	Module & Package	Reporting mode	At startup	DIAG EN
Watchdog "AWD" (separate clock) ISO D2.9.1			●		○		DIG	YES	
CPU Errors "Invalid Address", "Wrong opcode"			●		○		DIG	YES	
ADC Interface Checksum		●	○				DIG	NO	●
DSP Test Pattern (atan2)			●		○		DIG	NO	●
Critical ports monitoring			●				DIG	NO	●
DSP Overflow	○	○	●				DIG	YES	●
Magnetic field unchopping block diagnostic (SW)			●				DIG	NO	
ADC data adder test		○	●				DIG	YES	●
SENT Fall Collision detection (SENT pulse generator)			●				DIG	NO	●
DAC Overflow			●				DIG	NO	●
Communication Interface Diagnostic									
SENT parity check over Configuration registers				●			DIG	NO	●
SENT block: Protection against re-configuration at run-time				●			DIG	NO	●
SENT Frame Counter & Redundant Nibble				●			n/a	n/a	
System-level diagnostic									
Supply Voltage Monitors (all supply domains except VS_OV & Power-on reset)					●	●	ANA	YES	●
External Supply Overvoltage Monitor VS_OV					●	●	High-Z	YES	
Digital Supply under-voltage monitor (Power-on reset)					●	●	High-Z	YES	

Category and safety mechanism name	Front-end	ADC	DSP	Back-end	Support. Func.	Module & Package	Reporting mode	At startup	DIAG EN
Supply Bias Current Monitor					●		ANA	NO	●
Overheating monitor	○	○	○	○	○	●	ANA	YES	●
Warning/Reporting Mechanisms									
HW Error Controller			●	●	●		DIG	YES	
HW Fail-safe mode with timeout			●	●	●		DIG	YES	
Analog-type Error management	●	●			●		ANA	NO	
Safe start-up mode			●		●		DIG	n/a	
Mechanisms executed at start-up only									
RAM March-C HW Test at start-up			●		●		DIG	YES	

Table 40 - MLX91377 List of Self Diagnostics with Characteristics

14.3. Fault Handling Time Interval

The goal of this chapter is to specify the Fault Handling Time Interval (FHTI). The following definitions need to be considered:

Name	Definition
DTI_{ANA}	Time to run one full analog diagnostic cycle (programmable value)
DTI_{DIG}	Time to run one full nvram BIST cycle (programmable value)
τ_R	Output refresh period in analog output mode (see "Timings definition" chapter)
T_{pwm_input}	the period of the incoming PWM signal on gateway pin
$T_{trigger}$	the time between 2 SPC trigger pulses
DTI	Diagnostic Time Interval: worst-case time between 2 consecutive runs of a specific diagnostic
EXE	Execution Time: worst-case time between the measurement start of a given diagnostic and the availability of the result of this measurement
REP	Reporting Time: worst-case time needed between an internal diagnostic error event and a switch of the output to fail-safe state
FHTI	Fault Handling Time Interval: the time interval between the start of the first frame with invalid position value wihtout notice, and the end of the last frame preceding a fail-safe state of the IC. It is calculated as the sum of DTI, EXE, and REP figures. The following equation is valid for any diagnostic: $FHTI = DTI + EXE + REP$

Table 41 – Glossary of Terms for the Definition Regarding Fault Handling Time Interval

The following table details the cycle time, execution time and reporting time for all monitors included in MLX91377. These figures are provided for the analog and SPC output mode. In all cases, the worst case timing values are provided in the table below:

Category and safety mechanism name	DTI	EXE	REP
Signal-conditioning (AFE, External Sensor) Diagnostic			
Magnetic Signal Conditioning Voltage Test Pattern	1 * DTI_{ANA}	1 * τ_R	1 * τ_R
Magnetic Signal Cond. Rough Offset Clipping check	2.5 ms	1 * τ_R	1 * τ_R
External Sensor Sig. Cond. Voltage Valid Range Check	9 * τ_R	0	1 * τ_R
External Sensor Sig. Cond. Frequency Valid Range Check	1*T_{pwm_input}	1 * τ_R	1 * τ_R
A/D Converter Test Pattern	1 * DTI_{ANA}	0	1 * τ_R
ADC Conversion errors & Overflow Errors	1 * τ_R	0	1 * τ_R
Hall-element & Mechanical-stress Tests	1 * DTI_{ANA}	0	1 * τ_R
Digital-circuit Diagnostic			
RAM Parity, 1 bit per 16 bits word, ISO D.2.5.2	< 1 * DTI_{ANA}	0	0
ROM Parity, 1 bit per 16 bits word, ISO D.2.5.2	< 1 * DTI_{ANA}	0	0
NVRAM Double Error Detection ECC ISO D.2.4.1	< 10µs	0	0
NVRAM 16 bits signature (run-time) ISO D.2.4.3	1 * DTI_{DIG}	0	0

Category and safety mechanism name	DTI	EXE	REP
Logical Monitoring of program sequence ISO D.2.9.3 via Watchdog "IWD" (CPU clock) ISO D2.9.2	4 ms	0	0
Watch-dog "AWD" (separate clock) ISO D2.9.1	5ms	0	0
CPU error detection	1 * τ_R	0	0
ADC Interface Checksum	1 * DTI_{ANA}	0	0
DSP Test Pattern (atan2)	1 * DTI_{ANA}	0	0
Critical ports monitoring	1 * DTI_{ANA}	0	0
DSP overflow	1 * τ_R	0	0
ADC data adder test	1 * τ_R	0	0
SENT Fall Collision detection & DAC Overflow	1 * τ_R	0	0
SENT H/W Interface Diagnostic			
SENT parity check over Configuration registers	1 * $T_{trigger}$	0	0
SENT HW: Protection against re-configuration at run-time	1 * $T_{trigger}$	0	0
System-level diagnostic			
Supply Voltage Monitors (all supply domains) except VS_OV & POR	1 * DTI_{ANA}	0	1 * τ_R
External Supply Overvoltage Monitor VS_OV	1 * DTI_{ANA}	0	1 * τ_R
Supply Bias Current Monitor	1 * DTI_{ANA}	0	1 * τ_R
Overheating monitor	9 * τ_R	1 * τ_R	1 * τ_R

Table 42 – Timings of the Cyclic Detection Mechanisms

Note :

1. **The orange colour coding** shows the worst case FHTI for analog and digital diagnostics
2. The ROM and RAM parity mechanism trigger a fail-safe state on the failing ROM or RAM word is accessed. (It is assumed that it will be accessed within one full diagnostic cycle in worst case)
3. EXE/REP time = 0 means that the execution or reporting time is negligible compared to the FHTI value

15. Recommended Application Diagrams

15.1. Wiring in TSSOP-16 dual-die Package for Analog Output

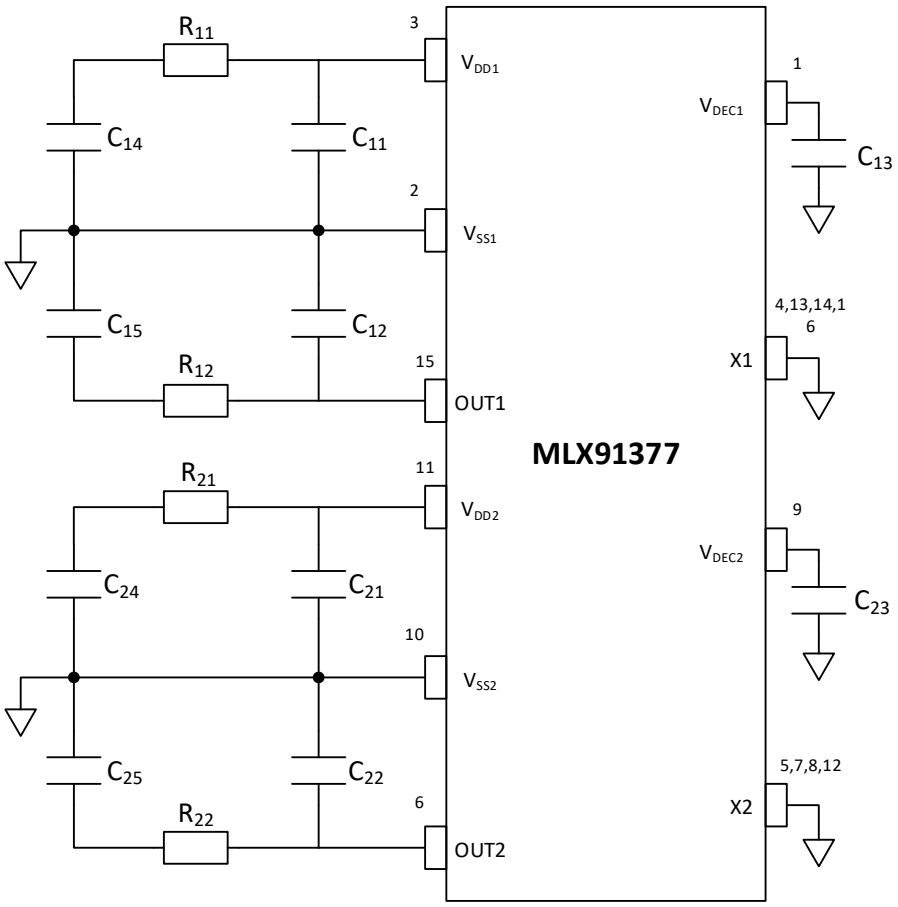


Figure 26 - Recommended wiring for the MLX91377 in TSSOP-16 dual-die package for analog output

Component	Min	Typ	Max	Remark
C_{11}, C_{21}	100nF	220nF	-	Close to the IC pin
C_{12}, C_{22}	10nF	-	100nF	
C_{13}, C_{23}	47nF	100nF	-	Close to the IC pin
C_{14}, C_{24}	-	0nF	1nF	Close to the connector
C_{15}, C_{25}	-	0nF	1nF	Close to the connector
R_{11}, R_{21}	-	0Ω	10Ω	
R_{12}, R_{22}	-	0Ω	10Ω	

Table 43 - Recommended Values for the MLX91377 in TSSOP-16 dual-die Package for analog output

C_{14}, C_{24}, C_{15}, C_{25}, R_{11}, R_{21}, R_{12} R_{22} are not needed under typical condition. They are only needed, when extremely high electromagnetic immunity (EMI) compliance is required, but the value of the resistors and capacitors should not exceed 10Ω and 1nF.

15.2. Wiring in TSSOP-16 dual-die Package for SPC Output

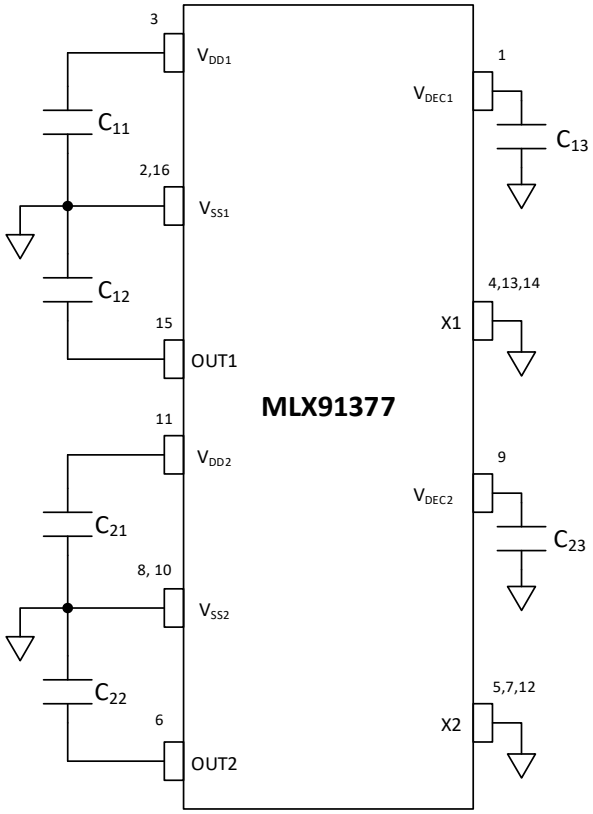


Figure 27 - Recommended wiring for the MLX91377 in TSSOP-16 dual-die package for SPC output

Component	min	Typ	Max	Remark
C_{11}, C_{21}	100nF	220nF	-	Close to the IC pin
C_{12}, C_{22}	-	2.2nF	4.7nF	Total capacitance on the bus
C_{13}, C_{23}	47nF	100nF	-	Close to the IC pin

Table 44 - Recommended Values for the MLX91377 in TSSOP-16 dual-die Package for SPC output

An external pi-filter to improve radiated emission performance in SPC protocol is not needed. The MLX91377 has a built-in high order low pass filter. Therefore, any additional external filter will deteriorate the SPC signal, and could make the output signal not comply to the SPC specifications, such as the fall times and the minimum output voltages. If extremely high electromagnetic immunity (EMI) compliance is needed, then a high-frequency low-pass RC-filter can be added at the output. The values should not exceed 10Ω and 1nF.

16. Standard Information Regarding Manufacturability of Melexis Products with Different Soldering Processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to standards in place in Semiconductor industry.

For further details about test method references and for compliance verification of selected soldering method for product integration, Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/en/quality-environment/soldering)

For all soldering technologies deviating from the one mentioned in above document (regarding peak temperature, temperature gradient, temperature profile etc), additional classification and qualification tests have to be agreed upon with Melexis.

For package technology embedding trim and form post-delivery capability, Melexis recommends consulting the dedicated trim & form recommendation application note : “Lead Trimming and Forming Recommendations” (http://www.melexis.com/en/documents/documentation/application-notes/lead-trimming-and-forming-recommendations).

Melexis is contributing to global environmental conservation by promoting lead free solutions. For more information on qualifications of RoHS compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/en/quality-environment.

17. ESD Precautions

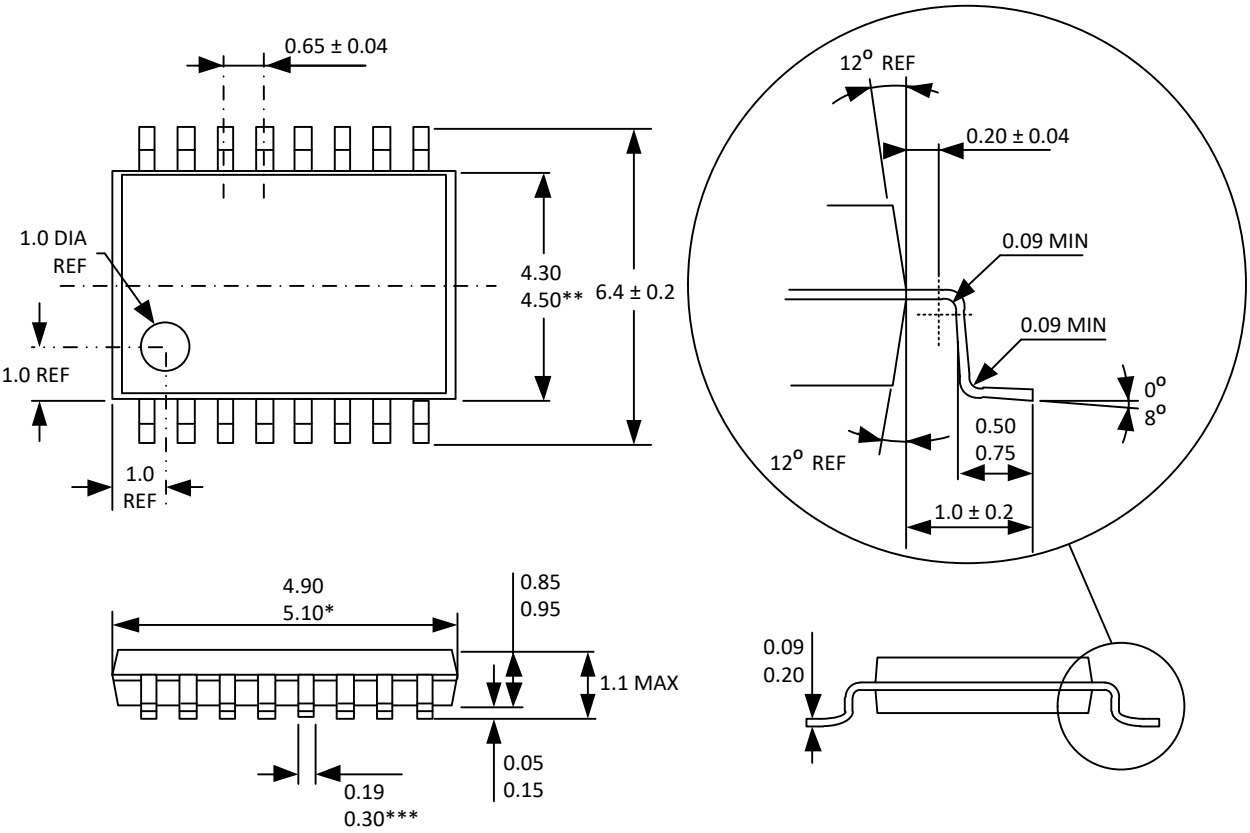
Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).

Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

18. Package Information

18.1. TSSOP-16 Package

18.1.1. TSSOP-16 - Package Dimensions



NOTES:

All dimensions are in millimeters (angles in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.
REF: Reference dimensions as stated in packaging supplier POD, based on JEDEC.

Figure 28 - TSSOP-16 Package Outline Dimensions

18.1.2. TSSOP-16 Dual-Die Package - Pinout and Marking

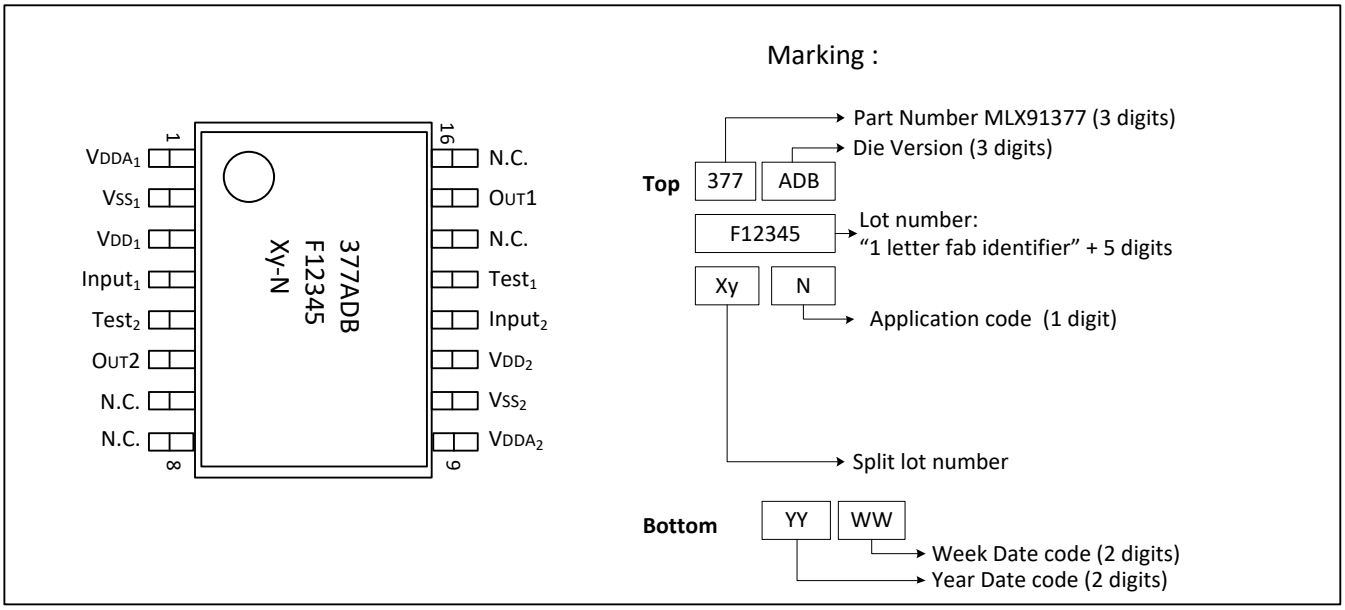


Figure 29 - TSSOP-16 Dual-Die Package Pinout and Marking

18.1.3. TSSOP-16 Dual-Die Package - Sensitive spot positioning

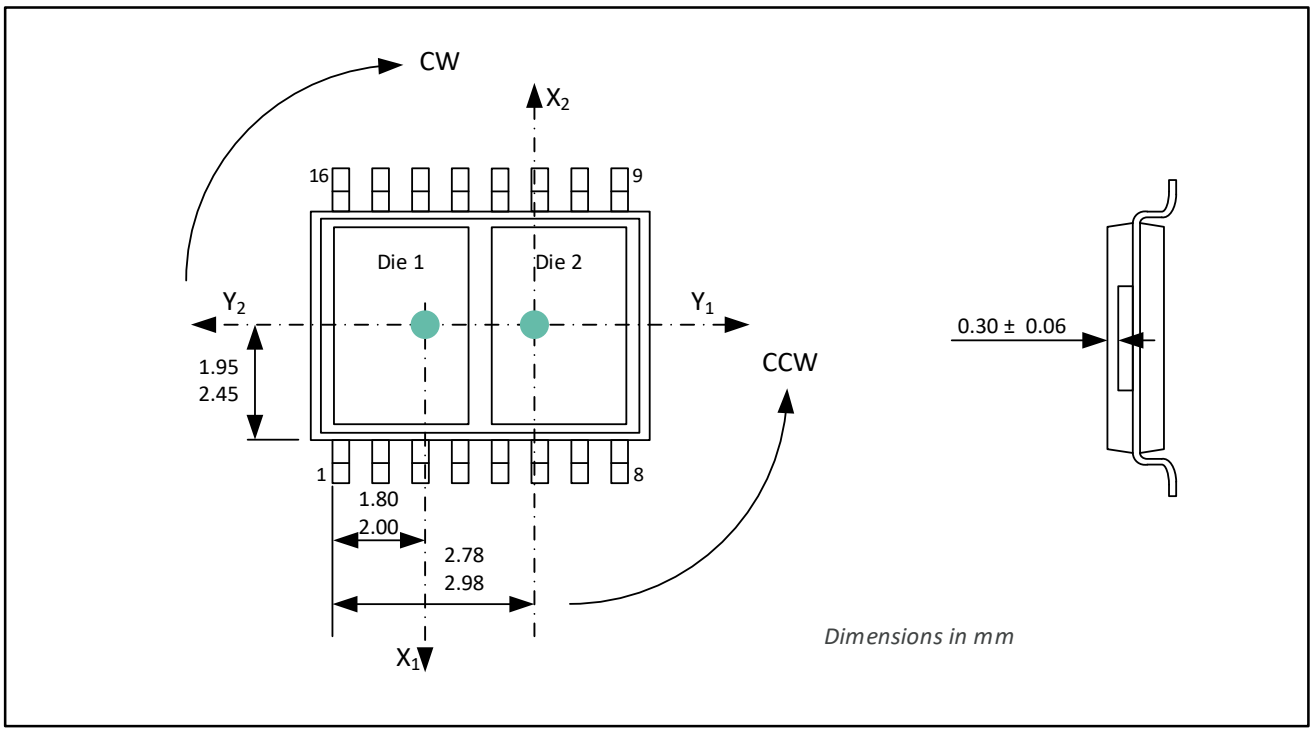


Figure 30 - TSSOP-16 Dual-Die Sensitive Spot Position

18.2. Packages Thermal Performances

The table below describe the thermal behaviour of available packages following JEDEC EIA/JESD 51.X standard.

Package	Junction to case - θjc	Junction to ambient - θja (JEDEC 1s2p board)	Junction to ambient - θja (JEDEC 1s0p board)
TSSOP-16	27.6 K/W	99.1 K/W	137 K/W

Table 45 - Standard Packages Thermal Performances

19. Contact

For the latest version of this document, go to our website at www.melexis.com.

For additional information, please contact our Direct Sales Team and get help for your specific needs:

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