

FEATURES

**High Accuracy Over Line and Load: $\pm 0.8\%$ @ 25°C,
 $\pm 1.4\%$ Over Temperature**
Ultralow Dropout Voltage: 120 mV Typical @ 100 mA
Requires only $C_O = 0.47 \mu\text{F}$ for Stability
**anyCAP = Stable with All Types of Output Capacitors
 (Including MLCC)**
Current and Thermal Limiting
Low Noise
Dropout Detector
Low Shutdown Current: 1 μA
3.0 V to 12 V Supply Range
-20°C to +85°C Ambient Temperature Range
Several Fixed Voltage Options
Ultrasmall SOT-23-6 (RT-6) Package
Excellent Line and Load Regulation

APPLICATIONS

Cellular Telephones
Notebook, Palmtop Computers
Battery Powered Systems
PCMCIA Regulator
Bar Code Scanners
Camcorders, Cameras

FUNCTIONAL BLOCK DIAGRAM

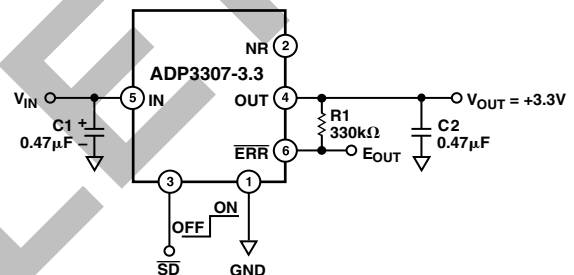
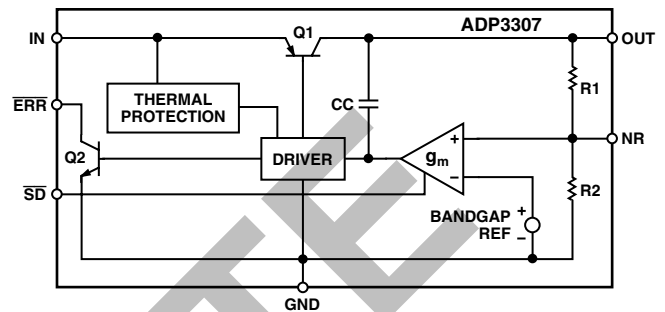


Figure 1. Typical Application Circuit

GENERAL DESCRIPTION

The ADP3307 is a member of the ADP330x family of precision low dropout anyCAP voltage regulators. The ADP3307 stands out from the conventional LDOs with a novel architecture and an enhanced process. Its patented design requires only a 0.47 μF output capacitor for stability. This device is stable with any type of capacitor regardless of its ESR (Equivalent Series Resistance) value, including ceramic types (MLCC) for space restricted applications. The ADP3307 achieves exceptional accuracy of $\pm 0.8\%$ at room temperature and $\pm 1.4\%$ overall accuracy over temperature, line and load variations. The dropout voltage of the ADP3307 is only 120 mV (typical) at 100 mA.

The ADP3307 operates with a wide input voltage range from 3.0 V to 12 V and delivers a load current in excess of 100 mA. It features an error flag that signals when the device is about to

lose regulation or when the short circuit or thermal overload protection is activated. Other features include shutdown and optional noise reduction capabilities. The ADP330x anyCAP LDO family offers a wide range of output voltages and output current levels from 50 mA to 300 mA:

- ADP3300 (50 mA, SOT-23-6)
- ADP3307 (100 mA, SOT-23-6)
- ADP3301 (100 mA, R-8)
- ADP3302 (100 mA, Dual Output)
- ADP3303 (200 mA)

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REV. A

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ADP3307—SPECIFICATIONS

(@ $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = 7\text{ V}$, $C_{IN} = 0.47\ \mu\text{F}$, $C_{OUT} = 0.47\ \mu\text{F}$, unless otherwise noted)¹ The following specifications apply to all voltage options.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---------------------------------|------------------------------------|---|------|-------|-------|-------------------|
| OUTPUT VOLTAGE ACCURACY | V_{OUT} | $V_{IN} = V_{OUTNOM} + 0.3\text{ V}$ to 12 V $I_L = 0.1\text{ mA}$ to 100 mA $T_A = 25^\circ\text{C}$ | -0.8 | | +0.8 | % |
| | | $V_{IN} = V_{OUTNOM} + 0.3\text{ V}$ to 12 V $I_L = 0.1\text{ mA}$ to 100 mA | -1.4 | | +1.4 | % |
| LINE REGULATION | $\frac{\Delta V_O}{\Delta V_{IN}}$ | $V_{IN} = V_{OUTNOM} + 0.3\text{ V}$ to 12 V $T_A = 25^\circ\text{C}$ | | 0.02 | | mV/V |
| LOAD REGULATION | $\frac{\Delta V_O}{\Delta I_L}$ | $I_L = 0.1\text{ mA}$ to 100 mA $T_A = 25^\circ\text{C}$ | | 0.06 | | mV/mA |
| GROUND CURRENT | I_{GND} | $I_L = 100\text{ mA}$ | | 0.76 | 2.0 | mA |
| | | $I_L = 0.1\text{ mA}$ | | 0.19 | 0.3 | mA |
| GROUND CURRENT IN DROPOUT | I_{GND} | $V_{IN} = 2.5\text{ V}$ $I_L = 0.1\text{ mA}$ | | 0.6 | 1.2 | mA |
| DROPOUT VOLTAGE | V_{DROP} | $V_{OUT} = 98\%$ of V_{OUTNOM} | | | | |
| | | $I_L = 100\text{ mA}$ | | 0.126 | 0.22 | V |
| | | $I_L = 10\text{ mA}$ | | 0.025 | 0.07 | V |
| | | $I_L = 1\text{ mA}$ | | 0.004 | 0.015 | V |
| SHUTDOWN THRESHOLD | V_{THSD} | ON | 2.0 | 0.75 | | V |
| | | OFF | | 0.75 | 0.3 | V |
| SHUTDOWN PIN INPUT CURRENT | I_{SDIN} | $0 < V_{SD} < 5\text{ V}$ | | | 1 | μA |
| | | $5\text{ V} < V_{SD} \leq 12\text{ V}$ @ $V_{IN} = 12\text{ V}$ | | | 22 | μA |
| GROUND CURRENT IN SHUTDOWN MODE | I_Q | $V_{SD} = 0\text{ V}$, $V_{IN} = 12\text{ V}$ $T_A = 25^\circ\text{C}$ | | 0.005 | 1 | μA |
| | | $V_{SD} = 0\text{ V}$, $V_{IN} = 12\text{ V}$ $T_A = 85^\circ\text{C}$ | | 0.01 | 3 | μA |
| OUTPUT CURRENT IN SHUTDOWN MODE | I_{OSD} | $T_A = 25^\circ\text{C}$ @ $V_{IN} = 12\text{ V}$ | | | 2 | μA |
| | | $T_A = 85^\circ\text{C}$ @ $V_{IN} = 12\text{ V}$ | | | 4 | μA |
| ERROR PIN OUTPUT LEAKAGE | I_{EL} | $V_{EO} = 5\text{ V}$ | | | 13 | μA |
| ERROR PIN OUTPUT "LOW" VOLTAGE | V_{EOL} | $I_{SINK} = 400\ \mu\text{A}$ | | 0.12 | 0.3 | V |
| PEAK LOAD CURRENT | I_{LDPK} | $V_{IN} = V_{OUTNOM} + 1\text{ V}$ | | 170 | | mA |
| OUTPUT NOISE @ 3.3 V OUTPUT | V_{NOISE} | $f = 10\text{ Hz}$ – 100 kHz | | | | |
| | | $C_{NR} = 0$ | | 100 | | $\mu\text{V rms}$ |
| | | $C_{NR} = 10\text{ nF}$, $C_L = 10\ \mu\text{F}$ | | 30 | | $\mu\text{V rms}$ |

NOTES

¹Ambient temperature of 85°C corresponds to a junction temperature of 125°C under typical full load test conditions.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

| | |
|---|--------------------|
| Input Supply Voltage | −0.3 V to +16 V |
| Shutdown Input Voltage | −0.3 V to +16 V |
| Error Flag Output Voltage | −0.3 V to +16 V |
| Noise Bypass Pin Voltage | −0.3 V to +5 V |
| Power Dissipation | Internally Limited |
| Operating Ambient Temperature Range | −55°C to +125°C |
| Operating Junction Temperature Range | −55°C to +125°C |
| θ_{JA} | 230°C/W |
| θ_{JC} | 92°C/W |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature Range (Soldering 10 sec) | 300°C |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

ORDERING GUIDE

| Model | Output Voltage | Package Option | Marking Code |
|-----------------|----------------|----------------|--------------|
| ADP3307ART-2.7 | 2.7 V | RT-6 | LTC |
| ADP3307ART-2.85 | 2.85 V | RT-6 | LXC |
| ADP3307ART-3 | 3.0 V | RT-6 | LUC |
| ADP3307ART-3.2 | 3.2 V | RT-6 | LVC |
| ADP3307ART-3.3 | 3.3 V | RT-6 | LWC |

Contact the factory for the availability of other output voltage options.

Other Members of anyCAP Family¹

| Model | Output Current | Package Options ² | Comments |
|---------|----------------|------------------------------|---------------|
| ADP3300 | 50 mA | SOT-23-6 | High Accuracy |
| ADP3301 | 100 mA | R-8 | High Accuracy |
| ADP3302 | 100 mA | R-8 | Dual Output |
| ADP3303 | 200 mA | R-8 | High Accuracy |

NOTES

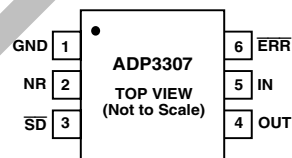
¹See individual data sheets for detailed ordering information.

²R = Small Outline, SOT-23 = Surface Mount, TSSOP = Thin Shrink Small Outline.

PIN FUNCTION DESCRIPTIONS

| Pin | Name | Function |
|-----|------------------|---|
| 1 | GND | Ground Pin |
| 2 | NR | Noise Reduction Pin. Used for further reduction of the output noise. (See text for details.) No connection if not used. |
| 3 | \overline{SD} | Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, this pin should be connected to the input pin. |
| 4 | OUT | Output of the Regulator, fixed 2.7 V, 3.0 V, 3.2 V or 3.3 V output voltage. Bypass to ground with a 0.47 μ F or larger capacitor. |
| 5 | IN | Regulator Input |
| 6 | \overline{ERR} | Open Collector Output that goes low to indicate that the output is about to go out of regulation. |

PIN CONFIGURATION

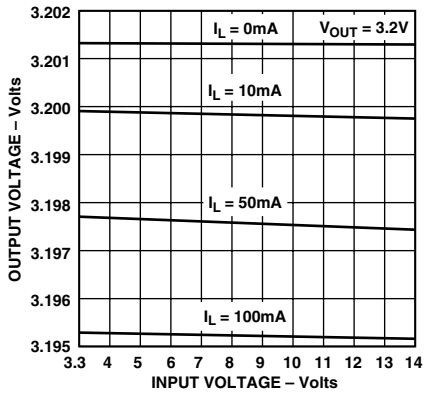


CAUTION

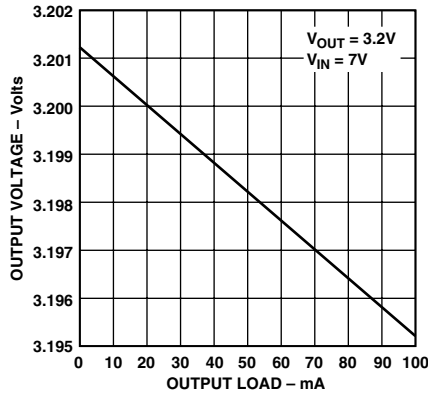
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3307 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



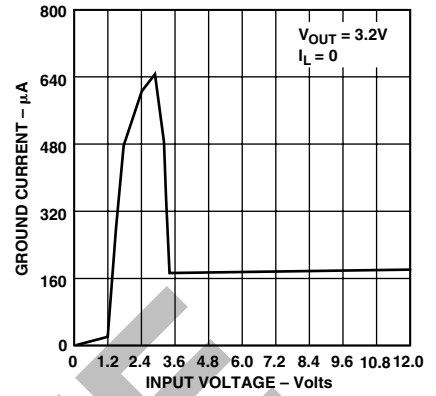
ADP3307—Typical Performance Characteristics



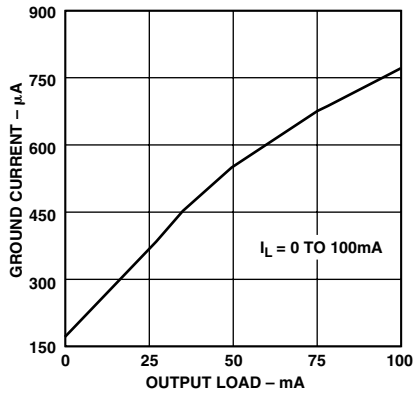
TPC 1. Line Regulation Output Voltage vs. Supply Voltage



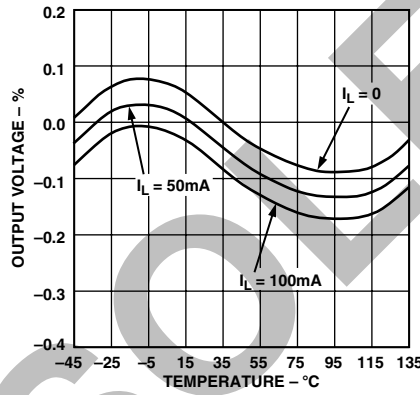
TPC 2. Output Voltage vs. Load Current Up to 100 mA



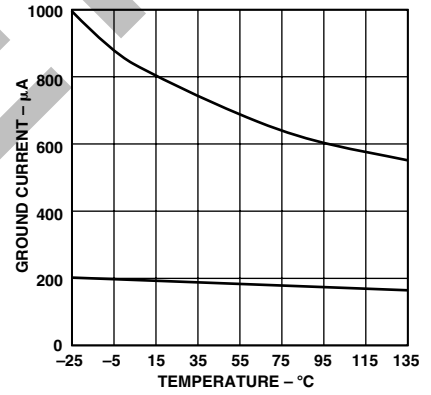
TPC 3. Quiescent Current vs. Supply Voltage—3.2 V (Both Outputs)



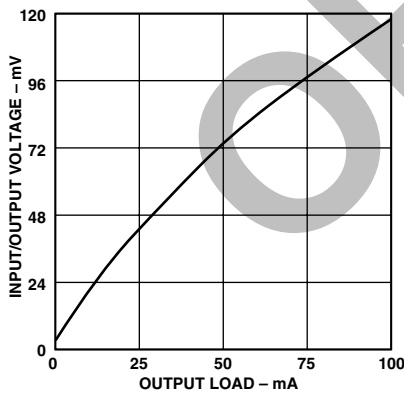
TPC 4. Ground Current vs. Load Current



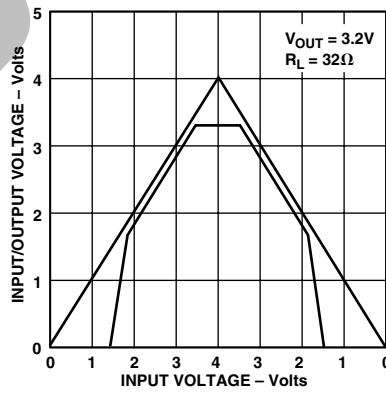
TPC 5. Output Voltage Variation % vs. Temperature



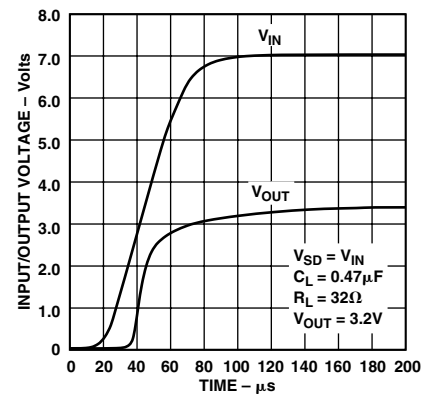
TPC 6. Quiescent Current vs. Temperature



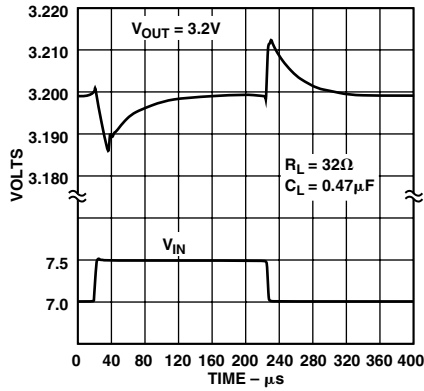
TPC 7. Dropout Voltage vs. Output Current



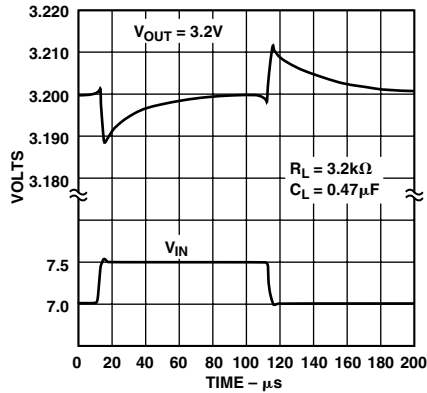
TPC 8. Power-Up/Power-Down



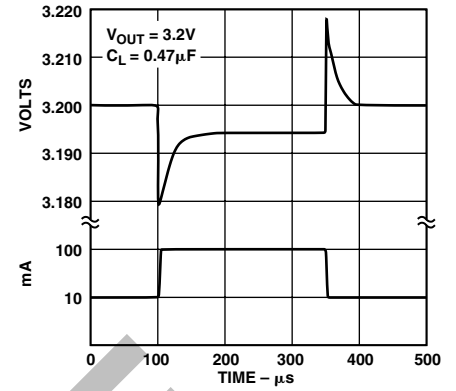
TPC 9. Power-Up Overshoot



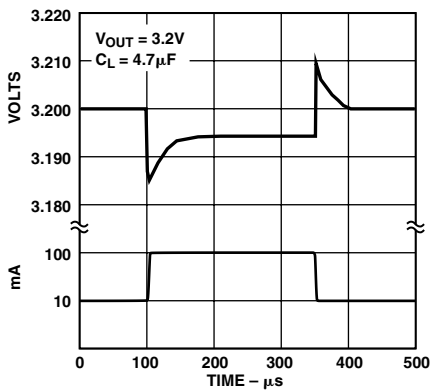
TPC 10. Line Transient Response



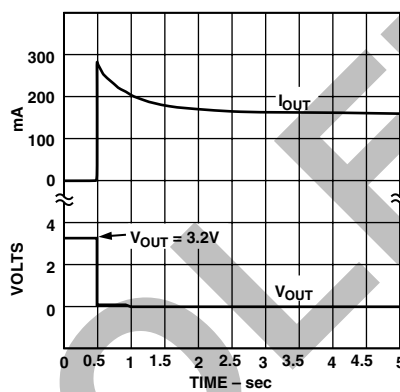
TPC 11. Line Transient Response



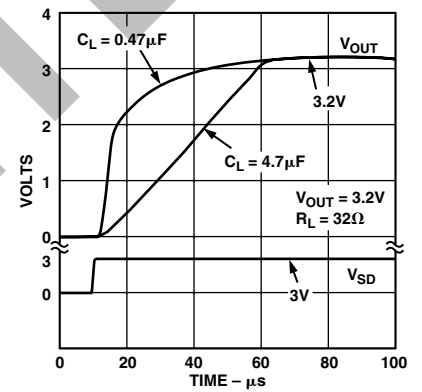
TPC 12. Load Transient



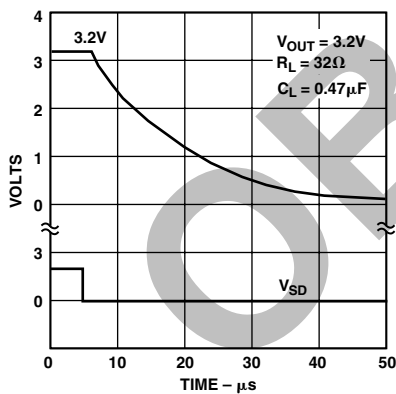
TPC 13. Load Transient



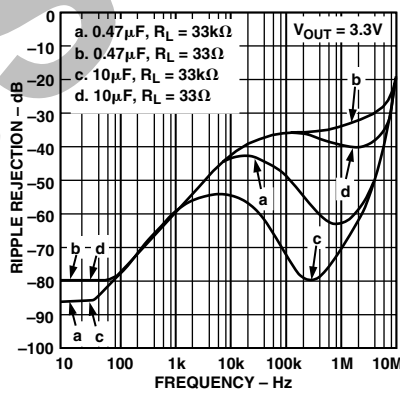
TPC 14. Short Circuit Current



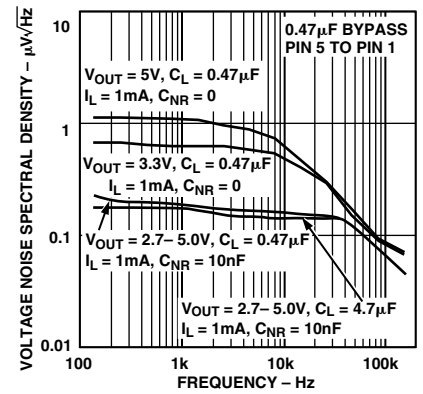
TPC 15. Turn On



TPC 16. Turn Off



TPC 17. Power Supply Ripple Rejection



TPC 18. Output Noise Density

ADP3307

THEORY OF OPERATION

The ADP3307 anyCAP LDO uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider consisting of R1 and R2 which is varied to provide the available output voltage option. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

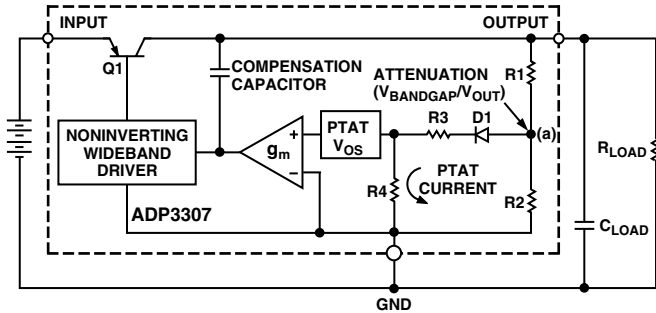


Figure 2. Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that at equilibrium it produces a large, temperature proportional input “offset voltage” that is repeatable and very well controlled. The gained up temperature proportional offset voltage is combined with the diode voltage to form a “virtual bandgap” voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the bandgap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by the diode D1, and a second divider consisting of R3 and R4, the values are chosen to produce a temperature stable output.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole splitting arrangement to achieve reduced sensitivity to the value, type and ESR of the load capacitance.

Most LDOs place strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value, required to keep conventional LDOs stable, changes depending on load and temperature. These ESR limitations make designing with conventional LDOs more difficult because of their unclear specifications and the dependence of ESR over temperature.

This is no longer true with the ADP3307 anyCAP LDO. It can be used with virtually any good quality capacitor, with no constraint on the minimum ESR. The innovative design allows the circuit to be stable with just a small 0.47 μF capacitor on the output. Additional advantages of the design scheme include superior line noise rejection and very high regulator gain that lead to excellent line and load regulation. An impressive $\pm 1.4\%$ accuracy is guaranteed over line, load and temperature.

Additional features of the circuit include current limit, thermal shutdown and noise reduction. Compared to the standard solutions that give warning after the output has lost regulation, the ADP3307 provides improved system performance by enabling the ERR pin to give warning before the device loses regulation.

As the chip’s temperature rises above 165°C, the circuit activates a soft thermal shutdown, indicated by a signal low on the ERR pin, to reduce the current to a safe level.

To reduce the noise gain of the loop, the node of the main divider network (a) is made available at the noise reduction (NR) pin which can be bypassed with a small capacitor (10 nF–100 nF).

APPLICATION INFORMATION

Capacitor Selection: anyCAP

Output Capacitors: as with any micropower device, output transient response is a function of the output capacitance. The ADP3307 is stable with a wide range of capacitor values, types and ESR (anyCAP). A capacitor as low as 0.47 μF is all that is needed for stability. However, larger capacitors can be used if high output current surges are anticipated. There is an upper limit on the size of the output capacitor. The ADP3307 is stable with extremely low ESR capacitors (ESR ≈ 0), such as multilayer ceramic capacitors (MLCC) or OSCON.

Input Bypass Capacitor: an input bypass capacitor is not required; however, for applications where the input source is high impedance or far from the input pins, a bypass capacitor is recommended. Connecting a 0.47 μF capacitor from the input to ground reduces the circuit’s sensitivity to PC board layout. If a bigger output capacitor is used, the input capacitor should be 1 μF minimum.

Noise Reduction

A noise reduction capacitor (C_{NR}) can be used to further reduce the noise by 6 dB–10 dB (Figure 3). Low leakage capacitors in 10 nF–100 nF range provide the best performance. As the noise reduction capacitor increases the high frequency loop-gain of the regulator, the circuit requires a larger output capacitor if it is used. The recommended value is 4.7 μF , as shown in Figure 3. Since the noise reduction pin (NR) is internally connected to a high impedance node, any connection to this node should be carefully done to avoid noise pick up from external sources. The pad connected to this pin should be as small as possible. Long PC board traces are not recommended.

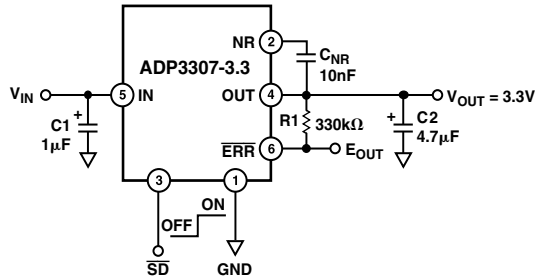


Figure 3. Noise Reduction Circuit

Thermal Overload Protection

The ADP3307 is protected against damage due to excessive power dissipation by its thermal overload protection circuit, which limits the die temperature to a maximum of 165°C. Under extreme conditions (i.e., high ambient temperature and power dissipation), where die temperature starts to rise above 165°C, the output current is reduced until the die temperature has dropped to a safe level. Output current is restored when the die temperature is reduced.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed 125°C.

Calculating Junction Temperature

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT}) I_{LOAD} + (V_{IN}) I_{GND}$$

Where I_{LOAD} and I_{GND} are load current and ground current, V_{IN} and V_{OUT} are input and output voltages respectively.

Assuming $I_{LOAD} = 100$ mA, $I_{GND} = 2$ mA, $V_{IN} = 5.5$ V and $V_{OUT} = 3.3$ V, device power dissipation is:

$$P_D = (5.5 - 3.3) 0.1 + 5.5 \times 2 \text{ mA} = 0.231 \text{ W}$$

$$\Delta T = T_J - T_A = P_D \times \theta_{JA} = 0.231 \times 165 = 38^\circ\text{C}$$

With a maximum junction temperature of 125°C, this yields a maximum ambient temperature of 87°C.

Printed Circuit Board Layout Consideration

Surface mount components rely on the conductive traces or pads to transfer heat away from the device. Appropriate PC board layout techniques should be used to remove heat from the immediate vicinity of the package.

The following general guidelines will be helpful when designing a board layout:

1. PC board traces with larger cross section areas will remove more heat. For optimum results, use PC boards with thicker copper and wider traces.
2. Increase the surface area exposed to open air so heat can be removed by convection or forced air flow.
3. Do not use solder mask or silkscreen on the heat dissipating traces because it will increase the junction-to-ambient thermal resistance of the package.

Shutdown Mode

Applying a high signal to the shutdown pin or tying it to the input pin will turn the output ON. Pulling the shutdown pin down to a low level or tying it to ground will turn the output OFF. In shutdown mode, quiescent current is reduced to less than 1 µA.

Error Flag Dropout Detector

The ADP3307 will maintain its output voltage over a wide range of load, input voltage and temperature conditions. If the output is about to lose regulation, for example, by reducing the supply voltage below the combined regulated output and dropout voltages, the ERR pin will be activated. The ERR output is an open collector that will be driven low.

Once set, the ERRor flag's hysteresis will keep the output low until a small margin of operating range is restored either by raising the supply voltage or reducing the load.

APPLICATIONS CIRCUITS

Crossover Switch

The circuit in Figure 4 shows that two ADP3307s can be used to form a mixed supply voltage system. The output switches between two different levels selected by an external digital input. Output voltages can be any combination of voltages from the Ordering Guide of the data sheet.

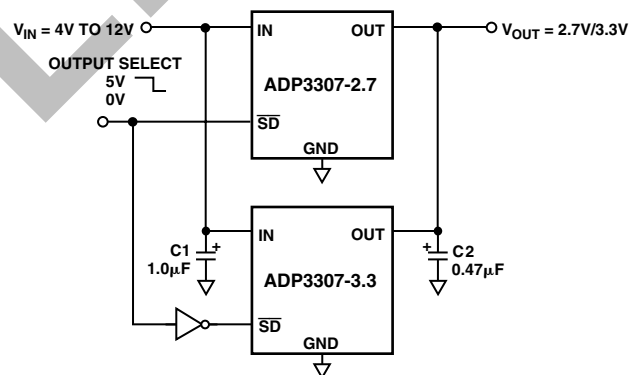


Figure 4. Crossover Switch

Higher Output Current

The ADP3307 can source up to 100 mA without any heatsink or pass transistor. If higher current is needed, an appropriate pass transistor can be used, as in Figure 5, to increase the output current to 1 A.

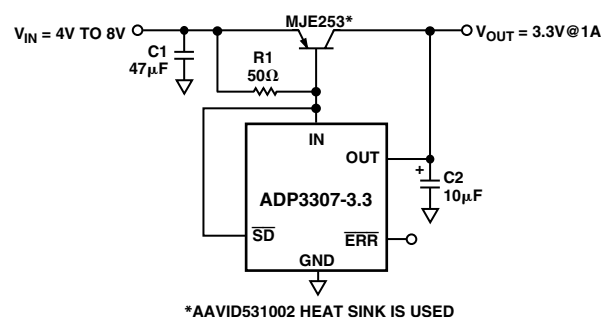


Figure 5. High Output Current Linear Regulator

ADP3307

Constant Dropout Post Regulator

The circuit in Figure 6 provides high precision with low dropout for any regulated output voltage. It significantly reduces the ripple from a switching regulator while providing a constant dropout voltage, which limits the power dissipation of the LDO to 30 mW. The ADP3000 used in this circuit is a switching regulator in the step-up configuration.

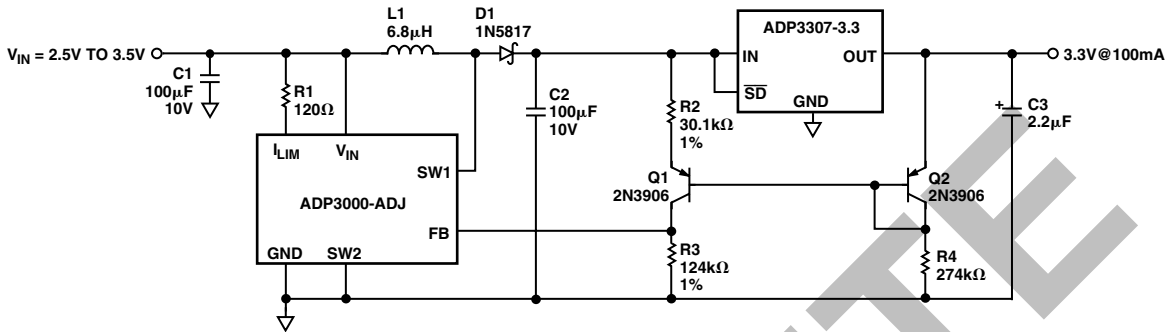
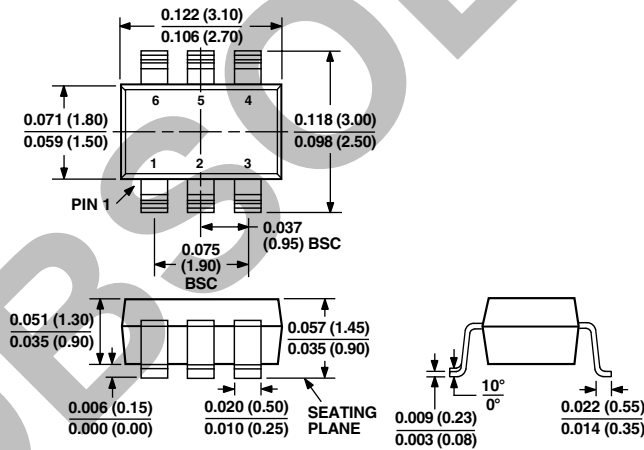


Figure 6. Constant Dropout Post Regulator

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-Lead Plastic Surface Mount (RT-6)



ADP3307–Revision History

| Location | Page |
|--|------|
| Data Sheet changed from REV. 0 to REV. A. | |
| Edits to FEATURES | 1 |
| Edits to GENERAL DESCRIPTION | 1 |
| Addition to the ORDERING GUIDE | 3 |
| Edit to Calculating Junction Temperature section | 7 |
| Edits to Figure 4 | 7 |