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THIS SPEC IS OBSOLETE

Spec No: 001-74847

Spec Title: CY7C1481BV25, 72-MBIT (2 M X 36) FLOW-
THROUGH SRAM

Sunset Owner: Pritesh Mandaliya (PRIT)

Replaced by: None

72-Mbit (2 M × 36) Flow-Through SRAM

Features

- Supports 133 MHz bus operations
- 2 M × 36 common I/O
- 2.5 V core power supply (V_{DD})
- 2.5 V I/O supply (V_{DDQ})
- Fast clock to output time
  - 6.5 ns (133 MHz version)
- Provide high performance 2-1-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed write
- Asynchronous output enable
- CY7C1481BV25 available in JEDEC standard Pb-free 100-pin TQFP package
- IEEE 1149.1 JTAG compatible boundary scan
- ZZ sleep mode option

Functional Description

The CY7C1481BV25 is a 2.5 V, 2 M × 36 synchronous flow through SRAM designed to interface with high speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive edge triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address pipelining Chip Enable ($\overline{CE_1}$), depth expansion Chip Enables (CE_2 and $\overline{CE_3}$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW_x}$ and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

The CY7C1481BV25 enables either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses are initiated with the Processor Address Strobe ($\overline{ADSP}$) or the cache Controller Address Strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the Address Advancement ($\overline{ADV}$) input.

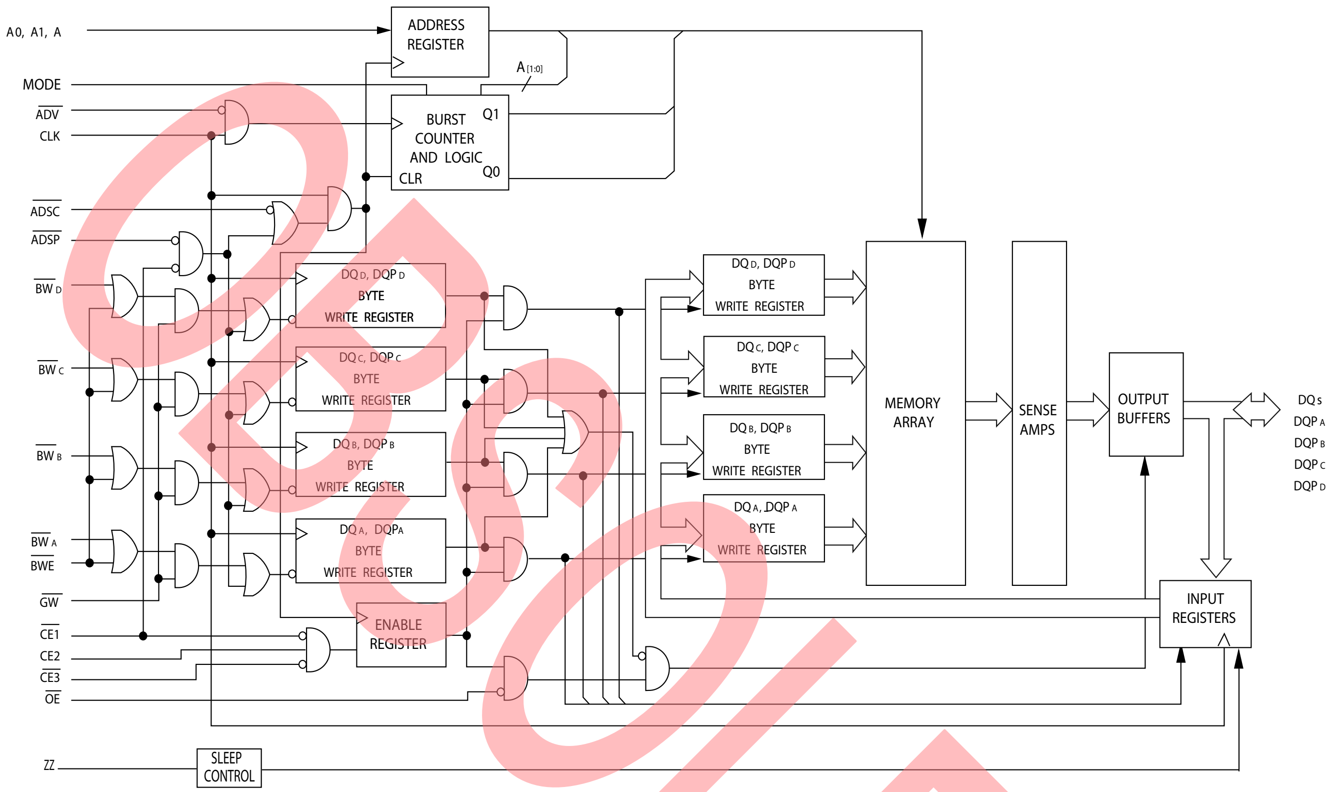
Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

For a complete list of related documentation, click here.

Selection Guide

Description	133 MHz	Unit
Maximum Access Time	6.5	ns
Maximum Operating Current	305	mA
Maximum CMOS Standby Current	120	mA

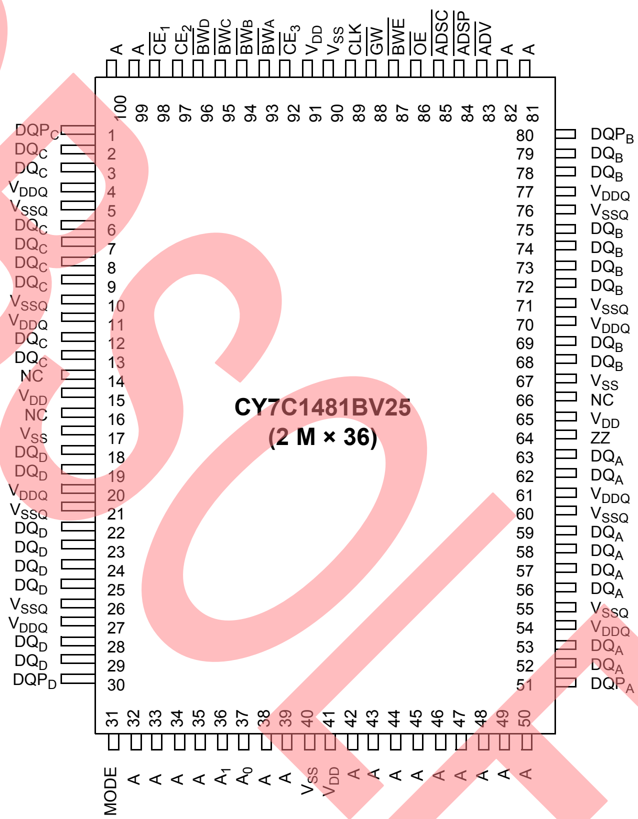
Logic Block Diagram – CY7C1481BV25



Contents

Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



Pin Definitions

Pin Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs Used to Select One of the Address Locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	Input-Synchronous	**Byte Write Select Inputs, Active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, Active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$).
CLK	Input-Clock	**Clock Input**. Captures all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance Input Signal, Sampled on the Rising Edge of CLK**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, Active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
ZZ	Input-Asynchronous	**ZZ "Sleep" Input, Active HIGH**. When asserted HIGH, places the device in a non time-critical "sleep" condition with data integrity preserved. For normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down.
DQ_s	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and DQP_X are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-Synchronous	**Bidirectional Data Parity I/O Lines.** Functionally, these signals are identical to DQ_s. During write sequences, DQP_x is controlled by $\overline{BW}_X$ correspondingly.
MODE	Input-Static	**Selects Burst Order**. When tied to GND, selects linear burst sequence. When tied to V_{DD} or left floating, selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode Pin has an internal pull up.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for the I/O Circuitry**.
V_{SS}	Ground	**Ground for the Core of the Device**.

Pin Definitions (continued)

Pin Name	I/O	Description
V_{SSQ}	I/O Ground	**Ground for the I/O Circuitry**.
NC	–	**No Connects**. Not internally connected to the die. 144M, 288M, 576M, and 1G are address expansion pins are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

The CY7C1481BV25 supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable and is determined by sampling the MODE input. Accesses are initiated with either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}_X$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active, and (2) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW (if the access is initiated by $\overline{ADSC}$, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic. It is then presented to the memory core. If the $\overline{OE}$ input is asserted LOW, the requested data is available at the data outputs a maximum of t_{CDV} after clock rise. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (2) $\overline{ADSP}$ is asserted LOW. The addresses presented are loaded into the address register and the burst inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_X$) are ignored during this first clock cycle. If the write inputs are asserted active on the next clock rise, the appropriate data is latched and written into the device. The device allows byte writes. All I/Os are tri-stated during a byte write. Because this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated after a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active, (2) $\overline{ADSC}$ is asserted LOW, (3) $\overline{ADSP}$ is deasserted HIGH, and (4) the write input signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_X$) indicate a write access. $\overline{ADSC}$ is ignored if $\overline{ADSP}$ is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to DQ_S is written into the specified address location. The device allows byte writes. All I/Os are tri-stated when a write is detected, even a byte write. Because this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tri-stated before data is presented to DQs. As a safety precaution, the data lines are tri-stated after a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1481BV25 provides an on-chip 2-bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to an interleaved burst sequence.

Sleep Mode

The ZZ input pin is asynchronous. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected before entering the “sleep” mode. $\overline{CE}_1$, CE_2, $\overline{CE}_3$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2$ V	–	120	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1481BV25 follows. [1, 2, 3, 4, 5]

Cycle Description	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	X	X	X	L	H	L	X	X	X	L–H	Tri-State
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L–H	Tri-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L–H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L–H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes

1. X = Do Not Care, H = Logic HIGH, L = Logic LOW.
2. $\overline{WRITE}$ = L when any one or more byte write enable signals and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
4. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to enable the outputs to tri-state. $\overline{OE}$ is a do not care for the remainder of the write cycle.
5. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as outputs when $\overline{OE}$ is active (LOW).

Truth Table for Read/Write

The read-write truth table for CY7C1481BV25 follows. [6, 7]

Function (CY7C1481BV25)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A (DQ_A, DQP_A)	H	L	H	H	H	L
Write Byte B(DQ_B, DQP_B)	H	L	H	H	L	H
Write Bytes A, B (DQ_A, DQ_B, DQP_A, DQP_B)	H	L	H	H	L	L
Write Byte C (DQ_C, DQP_C)	H	L	H	L	H	H
Write Bytes C, A (DQ_C, DQ_A, DQP_C, DQP_A)	H	L	H	L	H	L
Write Bytes C, B (DQ_C, DQ_B, DQP_C, DQP_B)	H	L	H	L	L	H
Write Bytes C, B, A (DQ_C, DQ_B, DQ_A, DQP_C, DQP_B, DQP_A)	H	L	H	L	L	L
Write Byte D (DQ_D, DQP_D)	H	L	L	H	H	H
Write Bytes D, A (DQ_D, DQ_A, DQP_D, DQP_A)	H	L	L	H	H	L
Write Bytes D, B (DQ_D, DQ_A, DQP_D, DQP_A)	H	L	L	H	L	H
Write Bytes D, B, A (DQ_D, DQ_B, DQ_A, DQP_D, DQP_B, DQP_A)	H	L	L	H	L	L
Write Bytes D, B (DQ_D, DQ_B, DQP_D, DQP_B)	H	L	L	L	H	H
Write Bytes D, B, A (DQ_D, DQ_C, DQ_A, DQP_D, DQP_C, DQP_A)	H	L	L	L	H	L
Write Bytes D, C, A (DQ_D, DQ_B, DQ_A, DQP_D, DQP_B, DQP_A)	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Notes
6. X = Do Not Care, H = Logic HIGH, L = Logic LOW.
7. Table only includes a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. An appropriate write is performed based on which byte write is

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with
Power Applied .... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.3 V to +3.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.3 V to $+V_{DD}$

DC Voltage Applied to Outputs
in Tri-State ....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage ....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage
(MIL-STD-883, Method 3015) .... >2001 V

Latch Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	2.5 V – 5% / + 5%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Electrical Characteristics

Over the Operating Range

Parameter [8, 9]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			2.375	2.625	V
V_{DDQ}	I/O Supply Voltage	For 2.5 V I/O		2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	For 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	For 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage [8]	For 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage [8]	For 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input Current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DDQ,}$ Output Disabled		–5	5	µA
I_{DD} [10]	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	7.5 ns cycle, 133 MHz	–	305	mA
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz	–	170	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{DD}$ – 0.3 V or $V_{IN} \leq$ 0.3 V, f = 0, inputs static	7.5 ns cycle, 133 MHz	–	120	mA
I_{SB3}	Automatic CE Power Down Current – CMOS Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{DDQ}$ – 0.3 V or $V_{IN} \leq$ 0.3 V, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz	–	170	mA
I_{SB4}	Automatic CE Power Down Current – TTL Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{DD}$ – 0.3 V or $V_{IN} \leq$ 0.3 V, f = 0, inputs static	7.5 ns cycle, 133 MHz	–	135	mA

Notes
8. Overshoot: $V_{IH(AC)} < V_{DD}$ + 1.5 V (pulse width less than $t_{CYC}/2$). Undershoot: $V_{IL(AC)}$ > –2 V (pulse width less than $t_{CYC}/2$).
9. $T_{Power-up}$: assumes a linear ramp from 0 V to $V_{DD(minimum)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.
10. The operation current is calculated with 50% read cycle and 50% write cycle.

Capacitance

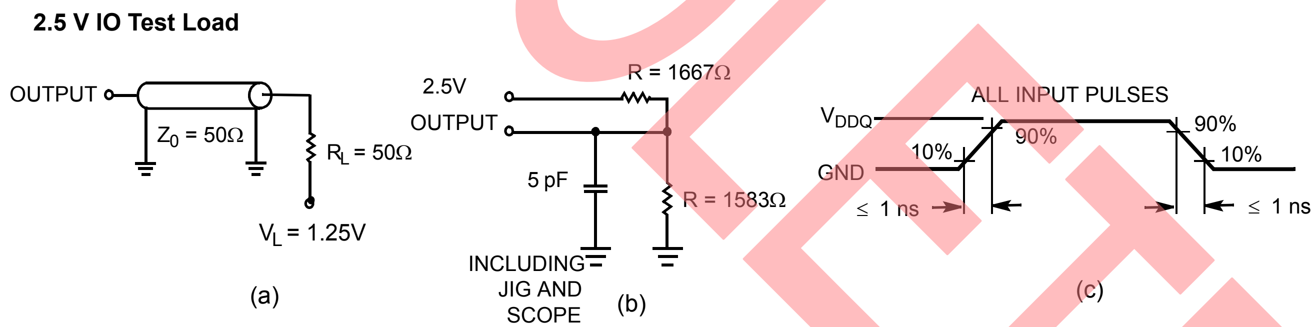
Parameter [11]	Description	Test Conditions	100-pin TQFP Package	Unit
$C_{ADDRESS}$	Address Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 2.5 V, V_{DDQ} = 2.5 V	6	pF
C_{DATA}	Data Input Capacitance		5	pF
C_{CTRL}	Control Input Capacitance		8	pF
C_{CLK}	Clock Input Capacitance		6	pF
C_{IO}	Input/Output Capacitance		5	pF

Thermal Resistance

Parameter [11]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	24.63	°C/W
Θ_{JC}	Thermal resistance (junction to case)		2.28	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Note
11. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

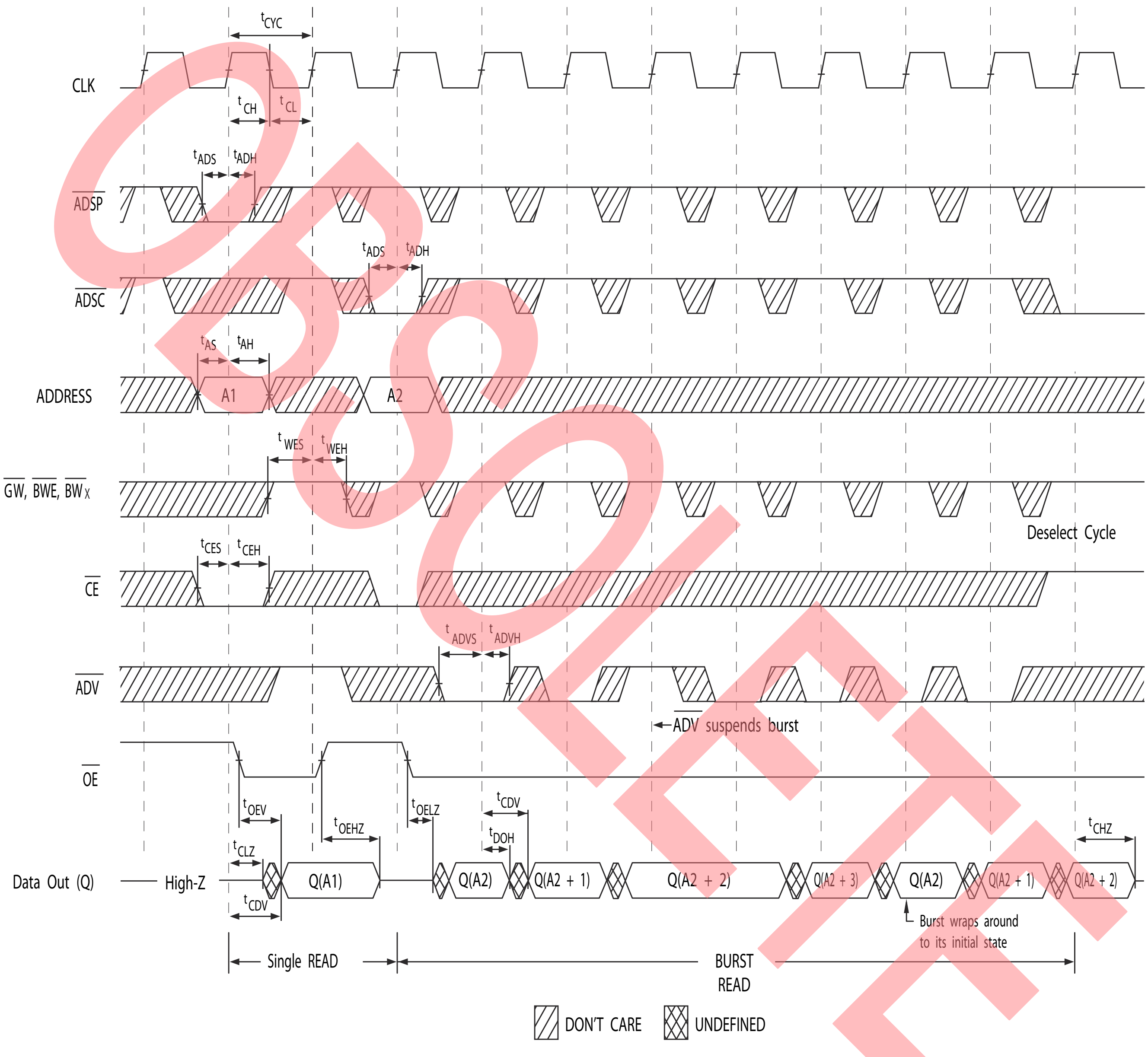
Parameter [12, 13]	Description	133 MHz		Unit
		Min	Max	
t_{POWER}	V_{DD}(typical) to the First Access [14]	1	–	ms
Clock				
t_{CYC}	Clock Cycle Time	7.5	–	ns
t_{CH}	Clock HIGH	2.5	–	ns
t_{CL}	Clock LOW	2.5	–	ns
Output Times				
t_{CDV}	Data Output Valid After CLK Rise	–	6.5	ns
t_{DOH}	Data Output Hold After CLK Rise	2.5	–	ns
t_{CLZ}	Clock to Low Z [15, 16, 17]	3.0	–	ns
t_{CHZ}	Clock to High Z [15, 16, 17]	–	3.8	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid	–	3.0	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low Z [15, 16, 17]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High Z [15, 16, 17]	–	3.0	ns
Setup Times				
t_{AS}	Address Setup Before CLK Rise	1.5	–	ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Setup Before CLK Rise	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ Setup Before CLK Rise	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Setup Before CLK Rise	1.5	–	ns
t_{DS}	Data Input Setup Before CLK Rise	1.5	–	ns
t_{CES}	Chip Enable Setup	1.5	–	ns
Hold Times				
t_{AH}	Address Hold After CLK Rise	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Hold After CLK Rise	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5	–	ns
t_{DH}	Data Input Hold After CLK Rise	0.5	–	ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5	–	ns

Notes

12. Timing reference level is 1.25 V when V_{DDQ} = 2.5 V.
13. Test conditions shown in (a) of Figure 2 on page 11 unless otherwise noted.
14. This part has an internal voltage regulator; t_{POWER} is the time that the power is supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
15. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 2 on page 11. Transition is measured ±200 mV from steady-state voltage.
16. At any supplied voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. The device is designed to achieve High Z before Low Z under the same system conditions.
17. This parameter is sampled and not 100% tested.

Timing Diagrams

Figure 3. Read Cycle Timing [18]



Note

18. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, CE_2 is LOW, or $\overline{CE}_3$ is HIGH.

Timing Diagrams (continued)

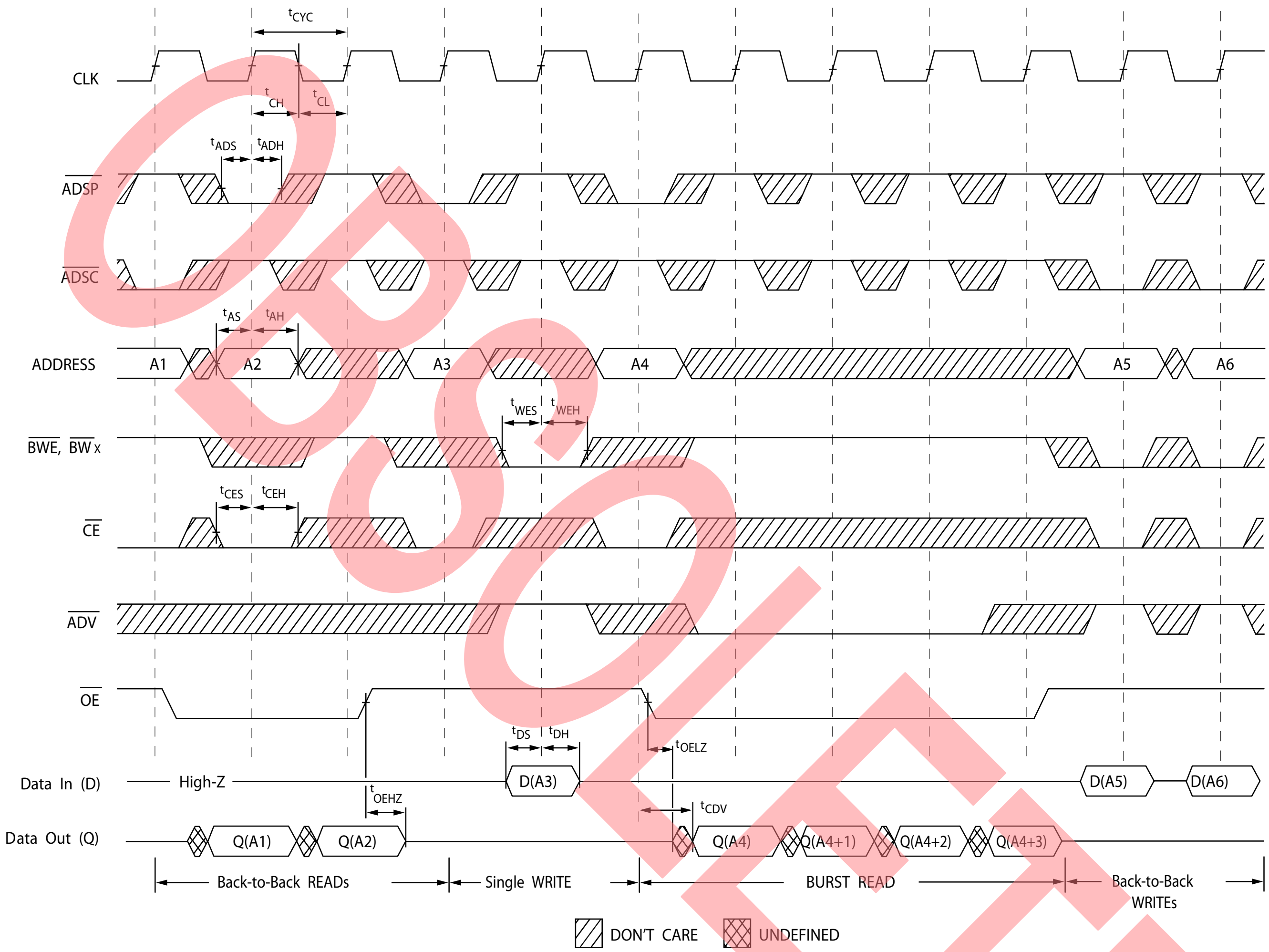
Figure 4. Write Cycle Timing [19, 20]

Notes

19. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE_1}$ is HIGH, CE_2 is LOW, or $\overline{CE_3}$ is HIGH.
20. Full width write can be initiated by either $\overline{GW}$ LOW, or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW_X}$ LOW.

Timing Diagrams (continued)

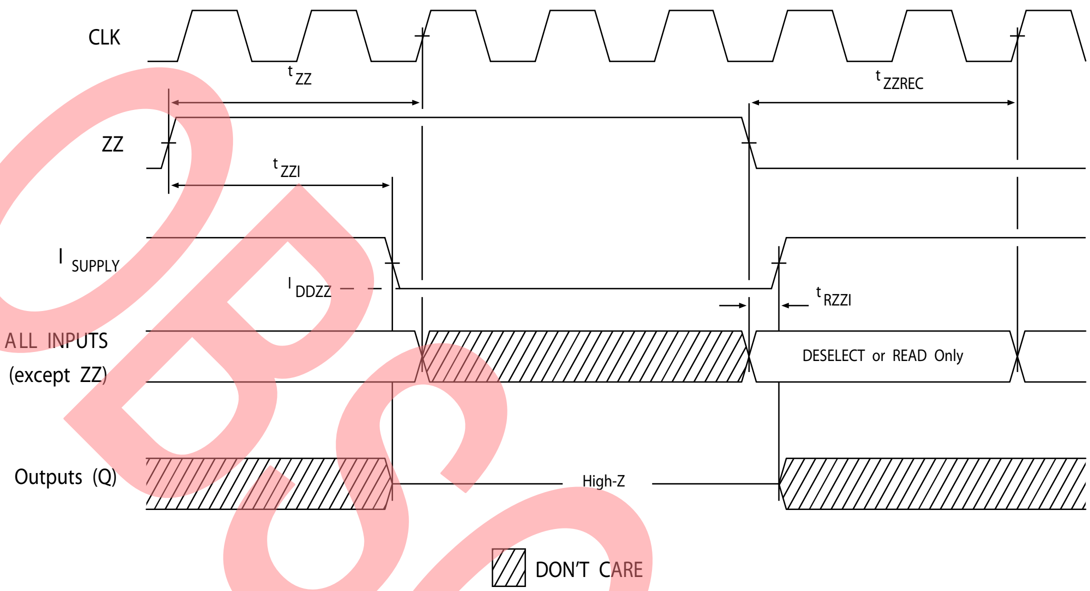
Figure 5. Read/Write Cycle Timing [21, 22, 23]



Notes
21. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE_1}$ is HIGH, CE_2 is LOW, or $\overline{CE_3}$ is HIGH.
22. The data bus (Q) remains in High Z following a write cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
23. $\overline{GW}$ is HIGH.

Timing Diagrams (continued)

Figure 6. ZZ Mode Timing [24, 25]



Notes
24. Device must be deselected when entering ZZ mode. See Truth Table on page 8 for all possible signal conditions to deselect the device.
25. DQs are in High Z when exiting ZZ sleep mode.

Ordering Information

Not all of the speed, package, and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1481BV25-133AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial

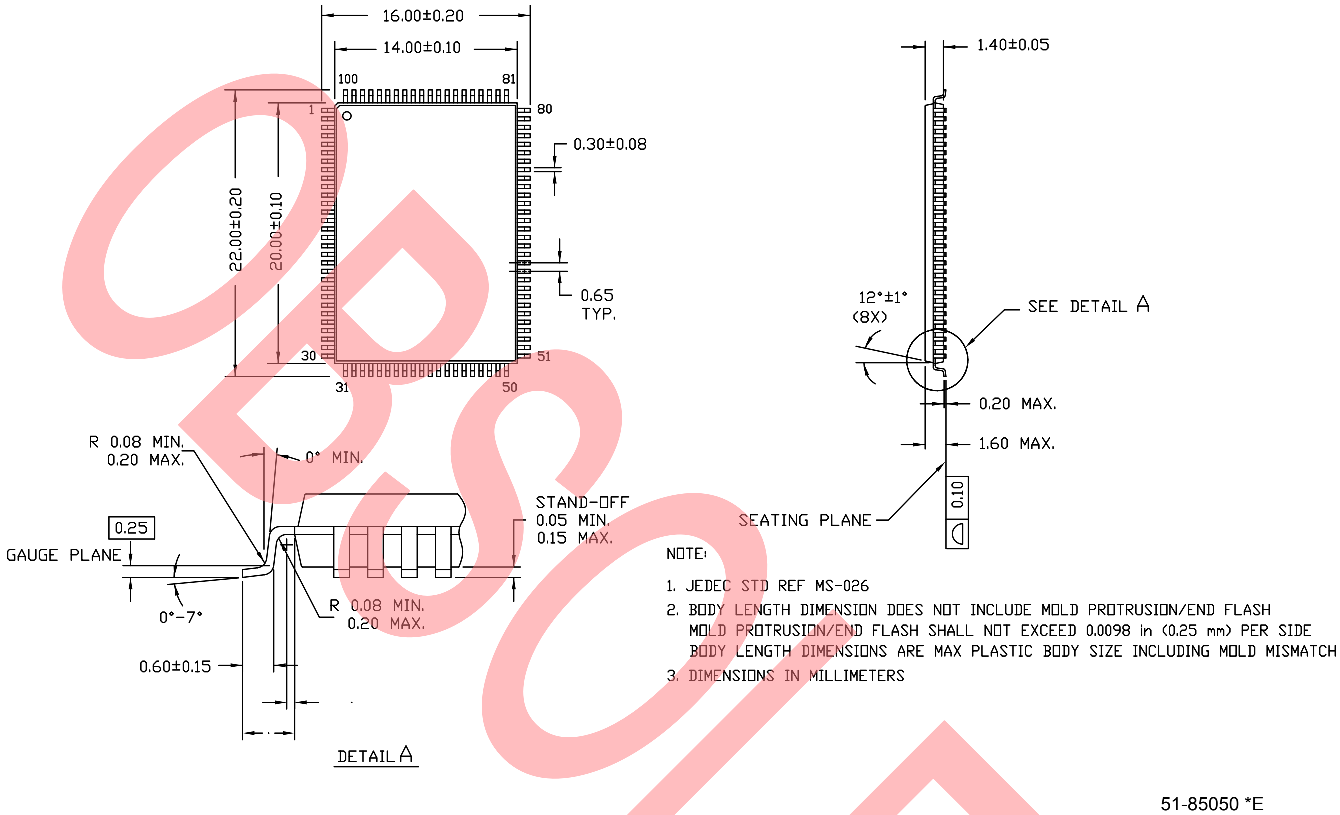
Ordering Code Definitions

CY 7 C 1481 B V25 - 133 A X I

- Temperature range: I = Industrial = –40 °C to +85 °C
- X = Pb-free
- Package Type: A = 100-pin TQFP
- Speed Grade: 133 MHz
- V25 = 2.5 V V_{DD}
- Process Technology: B ≥ errata fix PCN084636
- Part Identifier: 1481 = SCD, 2 Mb × 36 (72 Mb)
- Technology Code: C = CMOS
- Marketing Code: 7 = SRAM
- Company ID: CY = Cypress

Package Diagrams

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal-Oxide-Semiconductor
EIA	Electronic Industries Alliance
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	3617660	05/15/2012	PRIT / GOPA	New data sheet.
*A	4010294	05/24/2013	PRIT	No technical updates. Completing Sunset Review.
*B	4571750	11/18/2014	PRIT	Added documentation related hyperlink in page 1 Updated package diagram from 51-85050*D to 51-85050*E
*C	4810850	06/25/2015	PRIT	Obsolete document. Completing Sunset Review.

Document Title: CY7C1481BV25, 72-Mbit (2 M × 36) Flow-Through SRAM
Document Number: 001-74847

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