SEMTECH
Today's Results...Tomorrow's Vision

ADVANCED PRODUCT DISCONTINUANCE NOTIFICATION

Date: March 10, 2015

☐	Semtech Corporation, 200 Flynn Road, Camarillo CA 93012
☒	Semtech Canada Corporation, 4281 Harvester Road, Burlington, Ontario L7L 5M4 Canada
☐	Semtech Irvine, 5141 California Ave., Suite 100, Irvine CA 92617
☐	Semtech Neuchatel Sarl, Route des Gouttes d'Or 40, CH-2000 Neuchatel Switzerland
☐	Nanotech Semiconductor, Semtech Corporation, 2 West Point Court, Bristol, United Kingdom, BS32 4PY
☐	Semtech Corpus Christi SA de CV, Carretera Matamorros Edificio 7, Reynosa, Tamaulipas, Mexico 88780
☐	

Product Discontinuance Details

Purpose, Description and Effect of Change:

Due to unforeseen supply constraints, we are no longer able to supply the GN4121-CBE3 x1 Lane PCIe Bridge to Local Bus device. However, we are able to supply the GN4124-CBE3 x4 Lane PCIe Bridge to Local Bus device as a fully compatible drop in replacement part.

The GN4121 and GN4124 parts are physically identical and share the same manufacturing flow and final test process. Only the part number marking on the package distinguishes the difference between the two products. All reliability and qualification data is identical for both part numbers.

In light of this, we would like all existing GN4121 customers to switch to the GN4124 with immediate effect. Existing GN4121 designs will have ball E4 tied to 3.3V VCC, which will configure the GN4124 to operate as a GN4121 in x1 PCIe mode. Therefore, no design or PCB changes are required. The GN4124 will be functionally identical to the GN4121 in a GN4121-based x1 PCIe application.

Formal End of Life Notification will follow upon review of customer feedback.

Part Number(s) Affected:	**Customer Part Number(s) Affected:** ☒ N/A
GN4121-CBE3	

Replacement or Alternate Part Number(s) ☐ N/A or Not Offered

GN4124-CBE3

Last Time Buy (LTB) Date	**NA**	**Must Accept Final Delivery by**	**NA**
Sample Availability of Alt. Part	**Now**	**Qualification Report Availability of Alt. Part**	**Now**

Supporting Documents for Alternate or Replacement parts/Attachments:

1. **GN4124-CBE3 Datasheet (GENDOC-048407)**
2. **GN4124-CBE3 Reliability Qualification Report (GENDOC-052220)**

ADVANCED PRODUCT DISCONTINUANCE NOTIFICATION

Date: March 10, 2015

Additional Provisions		
We regret the inconvenience and impact this notice may cause your company. Semtech's sales, marketing, and distribution personnel stand ready to assist you in placing your company's final orders, or in providing the product information you require. For product inquiries or purchase order information, please contact your local Semtech sales representative.		
Issuing Authority		
Semtech Business Unit:	SIPG	
Semtech Contact Info:	Luis Blanco Semtech Corporation Sr. Manager, Quality Engineering 4281 Harvester Road Burlington, ON L7L 5M4 lblanco@semtech.com Office: (905) 632-7253 Fax: (905) 632-2055	[signature]
FOR FURTHER INFORMATION & WORLDWIDE SALES COVERAGE: http://www.semtech.com/contact/index.html#support		

GN4124
x4 Lane PCI Express to Local Bridge

Data Sheet

Revision History

Version	ECR	Date	Changes and Modifications
2	151915	May 2009	Created new document describing functionality and the register map for GN4124 & GN4121 devices. These common sections have been removed.
1	151527	May 2009	It is now a Data Sheet. Added the content of the document: GN4124 x4 PCI Express to Local Bus Bridge User Manual (Document ID: 47719) to this data sheet. This User Manual is no longer a stand-alone document. Changed some parameters in Table 2-1 (EEPROM_EN), Table 3-2, Table 3-3, Table 5-2 and Table 13-2. Changed Figure 4-2, Figure 6-2, Figure 7-1 and Figure 9-16. Modified descriptions in 9.4 Operation, 9.7.3 FCL FPGA Configuration and 9.7.4 FCL FSM FPGA Configuration. Changes to registers to PCI_BAR0_LOW, PCI_BAR2_LOW, PCI_BAR2_HIGH, PCI_BAR4_LOW, PCI_BAR4_HIGH, PCI_SUB_VENDOR, PCI_SUB_SYS, PCIE_DEVICE_CAP, PCIE_DCR, INT_CTRL, INT_STAT, INT_CFG0-7, GPIO_DIRECTION_MODE, GPIO_OUTPUT_ENABLE, GPIO_OUTPUT_VALUE, GPIO_INT_MASK, GPIO_INT_MASK_CLR (Note: formerly GPIO_INT_ENABLE), GPIO_INT_MASK_SET (Note: formerly GPIO_INT_DISABLE), GPIO_INT_STATUS, GPIO_INT_TYPE, GPIO_INT_VALUE, GPIO_INT_ON_ANY and FCL_CTRL.
D	151519	March 2009	Clarified output voltage and local bus timing in Table 3-6 and Table 3-11.
C	150789	December 2008	Corrected pin assignments and definitions. Updated electrical characteristics. Corrected Figure 2-2. Updated Local Bus Interface clock range.
B	150182	August 2008	Corrected pin assignments, part number and other updates.
A	148626	May 2008	New document.

Contents

GN4124 x4 Lane PCI Express to Local Bridge Data Sheet

1. Introduction

For the past decade, PCI has been a dominant interconnect for both PC and embedded systems. With the shift to high-speed serial interfaces, PCI Express® is quickly replacing parallel PCI. As a leader in providing solutions for high-speed serial communications, Gennum has developed the GN4124 family of PCI bridge controller components to complement FPGA devices. The GN4124 is specifically designed to take advantage of the architectural features of low-cost FPGA devices that do not have PCI Express capable SerDes on-chip. The result is a low-cost bridging solution for high-performance native PCI Express bridging.

The GN4124 is a desirable companion to large FPGA devices, where the requirement for firmware upgrading and on-the-fly reconfiguration are required.

The GN4124 is a 4-lane PCI Express to local bus bridge that is designed to work as a companion for FPGA devices to provide a complete bridging solution for general applications. In addition to a 4-lane PCI Express compliant PHY interface, the GN4124 contains the link and transaction layers, and an applications interface that is ideally suited to FPGA interfacing using a small number of pins.

Since the PCI Express transaction/link IP is hard-wired into the GN4124, there is no need to license PCIe IP. The level of integration and very low power operation of the GN4124 make it an ideal alternative to using a PIPE PHY, where IP licensing and the cost of FPGA resources and power consumption is unattractive by comparison. Using the GN4124, allows FPGA resources to be spent on what differentiates the product, rather than on implementing the PCI Express protocol.

1.1 Features

- 4 Lane PCI Express interface
  - Complies with PCI Express Base Specification 1.1
  - On-chip PHY, transaction, and link layer eliminates the cost of IP licensing
  - Two hardware virtual channels supported
  - Payload size of up to 512 bytes with up to three outstanding transactions in each direction
  - Supports 3x64-bit base address registers
  - Provides flexible power management capability
- Provides pin efficient local bus interface for easy attachment to popular low-cost FPGA devices
  - Uses DDR SSTL I/O for high-speed data transfer (up to 800MB/s)

- FPGA source code provided for 64-bit master/target read/write buses for easy user logic attachment
- Local bus may be operated asynchronously to the PCIe clock rate for power optimization

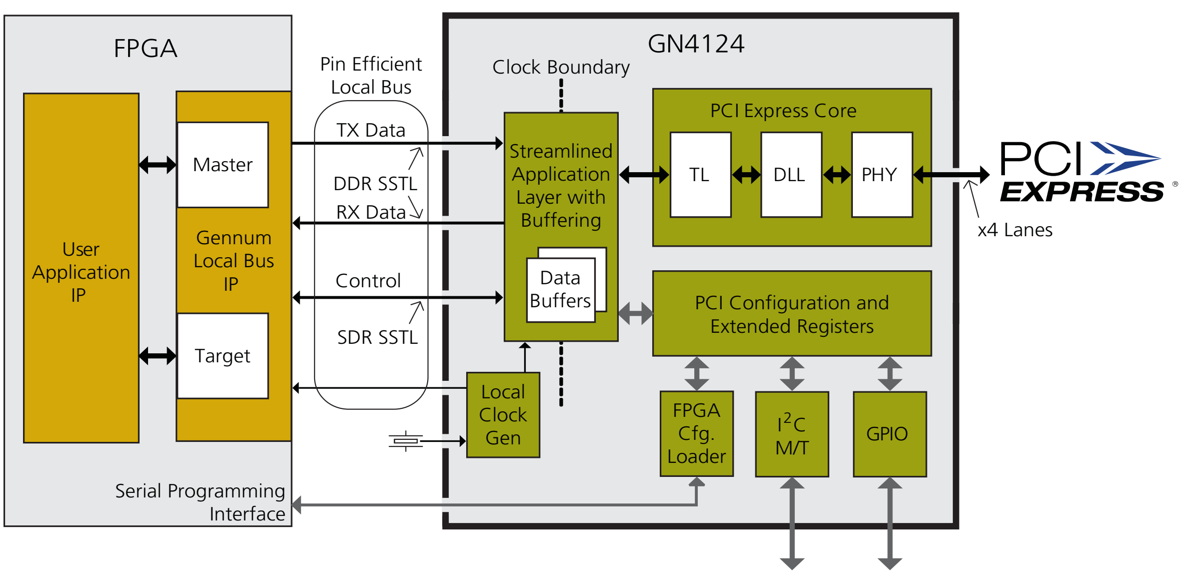
- "Live" on power up
  - On-chip type 0 PCI configuration space enables auto detection without FPGA activity
  - On-chip extended configuration space supports power management, serial number, MSI, and PCIe capability registers

- FPGA bitstream loader
  - Allows easy configuration of the attached FPGA through PCIe
  - Provides on-the-fly FPGA reconfiguration capability

- 2-wire master/target
  - Boot master mode allows PCI configuration space defaults to be loaded from a small EEPROM upon system reset
  - General master mode allows attached 2-wire devices to be read/written
  - Target mode allows internal registers to be accessed from an external circuit or processor

A simplified block diagram of the GN4124 chip is shown in Figure 1-1.

Figure 1-1: GN4124 with FPGA Simplified Block Diagram



1.2 Live on Power-up

Since the GN4124 contains a complete type 0 PCI configuration space, it is live on power-up so that a plug-and-play BIOS can auto-detect it and enumerate it without an attached FPGA having to be configured.

1.3 FPGA On-the-Fly Configuration Loader

An FPGA bitstream may be downloaded from the host system over PCIe to the attached FPGA using the on-chip FPGA configuration loader. This eliminates the expense of a dedicated FPGA ROM and makes on-the-fly reconfiguration and firmware upgrades simple. The ability to dynamically configure an attached FPGA over PCIe makes the GN4124 an ideal companion to all ranges of FPGA devices, including large SerDes capable devices, that require reconfiguration or firmware upgrades over PCIe.

1.4 Local Bus Interface

The local bus interface uses a combination of single and dual data rate SSTL I/O to accomplish very high data rates in the fewest possible pins. A singe data rate clock is used for SSTL control signals and separate dual data rate source synchronous clocking is used for the DDR SSTL data. The SDR control signals operate at up to 200MHz and the DDR I/O operate at up to 400MT/s across 16 bits using a 200MHz DDR clock. This provides 800MB/s in each direction.

The local bus may operate asynchronously from the PCI Express rate. In order to save power, the local bus clock can operate at the lowest possible rate required by an application.

The local bus protocol facilitates four types of transactions:

- PCIe-to-Local Target Writes: A PCIe agent (such as the host processor/root complex) writes data to the local bus.
- PCIe-to-Local Target Reads: A PCIe agent reads data from the local bus. Reads are split into a request phase (address phase) and a completion phase (data phase).
- Local-to-PCIe Master Writes: The attached FPGA writes data to a PCIe device (such as host memory via a root complex).
- Local-to-PCIe Master Reads: The attached FPGA reads data from a PCIe device.

The PCIe-to-Local transactions would typical involve a target controller implemented in the FPGA. Local-to-PCIe Master transactions allow a DMA controller in the FPGA to access PCI Express devices.

1.5 Virtual Channel Support

The GN4124 has two independent virtual channels that support the eight PCIe defined traffic classes. This enables high local bus utilization by supporting non-blocking traffic between virtual channels. This is accomplished with separate on-chip buffering resources for each of the two virtual channels. For example, when write buffering is full for VC0 and VC1 has room, then VC1 traffic may proceed without reference to the state of VC0.

Virtual channels may be used to separate different types of application traffic. For example, a DMA engine in the FPGA may be aggressively reading and writing host memory to stream video data. At the same time another agent in the FPGA may need to communicate low bandwidth, latency sensitive synchronization information. If the two types of traffic are segregated in terms of virtual channels and traffic classes, then the low latency traffic can be allowed to pass the high bandwidth traffic.

1.6 PCI Express Application Layer

The on-chip applications layer transfers data between the PCI Express port and an attached FPGA using the local bus interface. It provides a mechanism to access internal registers through configuration space access and through one of the Base Address Registers (BAR4). The applications layer supports the transmission of message signalled interrupts.

1.7 Interrupt Controller

A flexible interrupt controller automatically generates PCIe message signalled interrupts from either external pins (GPIO pins) or internally generated interrupt sources. The interrupt controller can route any interrupt source to up to four GPIO pins.

1.8 2-Wire Serial Controller

An on-chip I^2C compatible controller provides both a master and target mode. After device reset, default configuration register values, such as Subsystem Vendor ID and BAR sizes, can be automatically loaded from a small serial EEPROM. After initialization, an external 2-wire master can access on-chip registers to read/write them.

1.9 Data Sheet Usage

The GN4124 Data Sheet includes detailed specifications on GN4124 device. However, there are other complementary documents to assist designers available on the Gennum Web site: www.gennum.com/mygennum. A complete set of documentation includes the following:

- GN4124 Data Sheet (this document)
- GN412x PCI Express Family Reference Manual (Document ID: 52624), which provides the details on functionality and the register map associated with the GN412x family of chips
- GN4124 Master List of Documents & Electronic Files (Document ID: 52423), which provides a summary of the content of the documentation & electronic files, to help navigate the content on MyGennum
- Reference Design Kit (RDK) board and the asssociated documentation

Following chapters detail the specifications of the GN4124:

- 2. Pin Descriptions
- 3. Electrical Characteristics
- 5. Package & Ordering Information

Before finalizing a system design based on the GN4124, please contact Gennum to verify that you have the most recent specifications.

Gennum is constantly trying to improve the quality of its product documentation. If you have any questions or comments, please contact Gennum Technical Support.

1.10 Getting Help from Gennum

For technical support, contact Gennum by telephone or e-mail. E-mail ensures the quickest response. The most up-to-date technical support information is also posted on the Gennum website. E-mail: vbapps@gennum.com.

1.11 Getting Answers to PCI Express Related Questions

This data sheet assumes a basic understanding of the PCI Express Specification. If you are looking for a copy of the specification please contact the PCI Special Interest group at 503-619-0569 or visit their Web site at: http://www.pcisig.com.

If you are not familiar with the PCI Express specification, a good place to start is by reading one of several books on the subject. One of the most popular is PCI Express System Architecture written by Tom Shanley, Don Anderson, and Ravi Budruk (published by MindShare Inc.).

2. Pin Descriptions

2.1 Pin Assignments

Figure 2-1: GN4124 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS_PCIE	PERn0	VSS_PCIE	DBG0	DBG7	GPIO15	GPIO9	SPRI_CLK	TDI	GPIO7	GPIO6	SPRI_DONE	GPIO4	TDO	PLL_TEST_OUT	VSS	A
B	VDD_PCIE	PERp0	NC	DBG2	DBG6	GPIO13	GPIO14	$\overline{RSTIN}$	GPIO8	SPRI_DATAOUT	SCLK	TRST	SPRI_XI_SWAP	SPRI_STATUS	VSS	L2P_DATA15	B
C	PETp0	VSS_PCIE	VDD_PCIE	VSS	DBG5	DBG1	GPIO12	GPIO10	$\overline{RSTOUT33}$	GPIO2	SPRI_CONFIG	SDATA	LB_REF_CLK_MO	VSS	L2P_DATA7	L2P_DATA14	C
D	PETn0	VSS_PCIE	VDD_PCIE	VSS	VDDC	SCAN_EN	DBG3	VDDC	GPIO3	NC	GPIO1	LB_REF_CLK_MI	VDDC	NC	L2P_DATA6	VDDC	D
E	VDDP	PETn1	VSS_PCIE	VSS	EEPROM_EN	TEST_EN	DBG4	VCCO33	VCCO33	VDDC	GPIO5	GPIO0	VDDC	NC	L2P_DATA5	L2P_DATA13	E
F	VTT_AB	PETp1	VSS_PCIE	NC	VDDW	VDDC	GPIO11	VCCO33	VCCO33	TMS	TCK	VDDC	VDDC	L2P_RDY	L2P_DATA4	L2P_DATA12	F
G	PERp1	VSS_PCIE	VDDAUX	VSS	PECLKINp	VSS	VSS	VSS	VSS	VSS	VSS	VDDC	NC	L2P_EDB	L2P_CLKn	L2P_CLKp	G
H	PERn1	VSS_PCIE	PCIE_VDDA	VDDC	PECLKINn	VSS	VSS	VSS	VSS	VSS	VCCO18	VCCO18	VSS	L2P_DFRAME	VDDC	L2P_VALID	H
J	PERn2	VSS_PCIE	PCIE_VDDA	VSS	VSS	NC	VSS	VSS	VSS	VSS	VCCO18	VCCO18	VDDC	L_WR_RDY1	L2P_DATA3	L2P_DATA11	J
K	PERp2	VSS_PCIE	VSS	VDDP	VDDW	LCLK_MODE3	VSS	VSS	VSS	VSS	VSS	VSS	NC	L_WR_RDY0	VDDC	L2P_DATA10	K
L	VSS	PETp2	VSS_PCIE	LCLK_MODE2	VDDC	VDDC	NC	VCCO18	VCCO18	VDDC	VSS	VSS	VDDC	P_RD_D_RDY1	L2P_DATA2	L2P_DATA9	L
M	VTT_CD	PETn2	VSS_PCIE	LCLK_MODE1	LCLK_MODE0	VDDC	VSS	VCCO18	VCCO18	VDDC	VSS	VSS	NC	P_RD_D_RDY0	L2P_DATA1	VDDC	M
N	PETn3	VSS_PCIE	VDD_PCIE	NC	VSS	RX_ERROR	NC	VDDC	P_WR_REQ0	VDDC	P_WR_RDY1	P_WR_RDY0	PLL_AVSS	TX_ERROR	L2P_DATA0	L2P_DATA8	N
P	PETp3	VSS_PCIE	VDD_PCIE	VSS	P2L_DATA15	VDDC	P2L_VALID	P2L_CLKp	P2L_RDY	P_WR_REQ1	VC_RDY1	VC_RDY0	VDDC	LCLK	VDDC	$\overline{RSTOUT18}$	P
R	VDD_PCIE	PERp3	VSS	P2L_DATA14	P2L_DATA13	P2L_DATA12	P2L_DFRAME	P2L_CLKn	P2L_DATA11	VREF	P2L_DATA10	P2L_DATA9	P2L_DATA8	NC	VSS	LCLKn	R
T	VSS_PCIE	PERn3	VSS_PCIE	VDDC	P2L_DATA7	P2L_DATA6	P2L_DATA5	P2L_DATA4	P2L_DATA3	P2L_DATA2	P2L_DATA1	VDDC	P2L_DATA0	PLL_AVDD	NC	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

3.3V 1.8V 1.2V 900mV 0V

2.2 Pin Descriptions

Table 2-1: GN4124 Pin Descriptions

Group	Pin No.	No. of Pins	Pin Name	I/O	Description
Global	B8	1	$\overline{\text{RSTIN}}$	I	Global Asynchronous Reset (Active LOW). LVCMOS, 3.3V, input, hysteresis.
	C9	1	$\overline{\text{RSTOUT33}}$	O	Reset Output; 3.3V (Active LOW). 3.3 V LVCMOS, totem-pole.
	D12	1	LB_REF_CLK_MI	I	Local Bus Reference Clock Crystal or Oscillator Input.
	C13	1	LB_REF_CLK_MO	O	Local Bus Reference Clock Crystal feedback output. Functional mode only.
	H3, J3	2	PCIE_VDDA	P	Clock Reference Analog Supply. (1.2V)
	G5, H5	2	PECLKINp, PECLKINn	I	PCIe Reference Clock Signal. For a PCI Express add-in card, these signals should be driven by the card edge connector and AC coupled using 150nF capacitors.
	E5	1	EEPROM_EN	I	Used to report that EEPROM is present. (1 = present) LVCMOS, 3.3V, input. EEPROM_EN should be tied HIGH, to allow the internal GN4124 registers to load on power up from the EEPROM. Refer to Initialization from a 2-Wire EEPROM from on what is required for EEPROM boot up options.

Group	Pin No.	No. of Pins	Pin Name	I/O	Description
Global: Test Interface	A9	1	TDI	I	JTAG Test Data Input. LVCMOS, 3.3V, input, pull-up.
	F10	1	TMS	I	JTAG Test Mode Select Input. LVCMOS, 3.3V, input, pull-up.
	F11	1	TCK	I	JTAG Test Clock. LVCMOS, 3.3V, input.
	B12	1	TRST	I	JTAG Test Reset. LVCMOS, 3.3V, input, hysteresis, pull-up.
	A14	1	TDO	O	JTAG Test Data Output. LVTTL, 3.3V, output, 6mA, tristate.
	D6	1	SCAN_EN	I	Scan Enable (Tied LOW for normal operations). LVCMOS, 3.3V, input, pull-down.
	E6	1	TEST_EN	I	Test Mode Enable (Tied LOW for normal operations). LVCMOS, 3.3V, input, pull-down.
	A15	1	PLL_TEST_OUT	I/O	PLL Test Output (No connect for normal operations). LVCMOS, 3.3V, bidirectional, 4mA, tristate.
Global: 2-Wire Interface	B11	1	SCLK	I/O	Two-wire Clock port. LVCMOS, 3.3V, bidirectional, 4mA, tristate.
	C12	1	SDATA	I/O	Two-wire Data port. LVCMOS, 3.3V, bidirectional, 4mA, tristate.
Global: General Purpose Interface	A6, B7, B6, C7, F7, C8, A7, B9, A10, A11, E11, A13, D9, C10, D11, E12	16	GPIO[15:0]	I/O	General Purpose Input/Output. LVCMOS, 3.3V, bidirectional, 4mA, tristate.
Global: Debug Interface	A5, B5, C5, E7, D7, B4, C6, A4	8	DBG[7:0]	I	Debug Bus Port (Tied LOW for normal operations). LVCMOS, 3.3V, input, pull-down.

Group	Pin No.	No. of Pins	Pin Name	I/O	Description
Global: Serial Programming Interface	A8	1	SPRI_CLK	I/O	Serial Programming Interface (FPGA Configuration Loader). LVCMOS, 3.3V, bidirectional, 12mA, tristate.
	B10	1	SPRI_DATAOUT	I/O	Serial Programming Interface (FPGA Configuration Loader). LVCMOS, 3.3V, bidirectional, 12mA, tristate.
	C11	1	SPRI_CONFIG	I/O	Serial Programming Interface (FPGA Configuration Loader). LVCMOS, 3.3V, bidirectional, 12mA, tristate.
	A12	1	SPRI_DONE	I/O	Serial Programming Interface (FPGA Configuration Loader). LVCMOS, 3.3V, bidirectional, 12mA, tristate.
	B13	1	SPRI_XI_SWAP	I/O	Serial Programming Interface (FPGA Configuration Loader). LVCMOS, 3.3V, bidirectional, 12mA, tristate.
	B14	1	SPRI_STATUS	I/O	Serial Programming Interface (FPGA Configuration Loader). LVCMOS, 3.3V, bidirectional, 12mA, tristate.
PCI Express Link: PCIe x4 PHY interface	A1, A3, C2, D2, E3, F3, G2, H2, J2, K2, L3, M3, N2, P2, T1, T3	16	VSS_PCIE	G	PHY VSS.
	B1, C3, D3, N3, P3, R1	6	VDD_PCIE	P	PHY VDD. 1.2V (Core)
	G3	1	VDDAUX	P	PHY VDDAUX. 1.2V
	F1	1	VTT_AB	P	PCIe PHY transmit termination lanes A/B. Driven to voltage VTT. 1.5V See Table 3-6.
	M1	1	VTT_CD	P	PCIe PHY transmit termination lanes C/D. Driven to voltage VTT. 1.5V See Table 3-6.
PCI Express Link: PCIe Transmit [Output from the device]	N1, M2, E2, D1	4	PETn[3:0]	O	PCIe Transmit -Bus Lane A. CML
	P1, L2, F2, C1	4	PETp[3:0]	O	PCIe Transmit +Bus Lane A. CML

Group	Pin No.	No. of Pins	Pin Name	I/O	Description
PCI Express Link: PCIe Receive [Input to the device]	T2, J1, H1, A2	4	PERn[3:0]	I	PCIe Receive -Bus Lane A. CML **Note**: PERp[3:0] / PERn[3:0] each receiver lane can be connected using either the indicated polarity, or inverted polarity. Inverted polarity may be chosen in order to simplify the PCB layout by avoiding signal crossover and additional PCB vias. The GN4124 will automatically detect and compensate for polarity inversion during link training.
	R2, K1, G1, B2	4	PERp[3:0]	I	PCIe Receive +Bus Lane A. CML
Local Bus	P14, R16	2	LCLK, LCLKn	O	Local Bus Clock. SSTL, 1.8V, differential
	K6, L4, M4, M5	4	LCLK_MODE[3:0]	I	Selects the clock mode. LVCMOS, 3.3V, input, pull-down.
	P16	1	$\overline{\text{RSTOUT18}}$	O	Reset Output; 1.8V (Active LOW). CMOS, 1.8V, output
Local Bus: PCIe to Local [Inbound Data]	P9	1	P2L_RDY	I	Rx Buffer Full Flag. SSTL, 1.8V, input, with ODT.
	P5, R4, R5, R6, R9, R11, R12, R13, T5, T6, T7, T8, T9, T10, T11, T13	16	P2L_DATA[15:0]	O	Parallel Receive Data. SSTL, 1.8V, output
	R7	1	P2L_DFRAME	O	Receive Frame. SSTL, 1.8V, output
	P7	1	P2L_VALID	O	Receive Data Valid. SSTL, 1.8V, output
	P8, R8	2	P2L_CLKp, P2L_CLKn	O	Receiver Source Synchronous Clock. SSTL, 1.8V, output, differential

Group	Pin No.	No. of Pins	Pin Name	I/O	Description
Local Bus: Inbound Buffer Request/Status	P10, N9	2	P_WR_REQ[1:0]	O	PCIe Write Request. SSTL, 1.8V, output
	N11, N12	2	P_WR_RDY[1:0]	I	PCIe Write Ready. SSTL, 1.8V, input, with ODT.
	N6	1	RX_ERROR	I	Receive Error. SSTL, 1.8V, input, with ODT.
	P11, P12	2	VC_RDY[1:0]	O	Virtual Channel Ready Status. This provides a VC_RDY output to indicate the DL_UP[1] status of the Virtual Channel. This can be used to provide a synchronous reset to the external application in the event one of the Virtual Channels goes down e.g. hot reset initiated by PCIe host. SSTL, 1.8V, output
Local Bus: Local PCIe [Outbound Data]	B16, C16, E16, F16, J16, K16, L16, N16, C15, D15, E15, F15, J15, L15, M15, N15	16	L2P_DATA[15:0]	I	Parallel Transmit Data. SSTL, 1.8V, input, with ODT.
	H14	1	L2P_DFRAME	I	Transmit Data Frame. SSTL, 1.8V, input, with ODT.
	H16	1	L2P_VALID	I	Transmit Data Valid. SSTL, 1.8V, input, with ODT.
	G14	1	L2P_EDB	I	End-of-Packet Bad Flag. When a packet is considered bad and is terminated with EDB. SSTL, 1.8V, input, with ODT.
	G16, G15	2	L2P_CLKp, L2P_CLKn	I	Transmitter Source Synchronous Clock. SSTL, 1.8V, input, differential, with ODT.
Local Bus: Outbound Buffer Status	F14	1	L2P_RDY	O	Tx Buffer Full Flag. SSTL, 1.8V, output
	J14, K14	2	L_WR_RDY[1:0]	O	Local-to-PCIe Write. SSTL, 1.8V, output
	L14, M14	2	P_RD_D_RDY[1:0]	O	PCIe-to-Local Read Response Data Ready. SSTL, 1.8V, output
	N14	1	TX_ERROR	O	Transmit Error. SSTL, 1.8V, output

Group	Pin No.	No. of Pins	Pin Name	I/O	Description
Power	F5, K5	2	VDDW	P	3.3V
	R10	1	VREF	P	900mV reference voltage for SSTL I/O
	T14	1	PLL_AVDD	P	1.2V PLL supply voltage
	D5, D8, D13, D16, E10, E13, F6, F12, F13, G12, H4, H15, J13, K15, L5, L6, L10, L13, M6, M10, M16, N8, N10, P6, P13, P15, T4, T12	28	VDDC	P	1.2V core power
	E1, K4	2	VDDP	P	3.3V
	H11, H12, J11, J12, L8, L9, M8, M9	8	VCCO18	P	Power for 1.8V I/O
	E8, E9, F8, F9	4	VCCO33	P	Power for 3.3V I/O
Ground	N13	1	PLL_AVSS	G	PLL Ground. This pin is internally connected to VSS and, for noise isolation, should not be connected to VSS externally. Refer to the Gullwing RDK schematics and PCB layout for proper implementation.
	A16, B15, C4, C14, D4, E4, G4, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H13, J4, J5, J7, J8, J9, J10, K3, K7, K8, K9, K10, K11, K12, L1, L11, L12, M7, M11, M12, N5, P4, R3, R15, T16	43	VSS	G	Ground.
No Connect	B3, D10, D14, E14, F4, G13, J6, K13, L7, M13, N4, N7, R14, T15	14	NC	—	No Connect.

1. Data Link Layer indicates that a connection with the upstream devices has been established.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1: Absolute Maximum Ratings

Parameter	Value
Core Supply Voltage	-0.5V to +1.8 VDC
SSTL IO Supply Voltage	-0.5V to +2.5 V_{DC}
LVCMOS IO Supply Voltage	-0.5V to +4.6 V_{DC}
Input ESD Voltage (HBM)	2kV
Storage Temperature Range	-50°C < T_S < 125°C
Solder Reflow Temperature	260°C

3.2 Operating Conditions

Table 3-2: Operating Conditions

All electrical characteristics are valid over the range of these operating conditions, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Core Supply Voltage on pins VDDC, VDD_PCIE, VDDAUX, PLL_AVDD, PCIE_VDDA	V_{CORE}	–	1.14	1.2	1.26	V	±5%
SSTL IO Supply Voltage on pins VCCO18	V_{VCCO18}	–	1.71	1.8	1.89	V	±5%
LVCMOS IO and 3.3V Core Supply Voltage: pins VCCO33, VDDW, VDDP	V_{VCCO33}	–	3.0	3.3	3.6	V	±10%
Operating Temperature Range	T_A	Ambient	0	25	85	°C	

3.3 DC Electrical Characteristics

Table 3-3: DC Electrical Characteristics

Power and current limits listed have been derived from design and characteristics data.
They are not 100% tested in production.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Power Consumption	P_D	PCIe x4, LCLK=200MHz	–	650	950	mW	1
		PCIe x4, LCLK=100MHz	–	600	–	mW	2
		PCIe x1, LCLK=100MHz	–	475	–	mW	3
Total Core Supply Current on pins VDDC, VDD_PCIE, VDDAUX, PLL_AVDD, PCIE_VDDA	I_{CORE}	–	–	110[4]	– (See Note [5])	mA	–
SSTL IO Supply Current	I_{VCCO18}	–	–	340[6]	– (See Note 5)	mA	–
LVCMOS IO and 3.3V Core Supply Current: pins VCCO33, VDDW, VDDP	I_{VCCO33}	–	–	90[7]	– (See Note 5.)	mA	–

1. Data is based on an application circuit equivalent to that used on the GN4124 RDK board (Gullwing), typical operating conditions, PCIe negotiated to 4 lanes, default PCIe PHY settings, 200MHz local bus operation, and with concurrent data traffic at 75% bus utilization. Doesn't include power dissipated by components outside of the GN4124.
2. See Note 1. Typical operating conditions, 100MHz local bus operation.
3. See Note 1. Typical operating conditions, 100MHz local bus operation, PCIe negotiated to 1 lane.
4. This information is intended to guide power supply design. Data is based on an application circuit equivalent to that used on the GN4124 RDK board (Gullwing), typical operating conditions, 200MHz local bus operation, and with concurrent data traffic at 75% bus utilization.
5. Maximum supply current will vary greatly depending on the application circuit and device usage. A specific application's maximum current can be be predicted by measuring current under high temperature, high supply and full load conditions. To this resultant number, the following factors needed to be added:
   +25% for I_{CORE}
   +35% for I_{VCCO18}
   +25% for I_{VCCO33}
6. See Note 4. Based on use of 22-ohm serial termination and 51-ohm parallel termination in the application circuit.
7. See Note 4. Also includes current draw from an LDO used to power VTT_AB and VTT_CD.

Table 3-4: DC Electrical Characteristics for LVCMOS Buffers

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
High-level input voltage	V_{IH}	–	2	–	–	V	–
Low-level input voltage	VIL	–	–	–	0.8	V	–
Input leakage current	I_L	–	–	–	±5	μA	–
High-level output voltage	V_{OH}	IOH = -100 μA	2.8	–	–	V	–
Low-level output voltage	VOL	IOL = 100 μA	–	–	0.2	V	–

Table 3-5: DC Electrical Characteristics for SSTL Buffers

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
VREF input reference voltage	V_{REF}	–	833	900	969	mV	1
SSTL termination voltage	V_{TT}	–	V_{REF}-40	V_{REF}	V_{REF}+40	mV	2
High-level input voltage (DC)	V_{IH}	–	V_{REF}+125	–	V_{VCCO18}+ 300	mV	–
Low-level input voltage (DC)	V_{IL}	–	-300	–	V_{REF}-125	mV	–
High-level input voltage (AC)	V_{IH}	–	V_{REF}+250	–	–	mV	–
Low-level input voltage (AC)	V_{IL}	–	–	–	V_{REF}-250	mV	–

1. Typically the value of VREF is expected to be 50% * VDDQ of the transmitting device. Peak to peak AC noise on VREF may not exceed +/- 2% of VREF.
2. The termination voltage VTT should track the reference voltage VREF.

3.4 PCI Express Electrical Characteristics

3.4.1 PCI Express Transmitter Characteristics

Table 3-6: Transmitter Characteristics

Symbol	Description	Min	Typical	Max	Unit
Voltage Parameters					
$V_{TX\text{-}DIFF}$[1]	Output voltage compliance @ typical swing				
	$V_{TX\text{-}DIFFp}$ (peak-to-peak, single ended)	400	500	600	mV
	$V_{TX\text{-}DIFFpp}$ (peak-to-peak, differential)	800	1000	1200	mV
V_{TT}	Transmitter termination voltage	1.2	1.5	1.89	V
V_{OL}	Low-level output voltage	–	V_{TT} - 1.5 * $V_{TX\text{-}DIFFp}$	–	V

Symbol	Description	Min	Typical	Max	Unit
V_{OH}	High-level output voltage	–	V_{TT} - 0.5 * $V_{TX-DIFFp}$	–	V
$V_{TX-DC-CM}$	Transmit common-mode voltage	0	V_{TT} - $V_{TX-DIFFp}$	3.6	V
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle.	–	–	100	mV
$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	0	-3.35	-7.96	dB[2]
$V_{TX-IDLE-DIFFp}$	Electric Idle differential peak voltage	–	–	20	mV
$V_{TX-RCV-DETECT}$	Voltage change during Receive Detection	–	–	600	mV
$RL_{TX-DIFF}$	Transmitter Differential Return loss	10	–	–	dB
RL_{TX-CM}	Transmitter Common Mode Return loss	6	–	–	dB
Z_{OSE}	Single-ended output impedance	40	50	60	Ω
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
$T_{TX-RISE}$, $T_{TX-FALL}$	Rise / Fall time of TxP, TxN outputs	.125	–		UI[3]
Jitter Parameters					
UI	Unit Interval	399.88	400	400.12	ps[4]
$T_{TX-MAX-JITTER}$	Transmitter total jitter (peak-to-peak)	–	–	0.30[5]	UI
T_{TX-EYE}	Minimum TX Eye Width (1 - $T_{TX-MAX-JITTER}$)	0.70	–	–	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	–	–	0.15	UI
Timing Parameters					
$L_{TX-SKEW}$	Transmitter data skew between any 2 lanes	0	–	2UI + 200ps	ps
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an Electrical Idle ordered set	–	4	6	ns
T_{EIExit}	Time to exit Electrical Idle (L0s) state into L0	–	12	16	ns

1. Measured with Vtt = 1.2V, PHY_CONTROL register bits HIDRV='0', LODRV='0' and DTX="0000"(1x).
2. The de-emphasis ratio is determined through the DEQ bits of the PHY_CONTROL register inside the GN4124. Typical value is based on recommended setting of the PHY_CONTROL register.
3. As measured between 20% and 80% points.
4. UI does not account for SSC dictated variations.
5. Measured using PCI Express Compliance Pattern.

Figure 3-1: Typical Transition Signal Eye, De-emphasis Disabled, Default Drive Setting

The eye diagram is generated from SIGtest Version 2.1 available from the PCI Special Interest Group.

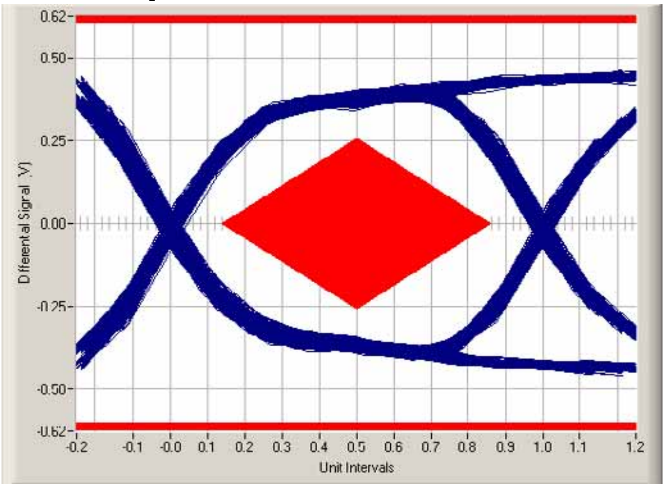
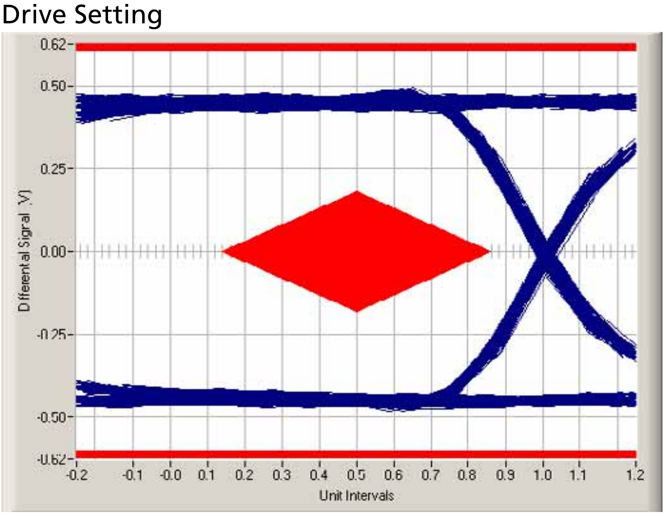


Figure 3-2: Typical Non-Transition Signal Eye, De-emphasis Disabled, Default Drive Setting



3.4.2 PCI Express Receiver Characteristics

Table 3-7: PCI Express Receiver Characteristics

Symbol	Description	Min	Typical	Max	Unit
Voltage Parameters					
$V_{RX\text{-}DIFFp\text{-}p}$	Differential input voltage (peak-to-peak)	170	–	1200	mV
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	Differential input threshold voltage (peak-to-peak) to assert TxIdleDetect output	65	–	235	mV
$V_{RX\text{-}CM\text{-}AC}$	Receiver common-mode voltage for AC-coupling	–	0	150	mV
$T_{RX\text{-}RISE}$, $T_{RX\text{-}FALL}$	Rise time / Fall time of RxP, RxN inputs	–	–	160	ps
$Z_{RX\text{-}DIFF\text{-}DC}$	Differential input impedance (DC)	80	100	120	Ω
$Z_{RX\text{-}COM\text{-}DC}$	Single-ended input impedance	40	50	60	Ω
$Z_{RX\text{-}COM\text{-}INITIAL\text{-}DC}$	Initial input common mode impedance (DC)	5	50	60	Ω
$Z_{RX\text{-}COM\text{-}HIGH\text{-}IMP\text{-}DC}$	Powered down input common mode impedance (DC)	200k	–	–	Ω
$RL_{RX\text{-}DIFF}$	Receiver Differential Return Loss[1]	10	–	–	dB
$R_{LRX\text{-}CM}$	Receiver Common Mode Return Loss	6	–	–	dB
Jitter Parameters					
$T_{RX\text{-}MAX\text{-}JITTER}$	Receiver maximum total jitter tolerance	0.65	–	–	UI
$T_{RX\text{-}EYE}$	Minimum Receiver Eye Width	0.35	–	–	UI
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between jitter median and max deviation from median	–	–	0.325	UI
Timing Parameters					
$T_{RX\text{-}SKEW}$	Maximum skew across all 4 lanes of the link	–	–	20	ns
T_{BDDly}	Beacon-Activity on channel to detection of Beacon[2]	33	–	100	ns
$T_{RX\text{-}IDLE\_ENTER}$	Delay from detection of Electrical Idle condition on the channel to assertion of TxIdleDetect output	–	10	20	ns
$T_{RX\text{-}IDLE\_EXIT}$	Delay from detection of L0s to L0 transition to de-assertion of TxIdleDetect output	–	5	10	ns

1. Over a frequency range of 50MHz to 1.25GHz.
2. This is a function of beacon frequency.

Table 3-8: Reference Clock (PECLKINn) Requirements

Symbol	Description	Min	Typical	Max	Unit
V_{IL-RC}	Low-level CML/CMOS input voltage	0	–	V_{DD} - 0.5	V
V_{IH-RC}	High-level CML/CMOS input voltage	–	V_{DD}		V
F_{RefClk}	Clock frequency range	99.5	100	100.03	MHz[1]
$D.C._{RefClk}$	Duty cycle	40	50	60	%
$T_{Skew-Ref}$	Skew between PECLKINp/PECLKINn inputs	–	–	0.05	RCUI
TCCJITTER	Cycle to Cycle jitter	–	–	150	ps
T_{RRef}, T_{FRef}	Rise/Fall time of PECLKINp/PECLKINn inputs	–	0.2	0.25	RCUI
PPM	PPM difference between reference clocks on different ends of a link	-300	–	+300	PPM

1. Includes 0 to -0.5% spread spectrum clock range.

3.4.3 Local Bus Timing

Figure 3-3 illustrates the timing relationships of the three local bus clock domains.

Figure 3-3: Local Bus Timing

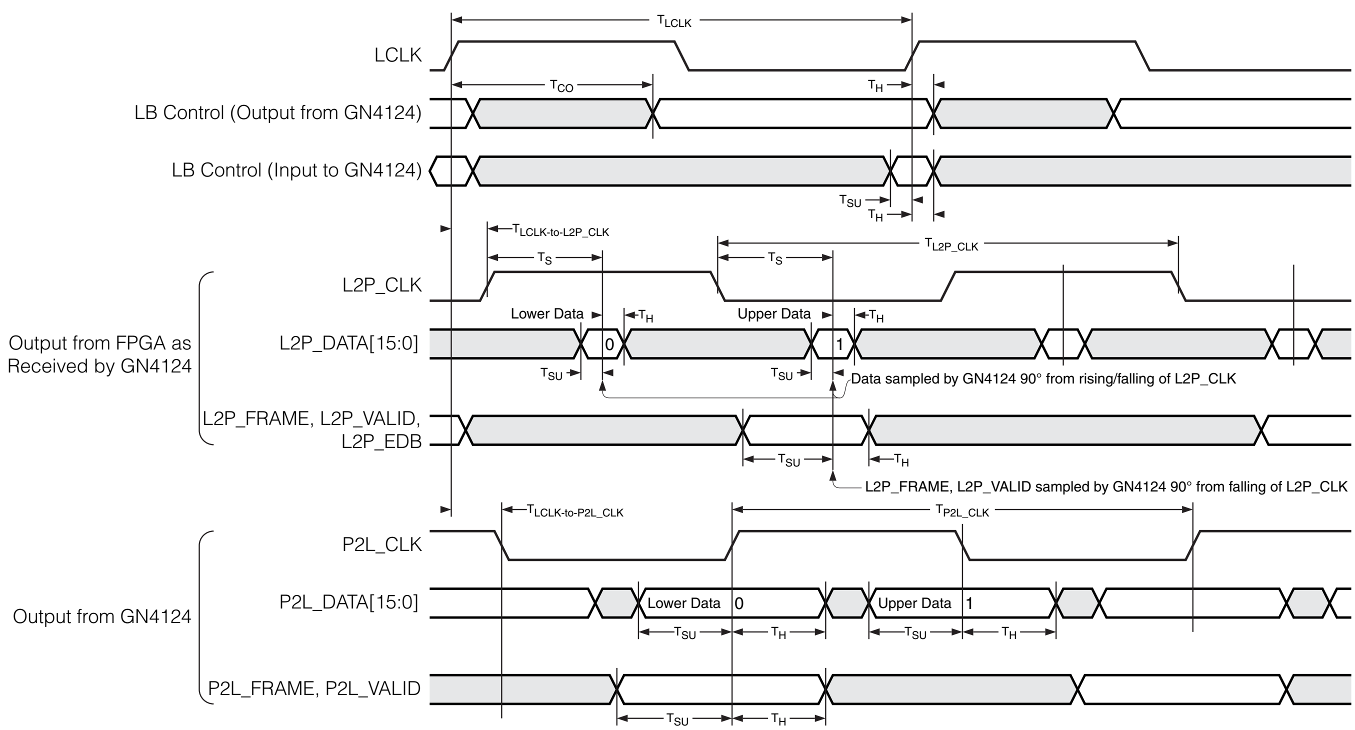


Table 3-9: Local Bus Signal Timing for Single Data Rate SSTL Over Specified Operating Conditions (TARGET SPECIFICATION)

Symbol	Description	Min	Max	Units
T_{LCLK}	LCLK Cycle Time	5	10	ns
T_{CO}	Clock to output delay for local bus control signals	0.7	5.0	ns[1]
T_{SU}	Required input set-up time to LCLK for local bus control inputs	–	1.0[2]	ns
T_{H}	Required input hold time from LCLK for local bus control inputs	–	0.7	ns

1. Local bus control signals received by an attached FPGA should be treated as asynchronous.
2. Local bus control inputs are synchronized by the GN4124. Failure to meet setup time will simply delay the cycle in which the change is recognized.

Table 3-10: Local Bus Timing for Source Synchronous SSTL Input Signals Over Specified Operating Conditions (TARGET SPECIFICATION)

Input signals include L2P_CLK, L2P_DATA(15:0), L2P_DFRAME, and L2P_VALID.

Symbol	Description	Min	Max	Units
T_{L2P_CLK}	L2P_CLK Cycle Time or Unit Interval (UI)	T_{LCLK}		ns
IJT_{L2P_CLK}	L2P_CLK input jitter tolerance (cycle-to-cycle)	–	100	ps
$T_{L2P\_CLK\_LOCK}$	L2P_CLK input lock time	–	1380	cycles
$T_{LCLK\text{-}to\text{-}L2P\_CLK}$	Delay from LCLK to L2P_CLK	0	T_{LCLK}	ns
T_S	Sample point for data relative to L2P_CLK (rising and falling)	L2P_CLK +90°		
T_{SU} (L2P_DATA)	Required input set-up time to L2P_CLK+T_S (rising and falling)	–	400	ps
T_H (L2P_DATA)	Required input hold time from L2P_CLK+T_S (rising and falling)	–	400	ps

Table 3-11: Local Bus Timing for Source Synchronous SSTL Output Signals Over Specified Operating Conditions (TARGET SPECIFICATION)

Output signals include P2L_CLK, P2L_DATA(15:0), P2L_DFRAME, and P2L_VALID.

Symbol	Description	Min	Max	Units
T_{P2L_CLK}	P2L_CLK Cycle Time or Unit Interval (UI)	T_{LCLK}		ns
$T_{LCLK\text{-}to\text{-}P2L\_CLK}$	Delay from LCLK to P2L_CLK	T_{LCLK}/2 - 1.2	T_{LCLK}/2 +1.2	ns
T_{SU} (P2L_DATA)	Output set-up time to P2L_CLK (rising and falling)	1200	–	ps
T_H (P2L_DATA)	Output hold time from P2L_CLK (rising and falling)	400	–	ps
T_{SKEW}	Skew between P2L_DATA lanes	–	300	ps

3.4.4 Local Clocks' Pins Settings

There are 3 local clocks used by the GN4124 and attached FPGA. They are:

- LCLK/LCLKn: The primary clock generated by the GN4124 and driven to the FPGA in the form of a differential SSTL output.
- P2L_CLKp/n: The source synchronous clock used by the GN4124 to communicate data to the FPGA. It is derived from the same source as LCLK/LCLKn.
- L2P_CLKp/n: The source synchronous clock generated by the attached FPFA to communicate data to the GN4124. It is derived by the FPGA from LCLK/LCLKn.

The local clock LCLK/LCLKn may be derived from either the PCI Express clock or a low frequency crystal oscillator. The options are described in Table 3-12.

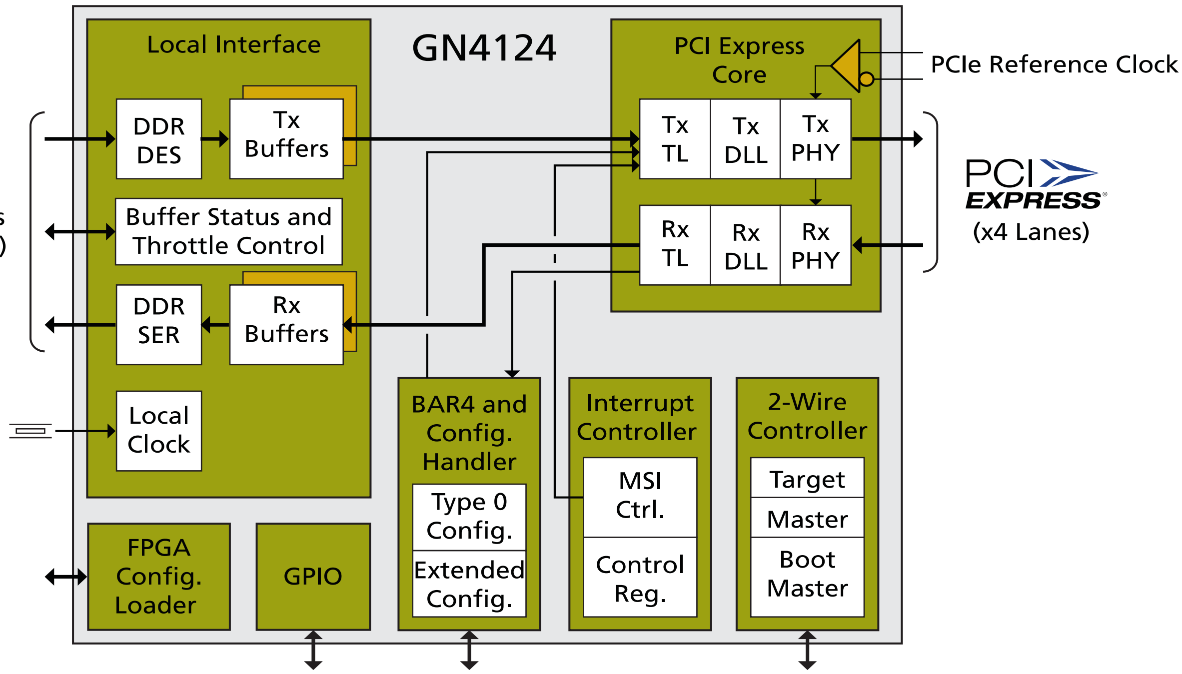
Table 3-12: GN4124 Clocks' Pins Settings

Signal	Description
LCLK_MODE[2]	Controls PLL Bypass. '0' = LCLK is generated by the PLL, which is configurable. This is recommended for low and predictable LCLK clock jitter. '1' = LCLK is driven by 125MHz clock generated from the PCI Express link.
LCLK_MODE[1]	Resets the PLL test clock divider. '0' = Resets the PLL test clock divider, so that PLL_TEST_OUT = '0'. '1' = PLL_TEST_OUT pin outputs a clock with a frequency of the PLL clock divided by 1024. This is used for test purposes.
LCLK_MODE[0]	Selects the source for the LCLK PLL. '0' = LB_REF_CLK oscillator (20-40MHz). This is recommended for low and predictable LCLK clock jitter. '1' = 125MHz clock generated from the PCI Express link.

4. Overview

A block diagram of the GN4124 is depicted in Figure 4-1.

Figure 4-1: GN4124 Block Diagram



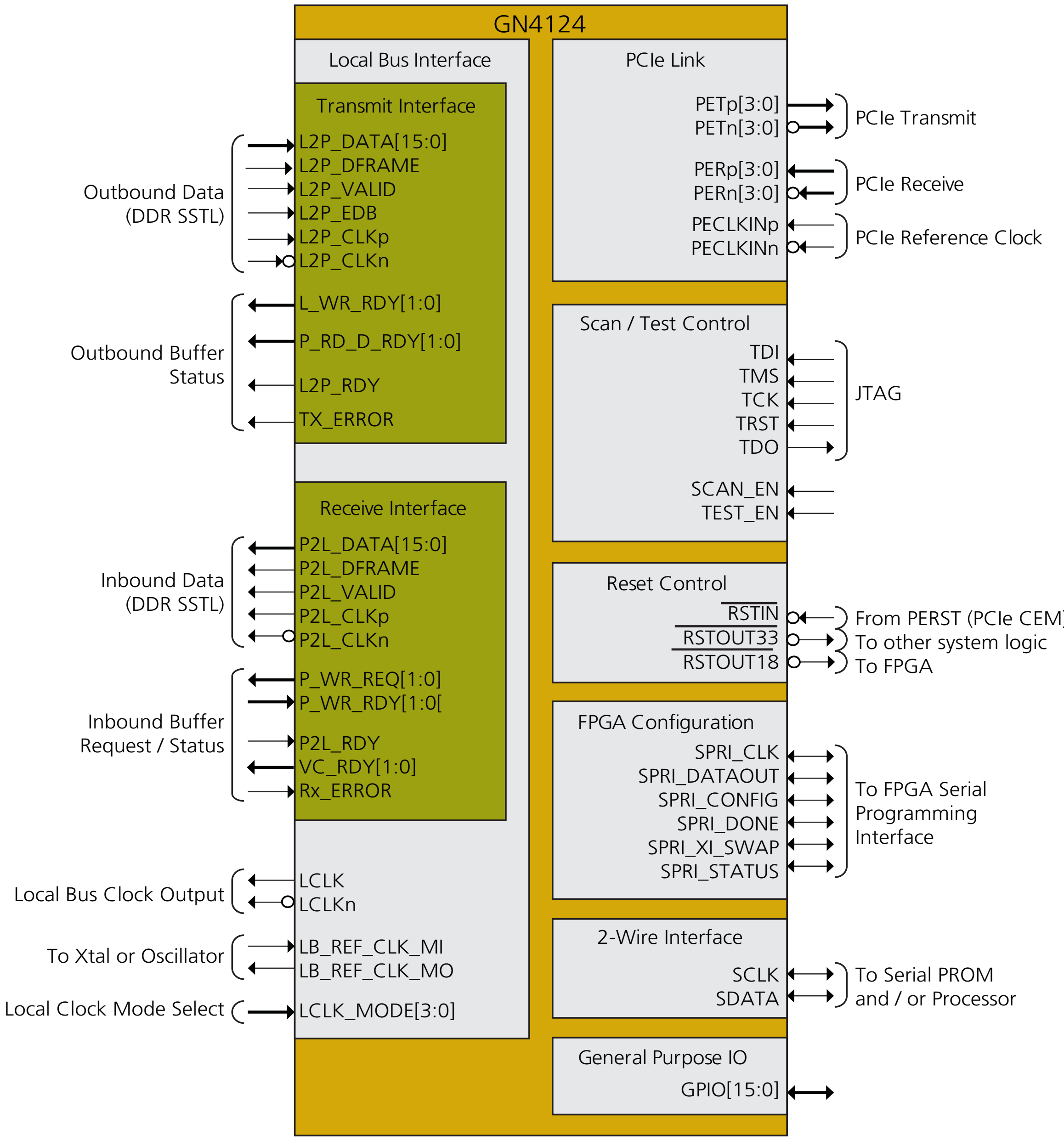
Each of the internal blocks is described in detail in the GN412x PCI Express Family Reference Manual. They are:

- The PCI Express link is described in PCI Express Link section of the GN412x PCI Express Family Reference Manual. This includes a description of the PCI Express related configuration registers.
- The Local bus is described in Local Bus Interface section of the GN412x PCI Express Family Reference Manual.
- The interrupt controller is described in Interrupt Control Unit section of the GN412x PCI Express Family Reference Manual.
- The boot master mode of the 2-wire controller is described in Initialization from a 2-Wire EEPROM section of the GN412x PCI Express Family Reference Manual.
- General purpose master/target mode of the 2-wire controller is described in 2-Wire Interface section of the GN412x PCI Express Family Reference Manual.
- General purpose IO are described in General Purpose IO Block section of the GN412x PCI Express Family Reference Manual.
- Details of all the internal registers and their respective register bit fields are described in Internal Registers section of the GN412x PCI Express Family Reference Manual.

4.1 GN4124 Signals

Figure 4-2 depicts the signals of the GN4124 laid out in their logical groupings.

Figure 4-2: GN4124 Signal Groups Diagram

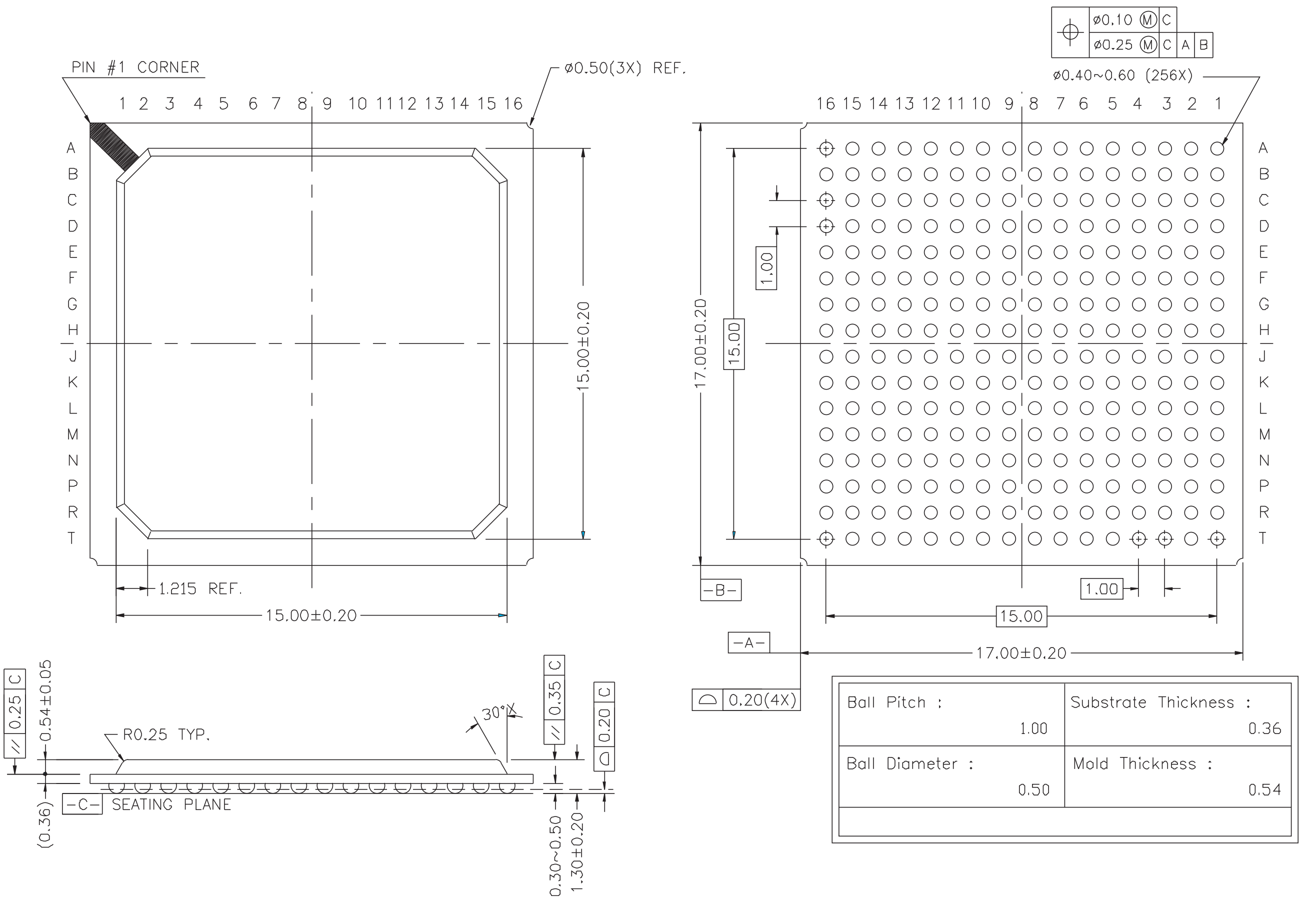


5. Package & Ordering Information

5.1 Package Dimensions

The GN4124 is packaged in a 256 ball BGA as illustrated in Figure 5-1.

Figure 5-1: GN4124 Package Dimensions



5.2 Packaging Data

Table 5-1: Packaging Data

Parameter	Value
Package Type	17mm x 17mm 256-ball BGA
Package Drawing Reference	
Moisture Sensitivity Level	3
Junction to Air Thermal Resistance, $\theta_{j\text{-}a}$ (at zero airflow)	27°C/W
Junction to Air Thermal Resistance, $\theta_{j\text{-}a}$ (at 1m/s airflow)	24°C/W
Junction to Air Thermal Resistance, $\theta_{j\text{-}a}$ (at 2m/s airflow)	22°C/W
Junction to Case Thermal Resistance, $\theta_{j\text{-}c}$	5.5°C/W
Psi	11.0°C/W
Pb-free and RoHS compliant	Yes

5.3 Ordering Information

Table 5-2: Packaging Data

Part Number	Package	Temperature Range
GN4124-CBE3	256-BGA	0°C to 85°C

Index

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

GENNUM CORPORATE HEADQUARTERS
4281 Harvester Road, Burlington, Ontario L7L 5M4 Canada
Phone: +1 (905) 632-2996
Fax: +1 (905) 632-2055
E-mail: corporate@gennum.com
www.gennum.com

OTTAWA
232 Herzberg Road, Suite 101
Kanata, Ontario K2K 2A1
Canada
Phone: +1 (613) 270-0458
Fax: +1 (613) 270-0429

CALGARY
3553 - 31st St. N.W., Suite 210
Calgary, Alberta T2L 2K7
Canada
Phone: +1 (403) 284-2672

UNITED KINGDOM
North Building, Walden Court
Parsonage Lane,
Bishop’s Stortford Hertfordshire, CM23 5DB
United Kingdom
Phone: +44 1279 714170
Fax: +44 1279 714171

INDIA
#208(A), Nirmala Plaza,
Airport Road, Forest Park Square
Bhubaneswar 751009
India
Phone: +91 (674) 653-4815
Fax: +91 (674) 259-5733

SNOWBUSH IP - A DIVISION OF GENNUM
439 University Ave. Suite 1700
Toronto, Ontario M5G 1Y8
Canada
Phone: +1 (416) 925-5643
Fax: +1 (416) 925-0581
E-mail: sales@snowbush.com
Web Site: http://www.snowbush.com

MEXICO
288-A Paseo de Maravillas
Jesus Ma., Aguascalientes
Mexico 20900
Phone: +1 (416) 848-0328

JAPAN KK
Shinjuku Green Tower Building 27F
6-14-1, Nishi Shinjuku
Shinjuku-ku, Tokyo, 160-0023
Japan
Phone: +81 (03) 3349-5501
Fax: +81 (03) 3349-5505
E-mail: gennum-japan@gennum.com
Web Site: http://www.gennum.co.jp

TAIWAN
6F-4, No.51, Sec.2, Keelung Rd.
Sinyi District, Taipei City 11502
Taiwan R.O.C.
Phone: (886) 2-8732-8879
Fax: (886) 2-8732-8870
E-mail: gennum-taiwan@gennum.com

GERMANY
Hainbuchenstraße 2
80935 Muenchen (Munich), Germany
Phone: +49-89-35831696
Fax: +49-89-35804653
E-mail: gennum-germany@gennum.com

NORTH AMERICA WESTERN REGION
Bayshore Plaza
2107 N 1st Street, Suite #300
San Jose, CA 95131
United States
Phone: +1 (408) 392-9454
Fax: +1 (408) 392-9427
E-mail: naw_sales@gennum.com

NORTH AMERICA EASTERN REGION
4281 Harvester Road
Burlington, Ontario L7L 5M4
Canada
Phone: +1 (905) 632-2996
Fax: +1 (905) 632-2055
E-mail: nae_sales@gennum.com

KOREA
8F Jinnex Lakeview Bldg.
65-2, Bangidong, Songpagu
Seoul, Korea 138-828
Phone: +82-2-414-2991
Fax: +82-2-414-2998
E-mail: gennum-korea@gennum.com

SEMTECH

GENNUM PRODUCTS

GN4124/GN4121

Reliability Qualification Report

Revision History

Version	ECR/ECO	Date	Modifications / Changes
0	151544	Mar. 2009	New document
1	151730	Apr. 2009	HTOL 2000hrs data added and GN4121 included as qualified
2	ECO-018675	Mar. 2014	Updated formatting, minor corrections, additional qualification data to support PCN for bond wire change

Contents

1 Device Specifics

1.1 Manufacturing Summary

Table 1. Manufacturing Summary

Gennum Device Codes	GN4124/GN4121
Silicon Fab Technology	UMC 0.13um
Assembly House	ASE-K
Package Type	17mm x 17mm LBGA

1.2 Product Information

The GN4124 is a four lane PCI Express to local bus bridge that is designed to work as a companion for FPGA devices to provide a complete bridging solution for general applications. In addition to a 4-lane PCI Express compliant PHY. It provides pin efficient local bus interface for easy attachment to popular low-cost FPGA devices (Uses SSTL I/O for high-speed data transfer). “Live” on power up enables auto detection without FPGA activity. FPGA bitstream loader allows easy configuration of the attached FPGA through PCIe.

The GN4121 is a single lane PCI Express to local bus bridge that is designed to work as a companion for FPGA devices to provide a complete bridging solution for general applications. In addition to a PCI Express compliant PHY interface, the GN4121 contains the link and transaction layers, and an applications interface that is ideally suited to FPGA interfacing using a small number of pins.

1.3 Process Qualification

GN4124/GN4121 are manufactured in UMC 0.13um Logic Process Technology. The UMC qualification report is accepted In Agile id# GENDOC-036661.

1.4 Product Qualification Approach

GN4124 four lane PCI Express was chosen as the main test vehicle for qualification. GN4121 is considered a subset of GN4124 using the same back end and fab process, but with only a single lane PCI Express bus. GN4121 Reliability Qualification has been bridged to GN4124 due to its similarities in architecture and design.

Package reliability stress experiments have been bridged to 352 LBGA (35x35mm body size, Au wire) ASE package qualification report which covers the GN4124 package envelope (17x17mm LBGA package). The 35x35mm 352 LBGA ASE-K Package Qualification Report is accepted in Agile ID# GENDOC-047723.

PCN-000163 was introducted with a change to copper wire from gold wire, additional reliability stress experiments have been performed in a 256 LBGA (17x17mm) GN4124 device as the test vehicle. The ASE-K Cu wire Package Qualificaiton Report is accepted in Agile ID# PRODDOC004748

The Qualification Report has been reviewed and approved by design, product engineering, and reliability engineering.

2 Reliability Qualification Stresses

2.1 Environmental Tests

Table 2. Environmental Tests

Stress	Conditions	Duration	Qualification Vehicle	Sample Size	Result
High Temperature Operating Life	JESD22-A108 $T_j \geq 125^oC$, $V_{cc} \geq V_{ccmax}$	2000 hrs	GN4124	80	Pass
Temperature Cycling	JESD22-A104 MSL Preconditioning, -55°C to +125°C (Condition B)	1000 cycles	Bridged to 352 LBGA Package Qual	25 each from 3 lots	Pass
HAST (unbiased)	JESD22-A118 MSL Preconditioning, 130°C/85% RH	100 hours	Bridged to 256 PBGA Test Vehicle	77	Pass
Moisture Sensitivity Level	J-STD-020 MSL3, 30°C/60%	192hrs	Bridged to 352 LBGA Package Qual	75	Pass
PCT	JESD22-A102 121°C/100% RH 2ATM	96hrs	Bridged to 352 LBGA Package Qual	22	Pass
Temperature Cycling	JESD22-A104 MSL Preconditioning, -55°C to +125°C (Condition B)	1000 cycles	GN4124 (Cu wire)	77	Pass
HAST (unbiased)	JESD22-A118 MSL Preconditioning, 130°C/85% RH	100 hours	GN4124 (Cu wire)	77	Pass
Moisture Sensitivity Level	J-STD-020 MSL3, 30°C/60%	192hrs	GN4124 (Cu wire)	77	Pass

2.2 Electrostatic Discharge and Latch Up Tests

Table 3. Electrostatic Discharge and Latch Up Tests

Stress	Conditions	Qualification Vehicle	Stress Level	Sample Size	Results
Human Body Model ESD	JESD22-A114	GN4124	1KV, 2kV	6	Pass
Machine Model ESD	JESD22-A115	GN4124	100V, 200 V	6	Pass
Charged Device Model ESD	JESD22-C101	GN4124	500V, 700V	6	Pass
Latch Up	JESD78 1.5 x Vcc; +/- 100 mA Level II, Class A	GN4124	25°C	6	Pass
			85°C	6	

3 Conclusion

Process qualification reports demonstrate that the processes used in the manufacture of the GS3490 are in volume production and are fully qualified by the suppliers and Semtech Corporation – Gennum Products Group. Semtech Corporation considers these process and libraries acceptable for use in the design and manufacture of Semtech products.

The GN4124 and GN4121 passed reliability tests. No performance degradation was observed during the evaluation. These products are considered suitable for production.