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Comprehensively Understand and Analyze Switching Regulator Noise

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Abstract

This article will introduce several different types of inherent switching regulator noise: switching ripple, wideband noise, and high frequency spike. The PSRRs of switching regulators as they relate to input noise suppression will also be discussed and analyzed. A comprehensive understanding of switching regulator noise is important when designing a low noise switching regulator in order to remove post-LDO regualtors to improve power converter efficiency, save solution size, and lower design cost.

Introduction

Generally, traditional switching regulators were considered very noisy on output voltage compared to low dropout (LDO) regulator output; however, LDO voltage caused significant extra thermal issues and made the power design more complicated. Comprehensive recognition of switching regulator noise is necessary and can help when designing a low noise switching solution for the purpose of producing low noise performance at the same level as LDO regulators. A buck regulator with current-mode control was the analysis and evaluation objective since it was the most commonly adopted in application. Signal analysis was the primary method used to understand switching ripple noise, the present wideband noise characteristic, and where it comes from, and high frequency spike noise due to switching. The switching regulator PSRR (power supply rejection ratio) will be discussed, as well as the signal analysis method, which is important to input noise suppression.

Switching Ripple Noise

This section presents the buck converter output ripple calculation formula in relation to fundamental and harmonic theory.

According to switching regulator topology and basic operation, the ripple is always the majority noise in a switching regulator, as the peak-to-peak voltage amplitude is generally several mV to tens of mV. It should be considered a periodic and predictable signal. It can be recognized and measured easily through oscillation scope in time domain or Fourier decomposition in frequency domain if it operates on a fixed switching frequency.

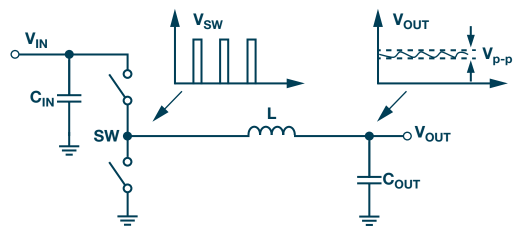

Figure 1. Buck regulator topology.

Figure 1 is a typical buck regulator. Since the two switches turn on and off alternately, the SW node voltage, V_{SW}, is an ideal square wave which relays to the duty cycle and input voltage, the V_{SW} can be expressed by the equations below,

$$V_{SW}(j\omega)=V_{IN}\sum_{-\infty}^{\infty}\frac{2\sin(k\times\pi\times D)}{k}\times\delta(\omega\text{-}k\times\omega_0)$$

$$V_{SW}(t)=V_{IN}\sum_{-\infty}^{\infty}\frac{\sin(k\times\pi\times D)}{k\times\pi}\times e^{j\omega_0\times k\times t}\qquad k=0,\pm1,\pm2\ldots$$

Where:

V_{IN} is input voltage. D is duty cycle which is equal to V_{OUT}/V_{IN} for buck regulator.

The V_{SW} fundamental and harmonics component only depends on duty cycle when V_{IN} is determined. Figure 2 shows the V_{SW} fundamental and harmonic amplitudes in relation to the duty cycle. The fundamental dominates the ripple amplitude when the duty cycle is close to half.

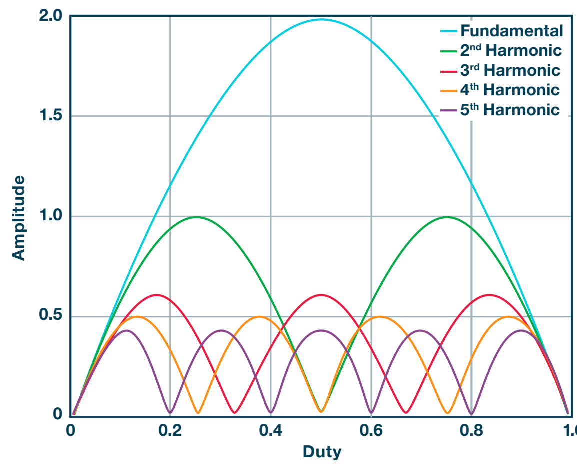

Figure 2. Buck regulator V_{SW} amplitude vs. duty.

The buck regulator output LC stage transfer function is as follows:

$$T_{LC}(j\omega)=\frac{ESR+j\omega\times ESL+\dfrac{1}{j\omega\times C_{OUT}}}{ESR+j\omega\times ESL+\dfrac{1}{j\omega\times C_{OUT}}+\dfrac{\dfrac{1}{j\omega\times C_L}(\mathrm{DCR}+j\omega\times L)}{\dfrac{1}{j\omega\times C_L}+\mathrm{DCR}+j\omega\times L}}$$

Where L is the output inductor value, DCR is the inductor resistor value, and C_L is the inductor parallel capacity value.

C_{OUT} is output capacity value. ESL is capacity series inductance. ESR is capacity series resistor value.

So the V_{OUT} can be expressed as below,

$$V_{OUT}(j\omega)=V_{SW}(j\omega)\times T_{LC}(j\omega)$$

To simplify the calculation, we assume 20 dB per decade for the output LC stage, then the V_{OUT} ripple fundamental and harmonic amplitudes in relation to the duty cycle, which are shown in Figure 3. The third, or odd, harmonic will be higher than an even harmonic when the duty cycle is close to half. Higher harmonics will have lower amplitude due to LC suppression and quite small proportions in comparison to the total ripple amplitude. Again, the fundamental amplitude is the majority component in the switching regulator output ripple.

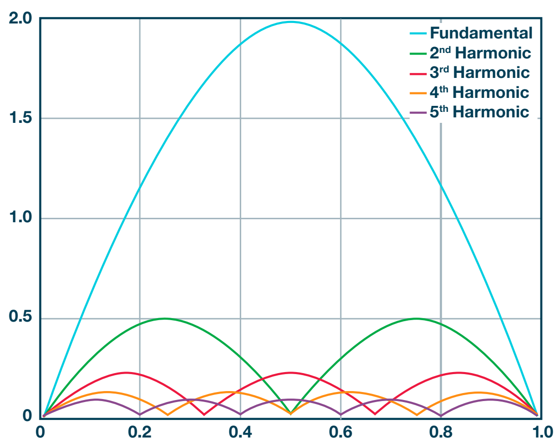

Figure 3. Buck regulator V_{OUT} ripple amplitude vs. duty.

For the buck regulator, the fundamental amplitude will relate to input voltage, duty cycle, switching frequency, and LC stage; however, all of these parameters will impact the application requirements like efficiency and solution size. To further reduce ripple, an additional post filter is recommended.

Wideband Noise

The wideband noise in a switching regulator is a random amplitude noise on the output voltage. It can be represented by noise density in V/√Hz over frequency, or V rms, which is integral to the density within frequency span. Due to silicon processes and reference filter design limitations, the wideband noise is mainly located in the 10 Hz to 1 MHz frequency range for switching regulators, which can be quite difficult to reduce via additional filters in low frequency ranges.

The typical buck regulator wideband noise peak-to-peak amplitude voltage is approximately 100 µV to 1000 µV, which is much less than switching ripple noise. If you use an additional filter to reduce switching ripple noise, then the wideband noise may become the primary noise in switching regulator output voltage. Figure 4 illustrates that the primary source of buck regulator output noise is a switching ripple when there is no additional filter. Figure 5 shows that the primary source of output noise when using an additional filter is wideband noise.

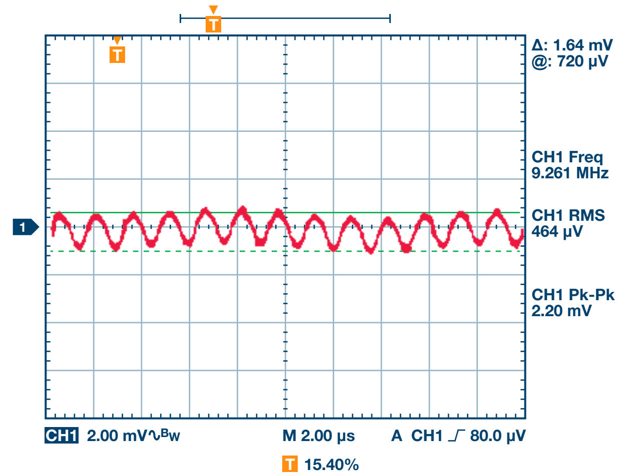

Figure 4. V_{OUT} without an additional filter.

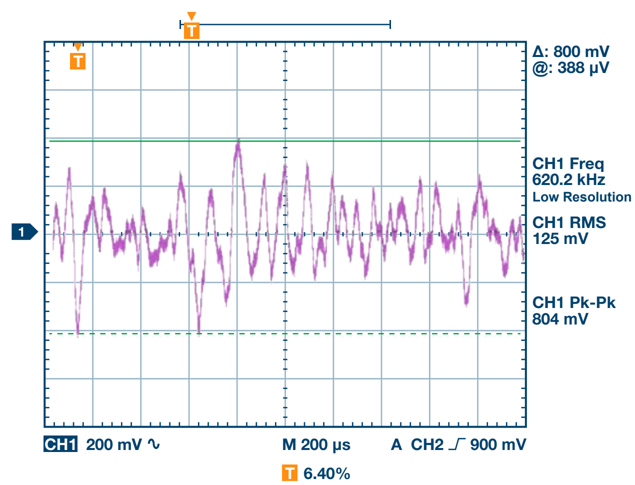

Figure 5. V_{OUT} with an additional filter (using 1000× pre-amp to measure).

To recognize and analyze switching regulator output wideband noise, it is necessary to have regulator control scheme and block noise information. For example, Figure 6 is a typical current-mode buck regulator control scheme and block noise source injection.

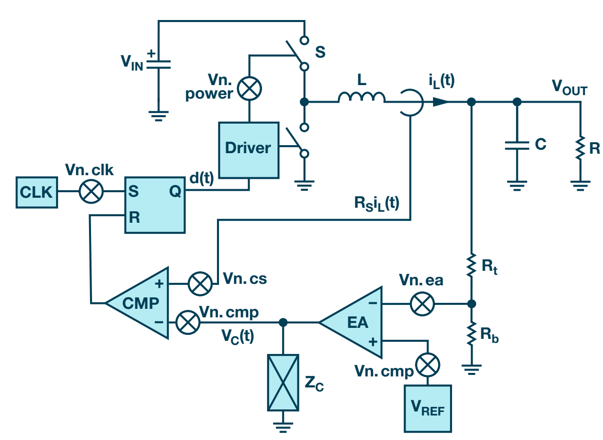

Figure 6. Typical current mode buck regulator control scheme.

With acquired control loop transfer function and block noise characterization, there are two separate kinds of noise: loop input noise and inside loop noise. The loop input noise would transfer to the output within the control loop bandwidth, while noise is attenuated outside of the loop bandwidth. It is critical to design a low noise EA and reference for a switching regulator, as the unit feedback gain will keep the noise level, not increase it with the output voltage level. The biggest challenge is in digging out the biggest noise source within the whole system and reducing it in the circuit design. The ADP5014 is optimized for low noise technology with a current mode control scheme and one simple LC external filter, achieving less than 20 µV rms noise performance over the 10 Hz to 1 MHz frequency span. The ADP5014 output noise performance show as Figure 7.

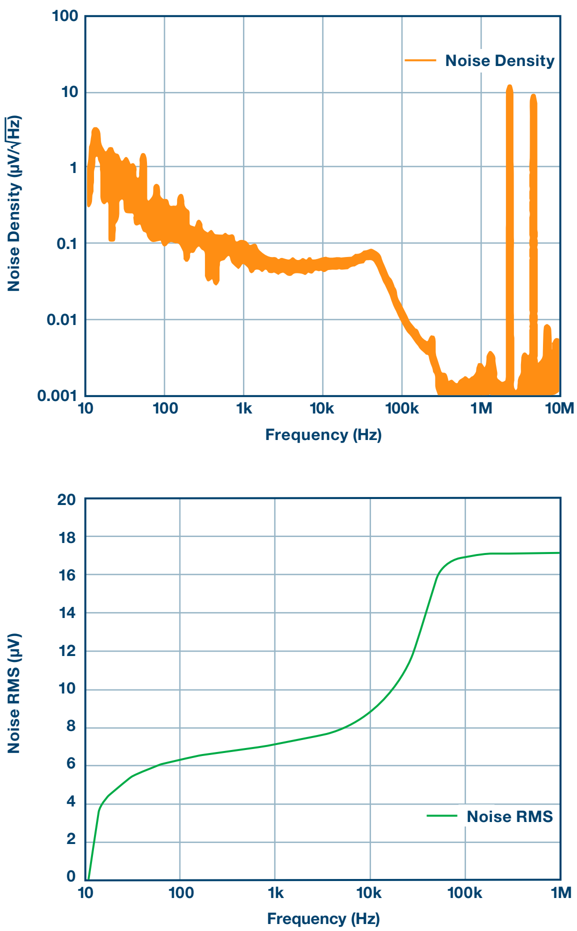

Figure 7. ADP5014 output noise performance with an additional LC filter.

High Frequency Spike and Ringing

The third type of noise is high frequency spike and ringing noise as the output voltage is generated by the switcher turn-on or turn-off transient. Consider parasitic inductor and capacity in silicon circuits and PCB trace; fast current transient will cause very high frequency voltage spike and ringing at the SW node for a buck regulator. The spike and ringing noise will increase with higher current load. Figure 8 shows how the spike takes shape for buck regulators. Depending on the switcher turn-on/-off slew rate, the highest spike and ringing frequency would be within the 20 MHz to 300 MHz range, so the output LC filter may not be very effective at suppression due to its parasitic inductor and capacitor. Compared to all of the above talking about conductive path, the worst is radiation noise from the SW and V_{IN} nodes, which will impact the output voltage and other analog circuits due to its very high frequency.

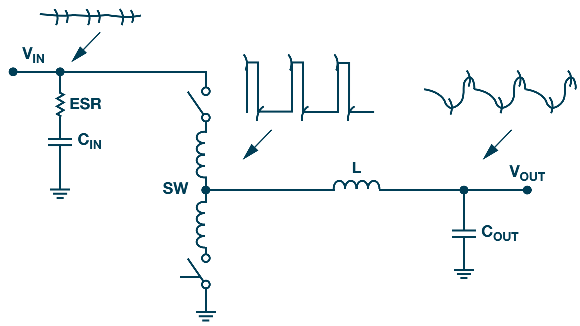

Figure 8. Buck regulator high frequency spike and ringing noise.

To reduce the high frequency spike and ringing noise, effective implementation of both application and silicon design is recommended. First, use an additional LC filter or bead on point of load. Usually this will make the spike noise on output much smaller than ripple noise, but this decision adds higher frequency components. Second, shield or keep away noise sources from the SW and input nodes from the output side and sensitive analog circuit, and shield the output inductor. Careful layout design and placement will be important. Third, optimize the switching regulator turn-on/-off slew rate and minimize the switcher's parasitic inductance and resistance to effectively reduce SW node noise. The ADI Silent Switcher® technology also helps reduce V_{IN} node noise via silicon design.

Switching Regulator PSRR

PSRR presents the switching regulator's suppression capability from the input power supply noise to the output. This section analyzes the buck regulator PSRR performance at low frequency range. The very high frequency noise mostly impacts the output voltage through the radiation path instead of the conductive path as previously discussed.

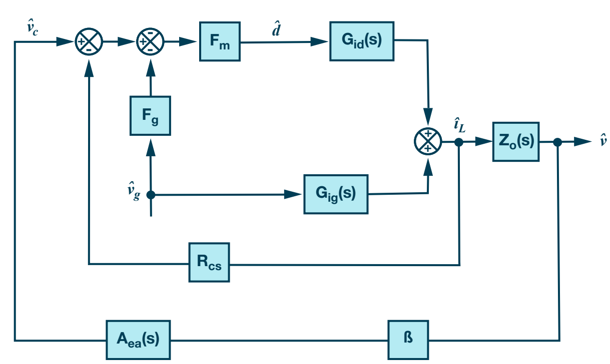

Figure 9. Current-mode buck small signal diagram from input voltage to output.

According to the buck small signal diagram in Figure 9, the buck PSRR can be express by

$$G_{go}(s) = \frac{(G_{ig}(s) - F_m \times F_g \times G_{id}(s)) \times Z_o(s)}{(1 + F_m \times G_{id} \times R_{cs})(1 + T_v(s))}$$

Where:

$$G_{ig}(s) = \frac{D(1 + sRC)}{R(1 + sL/R + s^2LC)} \qquad G_{id}(s) = \frac{V_{IN}(1 + sRC)}{R(1 + sL/R + s^2LC)}$$

F_m is slope gain

F_g is input voltage to control

R_{cs} is current sense gain

$Z_o(s)$ is output cap and load

$T_v(s)$ is loop transfer function.

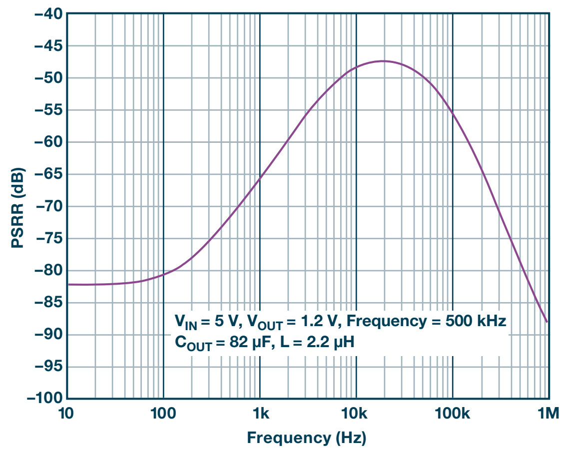

Figure 10. PSRR calculation results by using buck small signal mode.

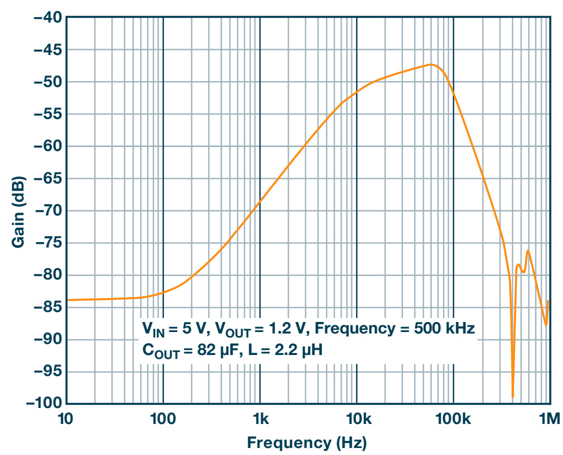

Figure 11. PSRR simulation by SIMPLIS mode.

Compare the signal mode calculation with simulation results. The small signal mode is effective and matches the simulation results.

The switching regulator's PSRR performance is dependent on the loop gain performance during low frequency range. Switching regulators have inherent LC filters that can suppress input noise in the middle frequency range (100 Hz to 10 MHz). That would be much better than LDO PSRR in those ranges. So, the switching regulator has perfect PSRR performance due to its high loop gain in low frequency, and inherent LC filters affect the middle frequency range.

Conclusion

More and more analog circuits, such as ADCs/DACs, clocks, and PLLs, require clean power supplies with high current. Each device will have different requirements and specifications for power supply noise in different frequency ranges. It is necessary to have a comprehensive understanding of the different switching regulator noise types and acknowledge the power supply noise requirement in order to design and implement an efficient and low noise switching regulator to meet the low noise specification of most analog circuit power supplies. Compared to LDO regulators, this low noise switching solution will have higher power efficiency, smaller solution size, and lower cost.

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