



PCN Number: MC110816

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Product/Process Change Notification (PCN)

Customer: Digi-Key

Date: 11/08/2016

Customer Part # and/or Lot# affected: A6260KLJTR-T and A6260SLJTR-T

Originator: Mark Caggiano

Phone: 603-626-2538

Duration of Change:

Permanent Temporary (explain)

Summary description of change: Part Change: Process Change: Other:

1. Allegro currently manufactures the A6260KLJTR-T and A6260SLJTR-T on the 6" wafer fab ABCD4 technology line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA. The 6" ABCD4 wafer fab line will be closing. Allegro will change manufacturing to the 8" ABCD4 technology wafer fab line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA
2. The A6260KLJTR-T and A6260SLJTR-T will change the final test location from Allegro MicroSystems, LLC Worcester, MA USA to Allegro MicroSystems (Thailand) Co., Ltd. (AMTC).

What is the part or process changing from (provide details)?

1. Allegro currently manufactures the A6260KLJTR-T and A6260SLJTR-T on the 6" wafer fab ABCD4 technology line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA, The 6" ABCD4 wafer fab line will be closing.
2. The A6260KLJTR-T and A6260SLJTR-T final test location is Allegro MicroSystems, LLC, Worcester, MA USA.

What is the part or process changing to (describe the anticipated impact of this change on form, fit and/or function)?

1. The A6260KLJTR-T and A6260SLJTR-T will change manufacturing to the 8 inch wafer fab ABCD4 technology line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA..
2. The A6260KLJTR-T and A6260SLJTR-T will change final test locations to Allegro MicroSystems (Thailand) Co., Ltd. (AMTC).

Allegro will be expanding its manufacturing capabilities with the addition of a new, wholly-owned integrated circuit test facility located in Saraburi, Thailand. The same make and model test equipment will be utilized and test site transfer buy off data will be on file for each device before production begins.



Note: Validation of equivalence within a specific application is at the discretion of the Customer

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Is a PPAP update required?

Yes

No

Is reliability testing required?

(If Yes, refer to attached plan)

Yes

No (explain)



Reliability Qualification Results

Device: 6260 (9326)

Assy Lot #: 1548731UAAA

Number of Leads: 8

Fab Location: PSL

Package: LJ (eSOIC)

Assembly Location: Unisem

Lead Finish: 100% Sn

Tracking Number: 3316

Reason for Qualification: 6260 (9326) - [6" to 8" Fab Transfer] - Automotive, High Brightness LED, Current Regulator

Reliability Qualification Results						
6260 (9326) - STR#3316						Requirements
Stress Test	Abv.	Test #	Test Method	Test Conditions	S.S.	Results
Preconditioning	PC	A1	JESD22-A113 / J-STD-020	85°C/60% RH, 168 hrs, Peak Reflow=260°C; MSL3, (HAST, AC, TC)	231	0 Rejects
HAST	HAST	A2	JESD22-A110	Ta=130°C, 85% RH, 2 ATM, 0, 96 hrs	77	0 Rejects
Autoclave	AC	A3	JESD22-A102	Ta=121°C, 100% RH, 15 PSIG, 0, 96 hrs	77	0 Rejects
Temperature Cycle	TC	A4	JESD22-A104	Ta = -65°C to +175°C, 0, 500, 1000 Cycles	77	0 Rejects
Wire Bond Pull	WBP	C2	Mil-Std-883 Method 2011	Temp conditions and sample size are defined in the test method. (after TC)		0 Rejects; Cpk>1.67
High Temperature Operating Life	HTOL	B1	JESD22-A108	Ta=125°C, 0, 1000 hrs	77	0 Rejects
Early Life Failure Rate	ELFR	B2	AEC-Q100-008 / JESD22-A108	Ta=125°C, 0, 48 hrs	800	0 Rejects
Electrostatic Discharge Human Body Model	HBM	E2	AEC-Q100-002 / JS-001-2014	Test Conditions, Sampling Size are defined in the Test Method		Classification H2, HBM = 2.0kV
Electrostatic Discharge Charged Device Model	CDM	E3	AEC-Q100-011	Test Conditions, Sampling Size are defined in the Test Method		Classification C6, > 1kV
Latch-Up	LU	E4	JESD78	Test Conditions, Sampling Size are defined in the Test Method		Class II, Level A
Electrical Distributions	ED	E5	AEC Q100-009	Tri-Temp Electrical Distributions - 30 pcs. (1 Lot)		0 Rejects; Cpk>1.67

This device qualification is considered to be passing all environmental stress evaluations per the *Allegro MicroSystems, LLC* 900019 specification and AEC-Q100.

Approved by:

Bob Demers

Bob Demers
Product Safety and Reliability
Allegro MicroSystems, LLC

Allegro MicroSystems, LLC

Proprietary

Expected completion date for internal qualification: Complete

Expected PPAP availability date: N/A

Target implementation date: May 2017

