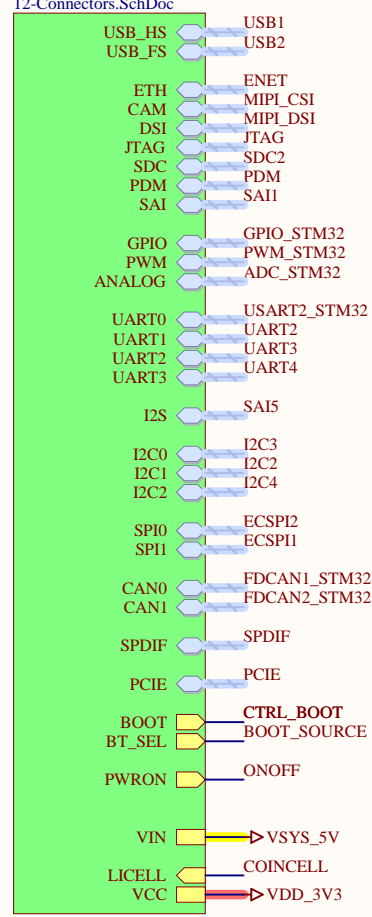
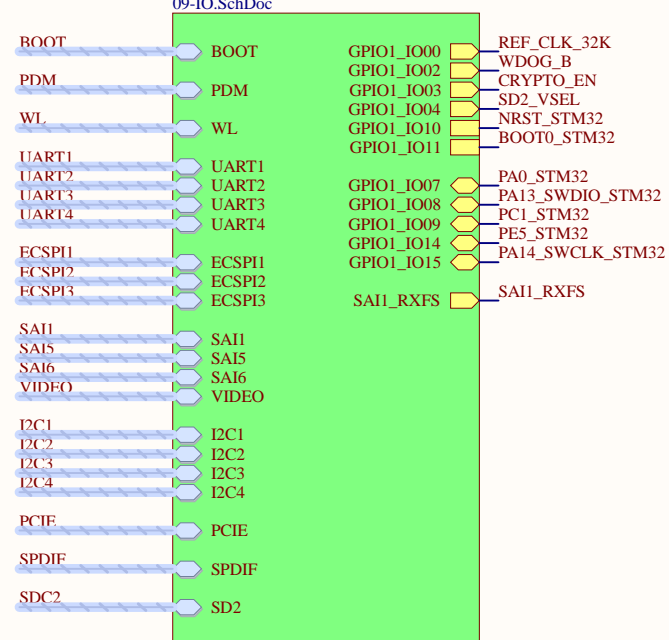


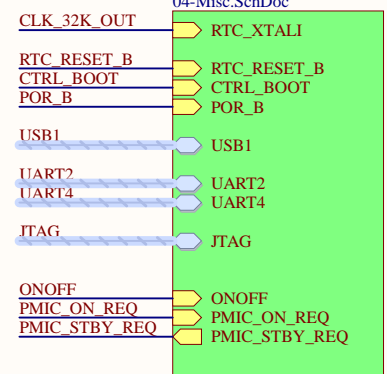
HD CONNECTORS  
12-Connectors.SchDoc



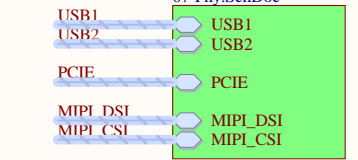
IMX8 IO  
09-IO.SchDoc



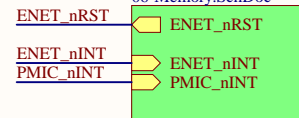
IMX8 MISC  
04-Misc.SchDoc



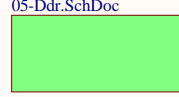
IMX8 Phy  
07-Phy.SchDoc



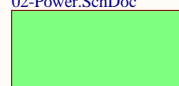
IMX8 Memory  
06-Memory.SchDoc



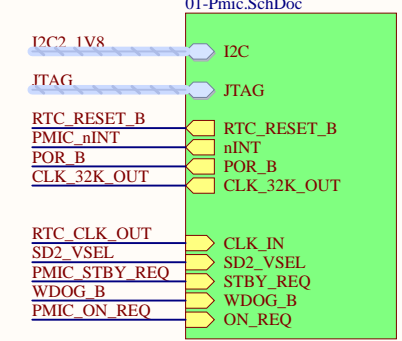
IMX8 DDR  
05-Ddr.SchDoc



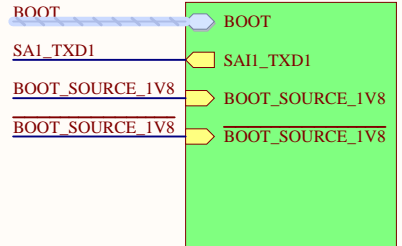
IMX8 Power  
02-Power.SchDoc



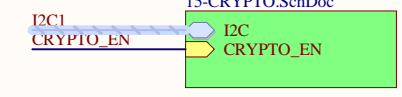
Pmic  
01-Pmic.SchDoc



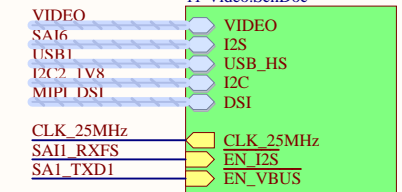
Boot  
03-Boot.SchDoc



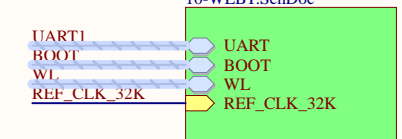
CRYPTO  
15-CRYPTO.SchDoc



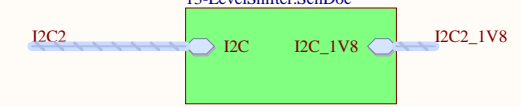
VIDEO, USB C  
11-Video.SchDoc



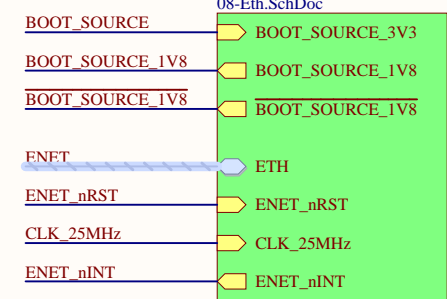
WLBT  
10-WLBT.SchDoc



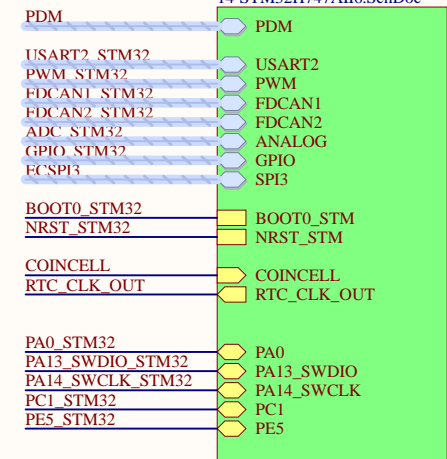
LevelShifter  
13-LevelShifter.SchDoc



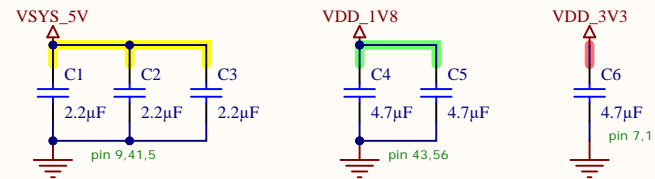
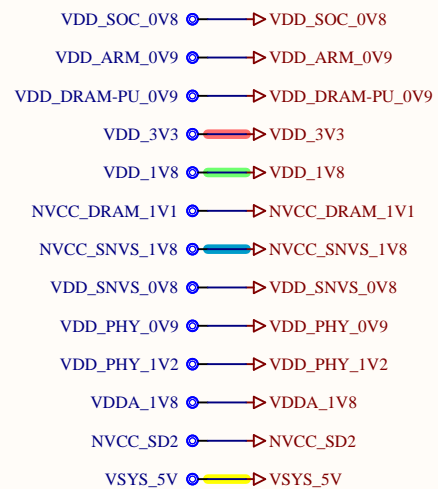
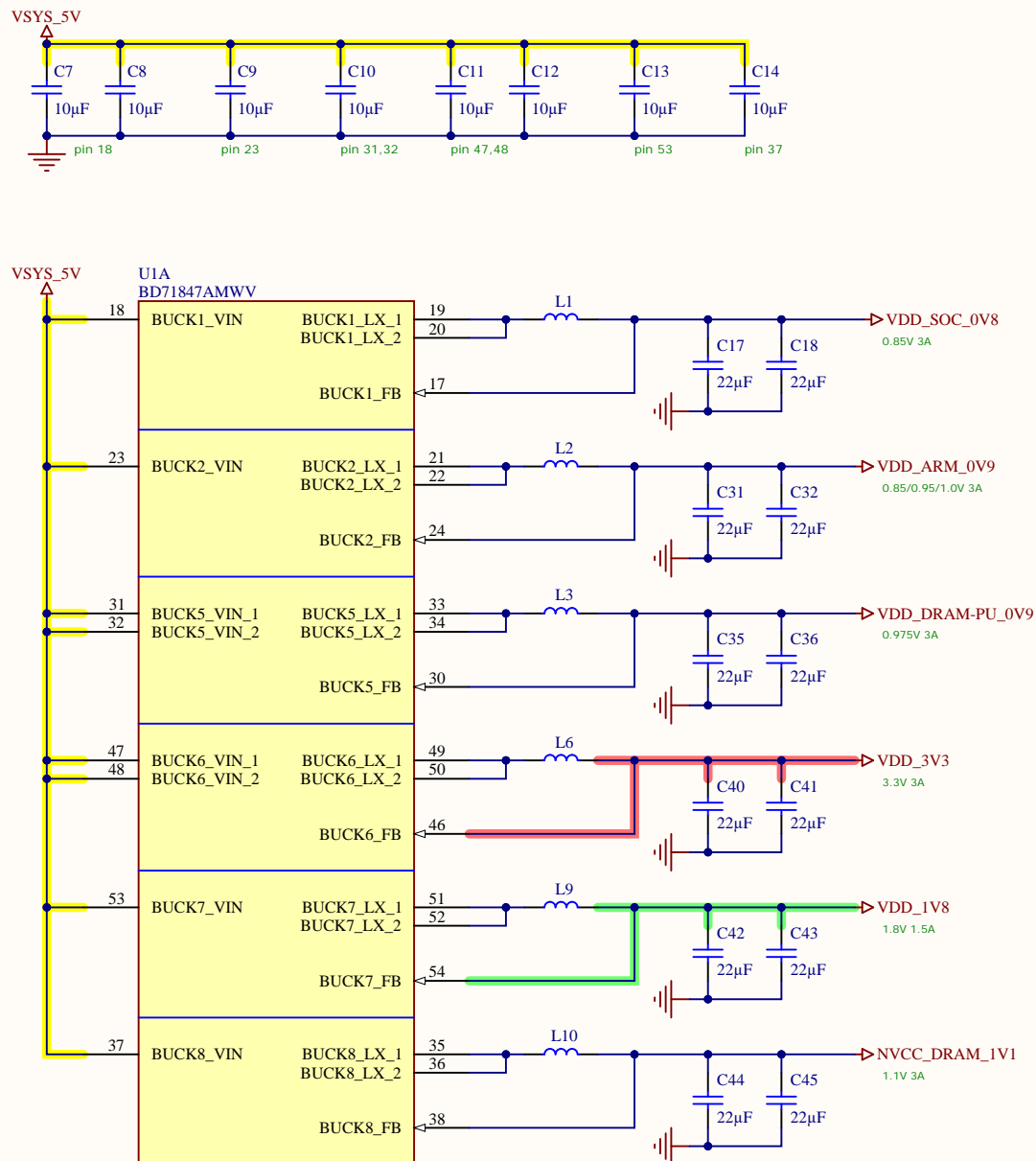
Eth  
08-Eth.SchDoc



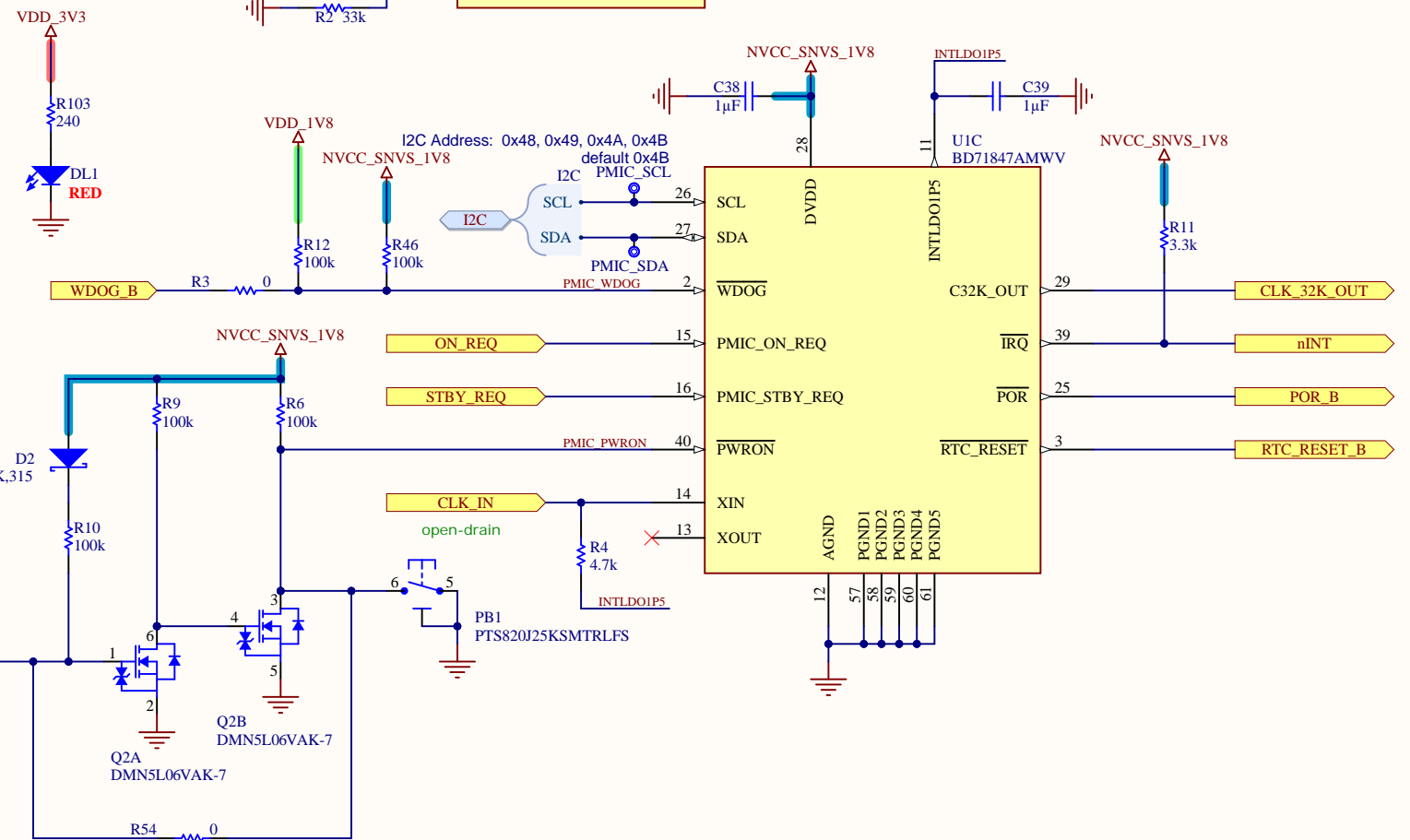
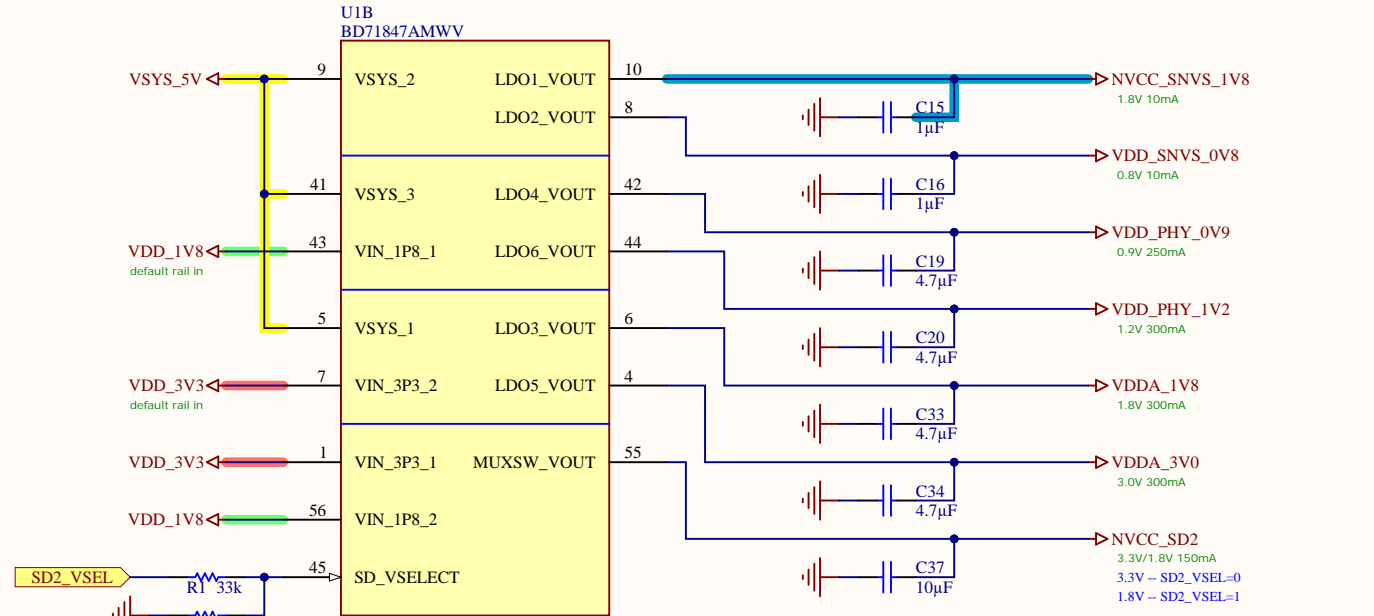
STM32H747AI16  
14-STM32H747AI16.SchDoc



# IMX8Mmini PMIC



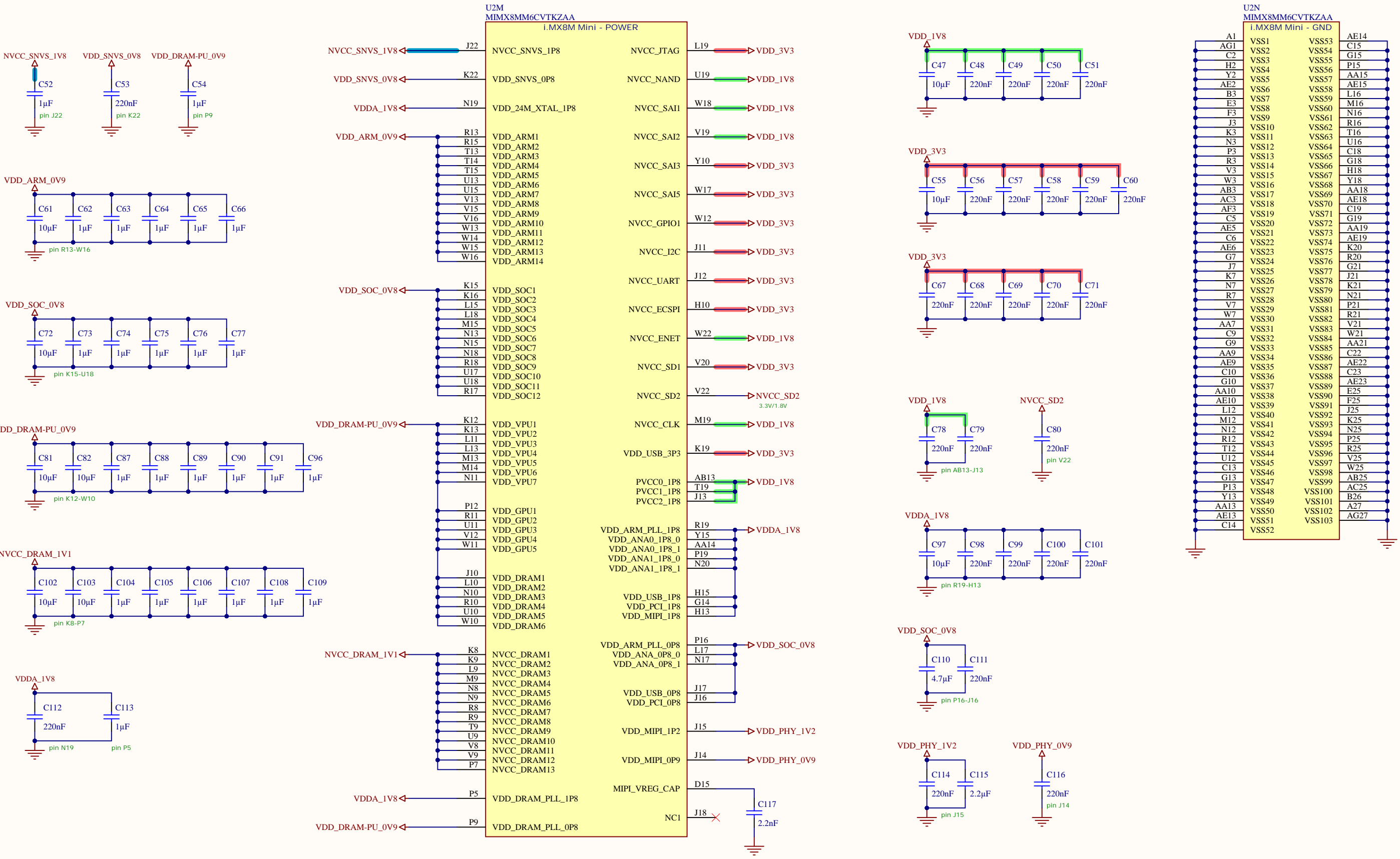
**NOTA**  
LDO5 deve essere settato a 3.0V (def 3.3)  
poi deve essere acceso prima di abilitare ANX7625



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Title: <b>PMIC</b>		Revision: <b>V4.2</b>		
ID: <b>2</b>	Date: <b>2022-02-25</b> Time: <b>16:28:09</b>			
File: 01-Pmic.SchDoc		Author: <b>Dario Pennisi</b>	RevAuthor: <b>Silvio Navaretti</b>	

# IMX8Mmini POWER

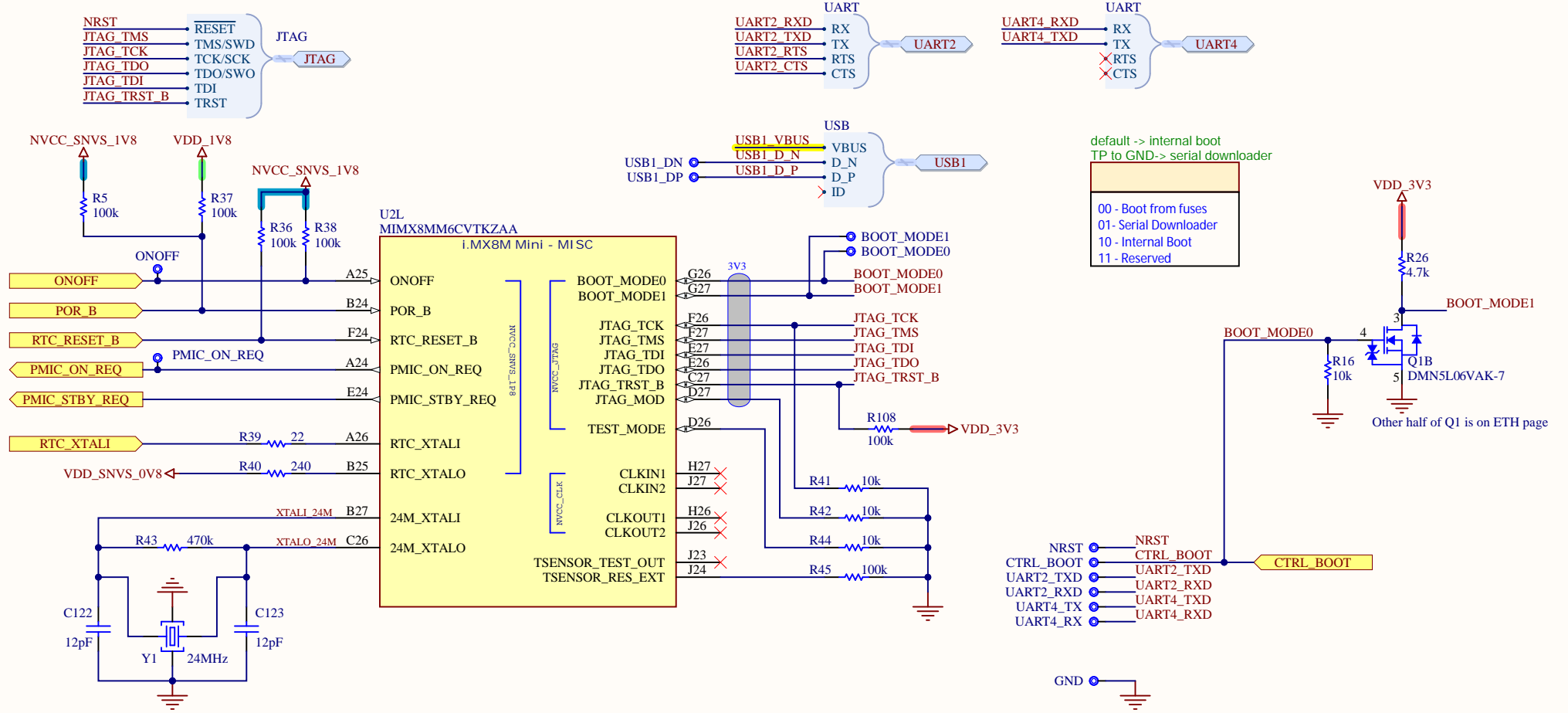


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Title: <b>POWER</b>			
ID: 3	Revision: V4.2		
Date: 2022-02-25	Time: 16:28:10	Sheet 3 of 16	
File: 02-Power.SchDoc	Author: Dario Pennisi	RevAuthor: Silvio Navaretti	



# IMX8Mmini MISC



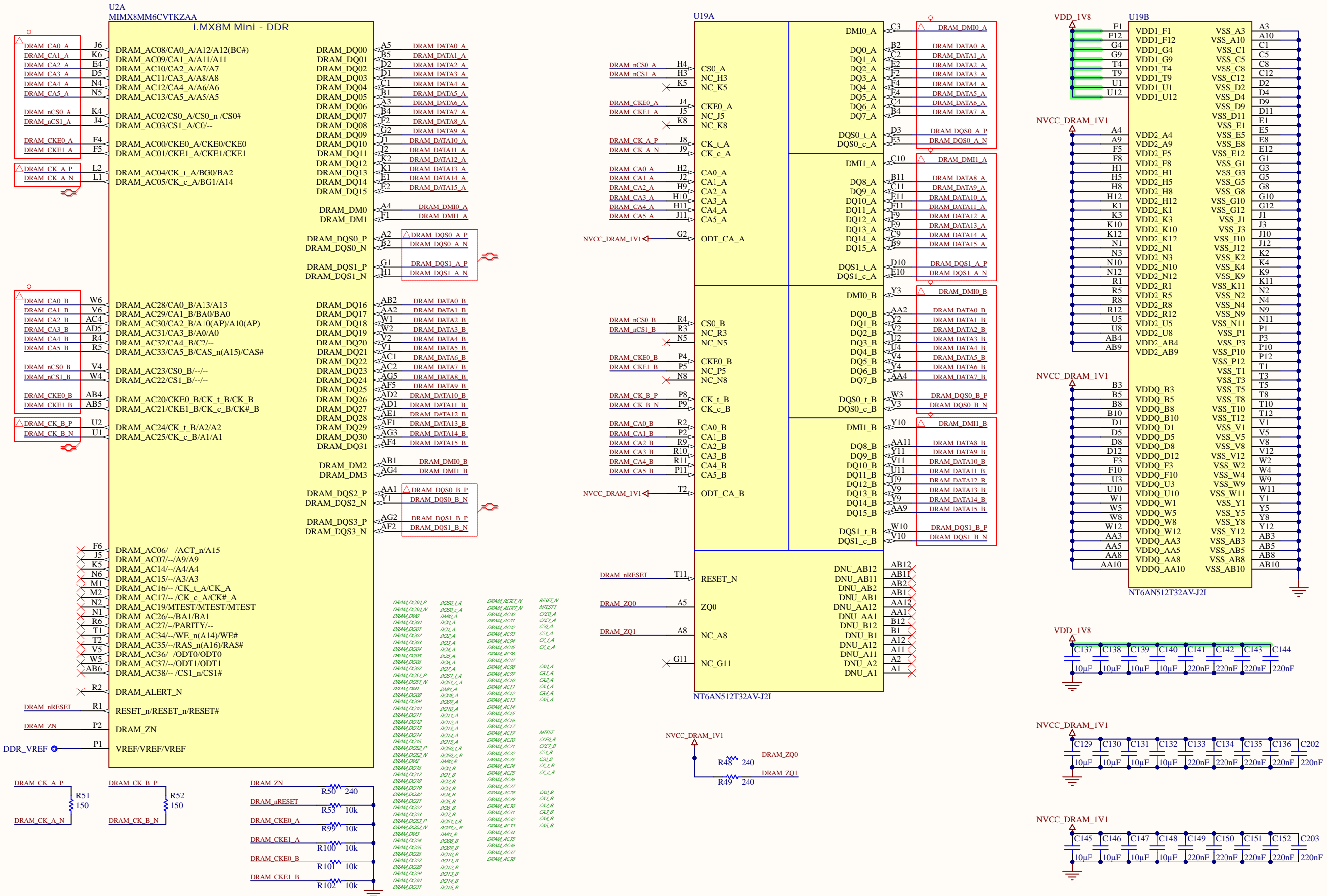
Mfg Tool

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Title: <b>MISCELLANEOUS</b>		Revision: <b>V4.2</b>	
ID: <b>5</b>	Date: <b>2022-02-25</b> Time: <b>16:28:10</b>		
File: <b>04-Misc.SchDoc</b>	Author: <b>Dario Pennisi</b>	Sheet <b>5</b> of <b>16</b>	RevAuthor: <b>*</b>



# IMX8Mmini DDR



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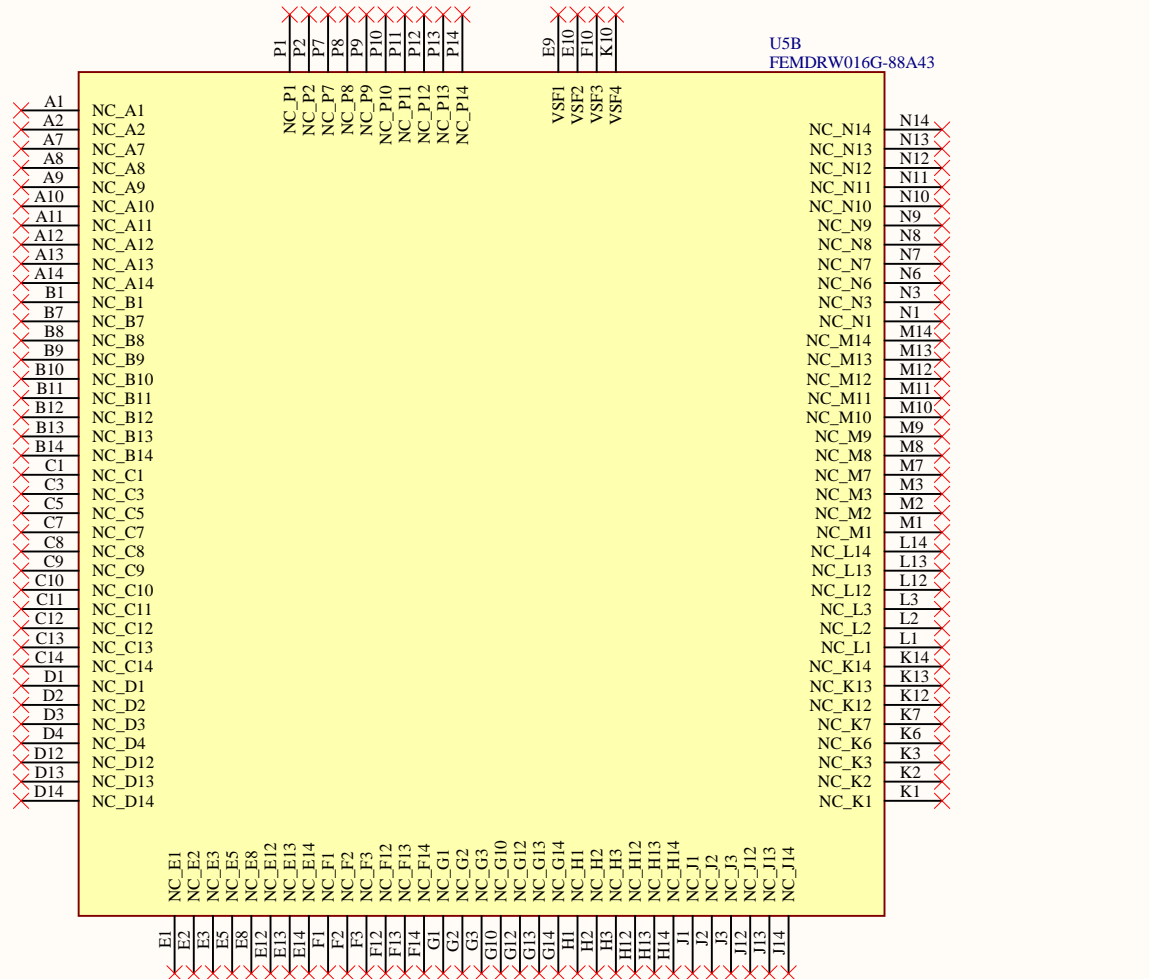
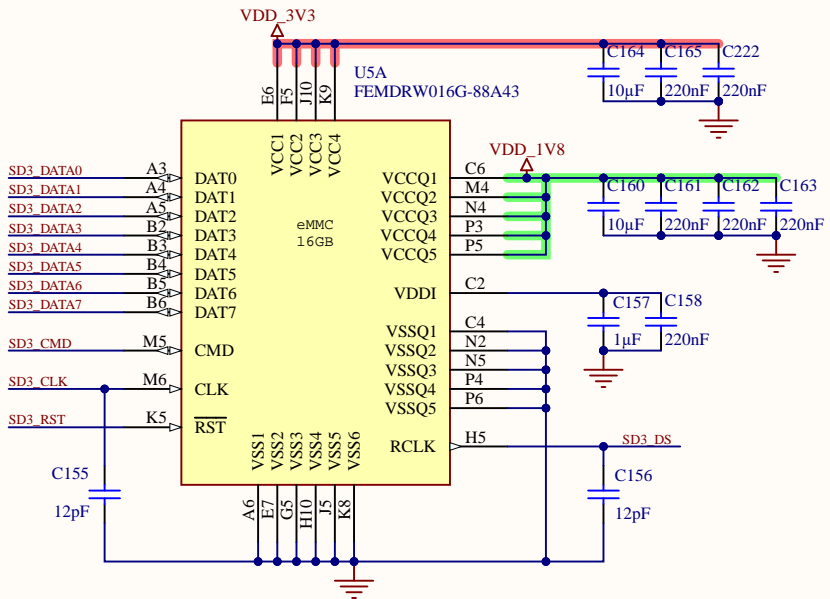
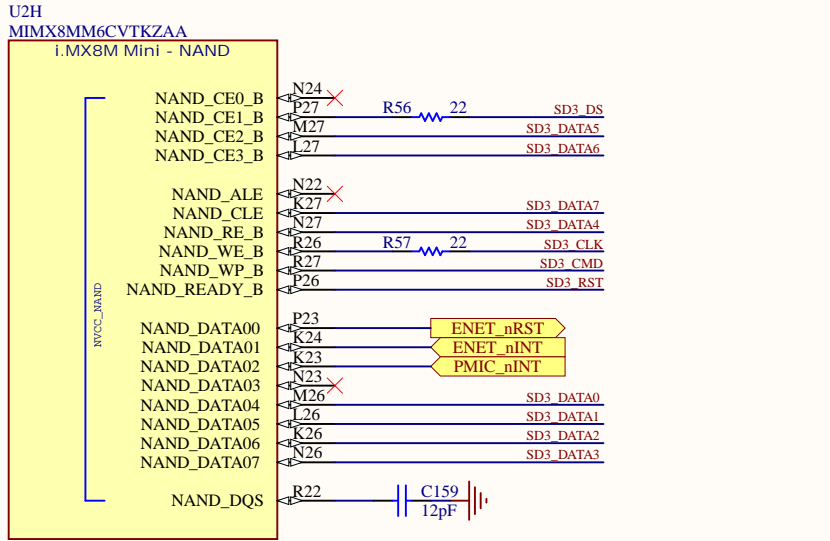
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<b>Title: DDR</b>			
ID: 6	Revision: V4.2		
Date: 2022-02-25	Time: 16:28:11	Sheet 6 of 16	
File: 05-Dr.SchDoc	Author: Dario Pennisi	RevAuthor: Silvio Navaretti	

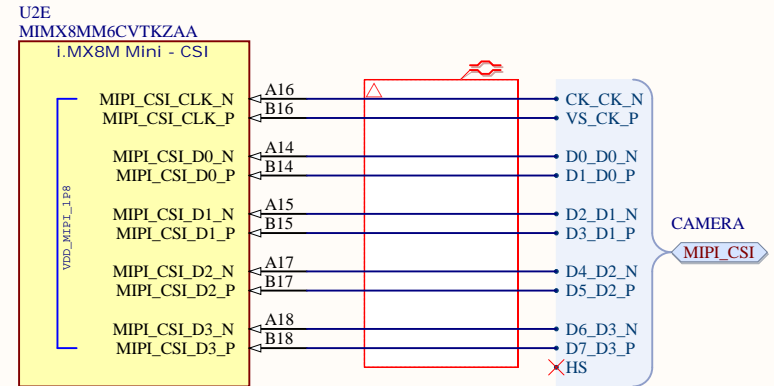
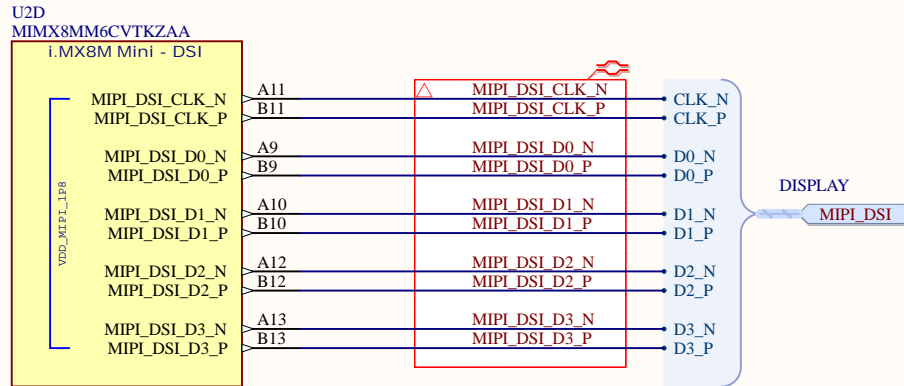
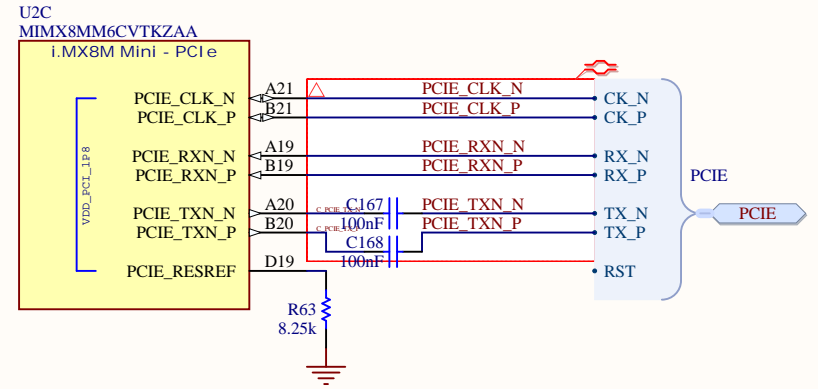
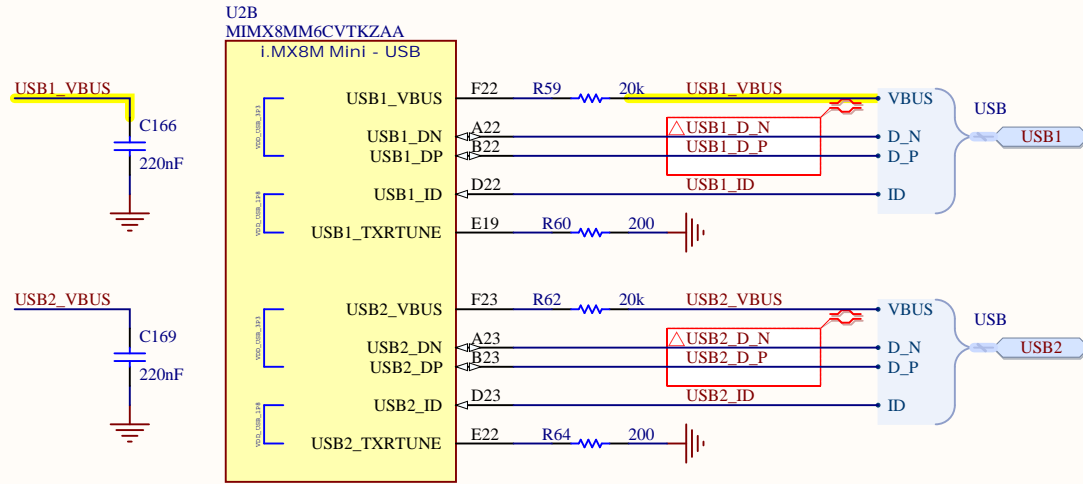
# IMX8Mmini Memory



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<b>Title: MEMORY</b>					
ID: 7		Revision: V4.2			
Date: 2022-02-25		Time: 16:28:11		Sheet 7 of 16	
File: 06-Memory_SchDoc		Author: Dario Pennisi		RevAuthor: Silvio Navaretti	

# IMX8Mmini PHY

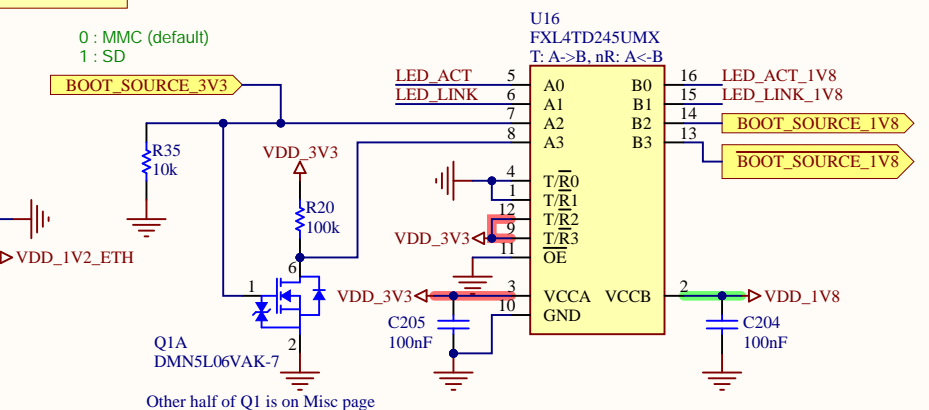
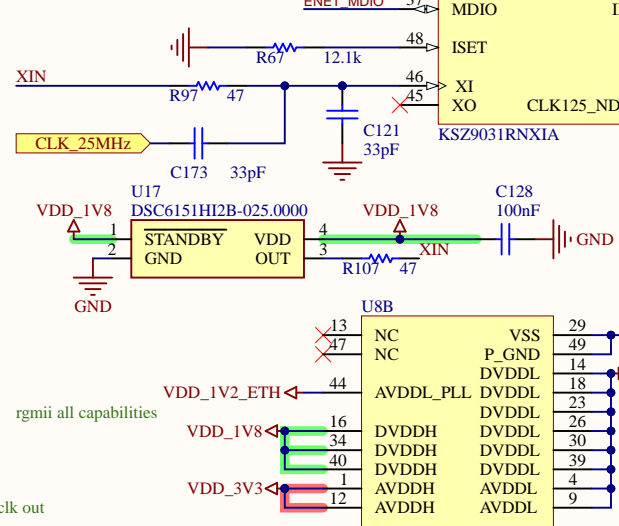
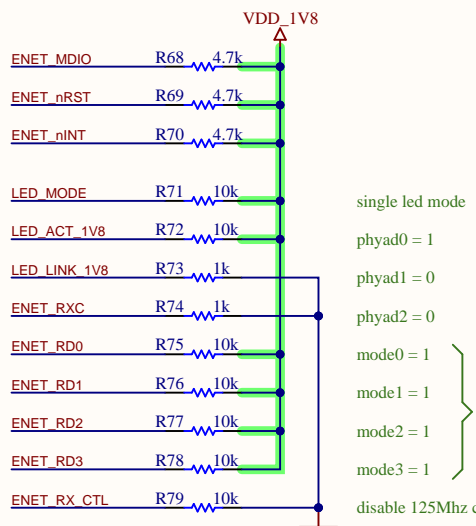
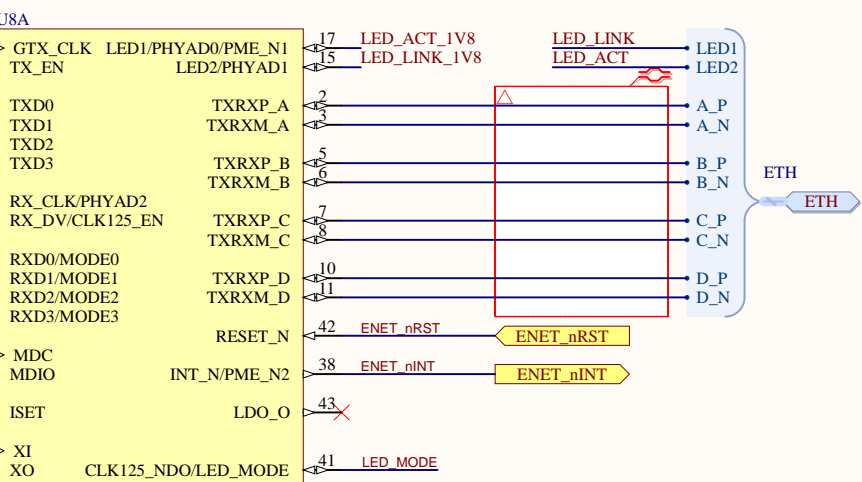
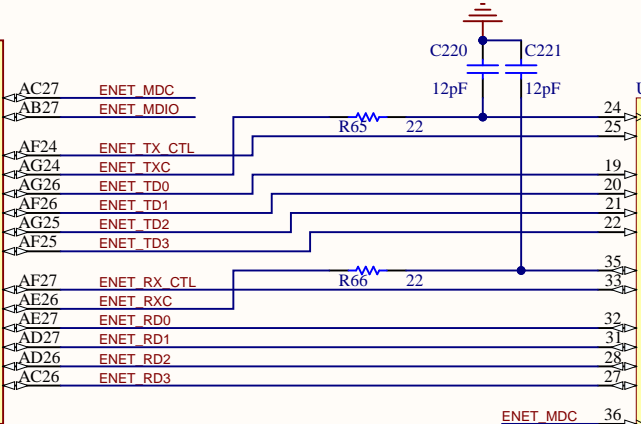
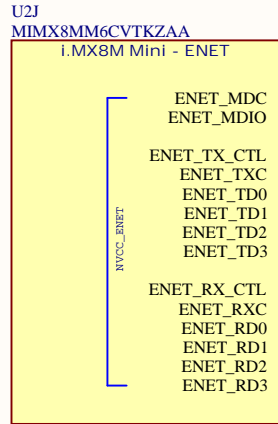
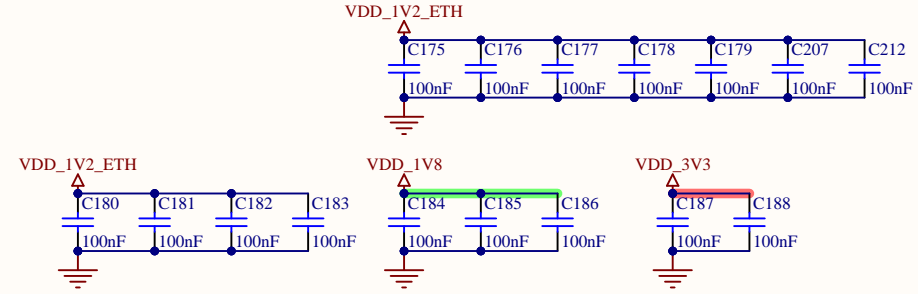
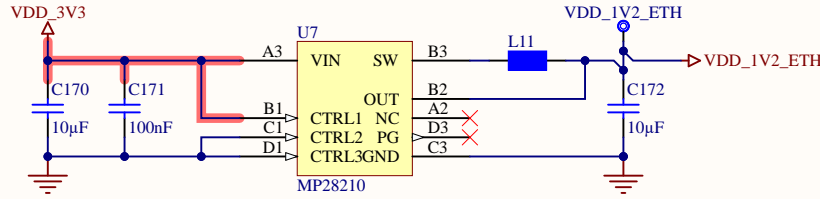


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<b>Title: PHY</b>					
<b>ID: 8</b>		Revision: V4.2			
Date: 2022-02-25	Time: 16:28:12	Sheet 8 of 16			
File: 07-Phy.SchDoc		Author: Dario Pennisi		RevAuthor: Silvio Navaretti	



# IMX8Mmini ETH

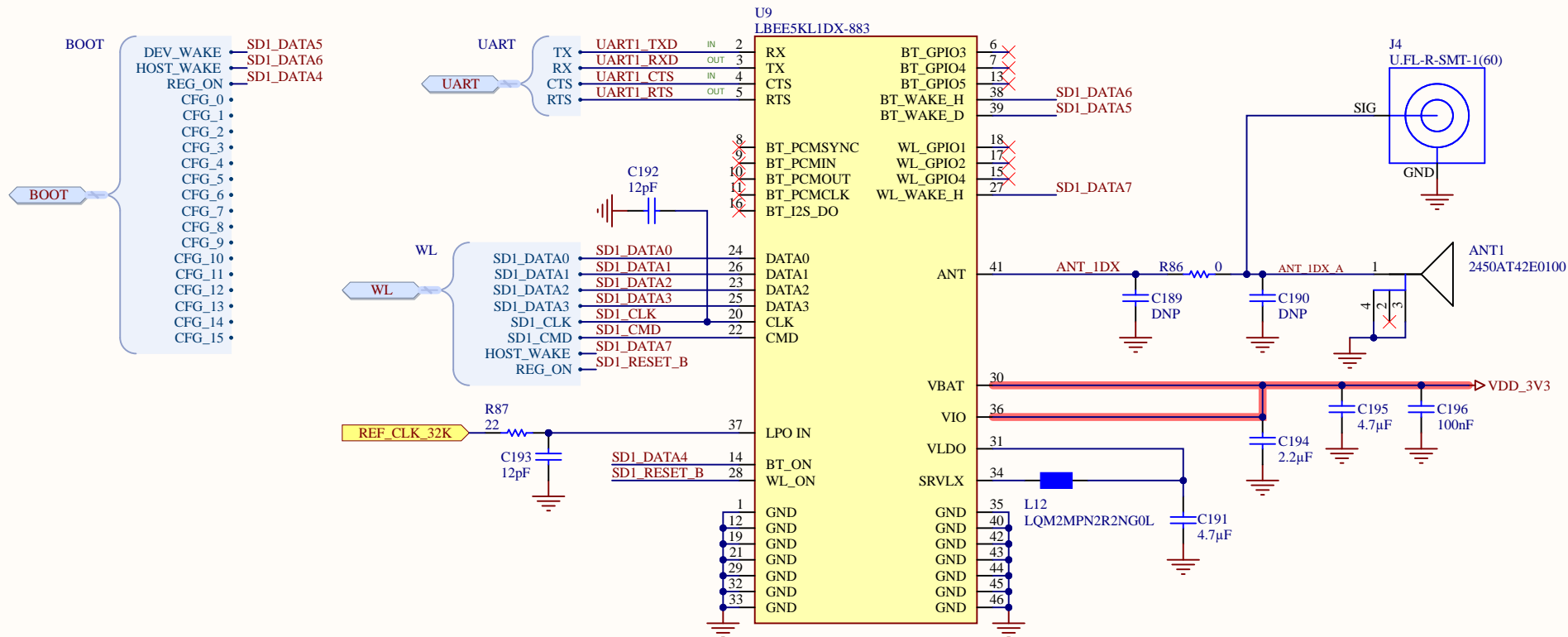


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Title: <b>ETHERNET</b>		Revision: <b>V4.2</b>	
ID: <b>9</b>	Date: <b>2022-02-25</b>	Time: <b>16:28:12</b>	Sheet <b>9</b> of <b>16</b>
File: <b>08-Eth.SchDoc</b>	Author: <b>Dario Pennisi</b>	RevAuthor: <b>Silvio Navaretti</b>	



# IMX8Mmini WL/BT

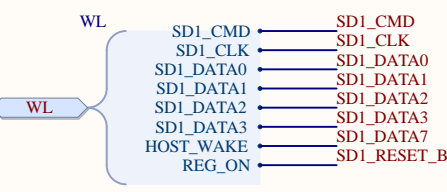
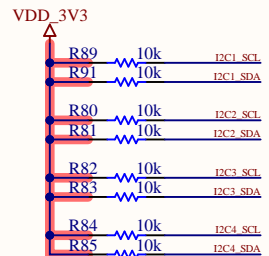
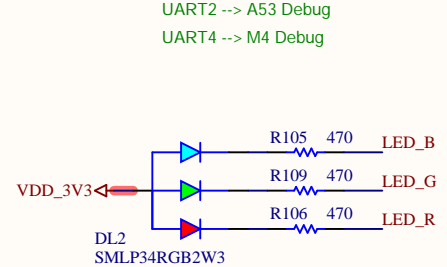
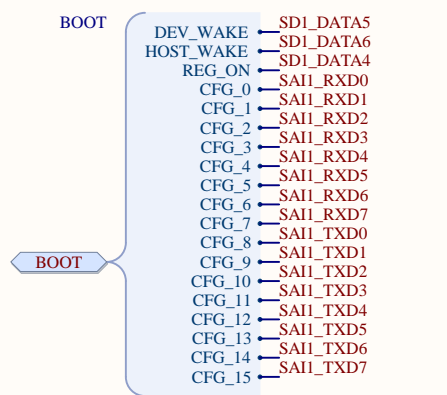
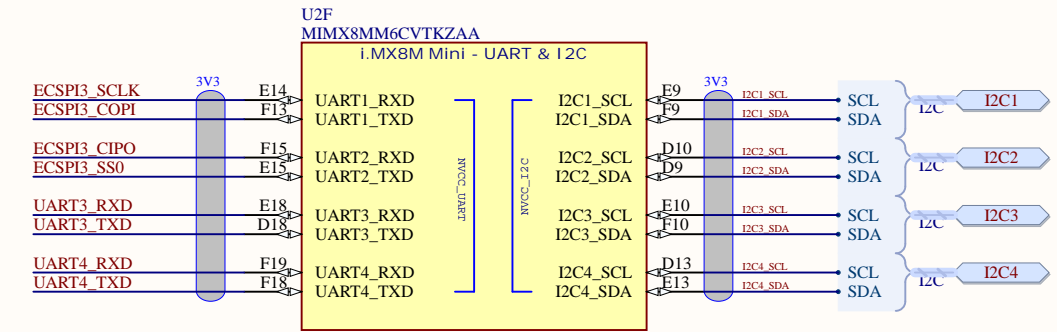
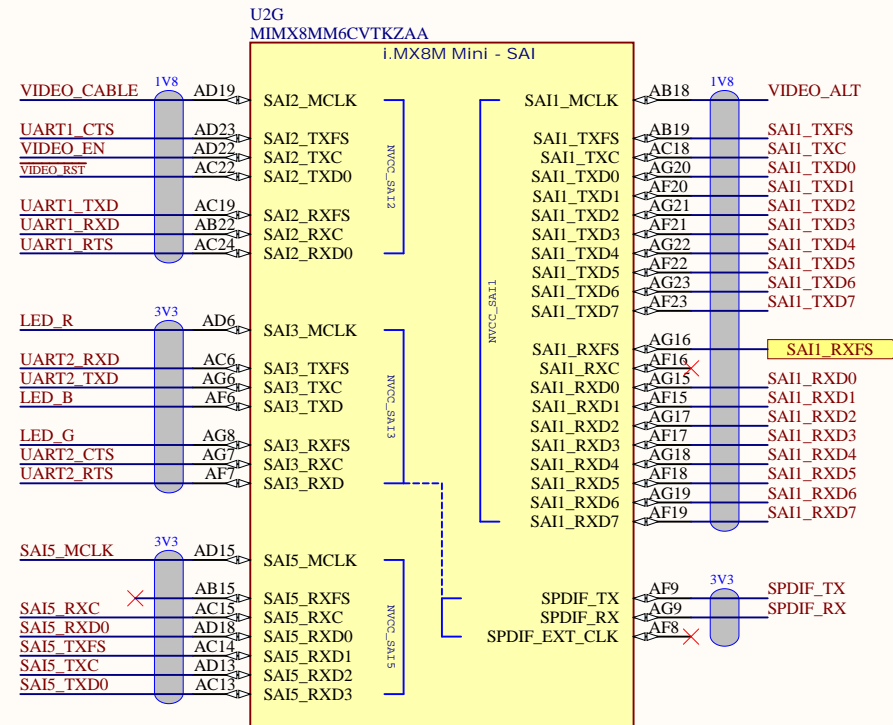
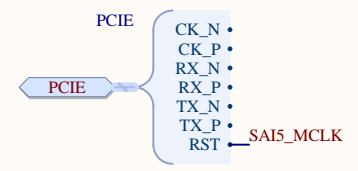
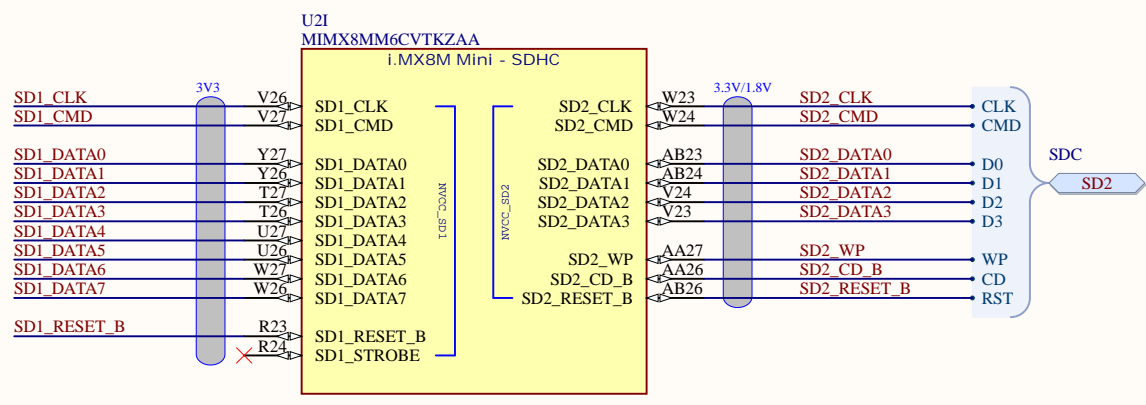
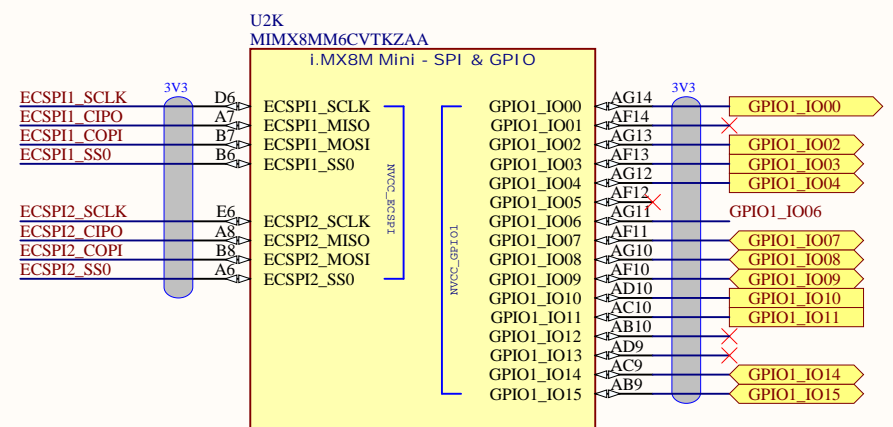
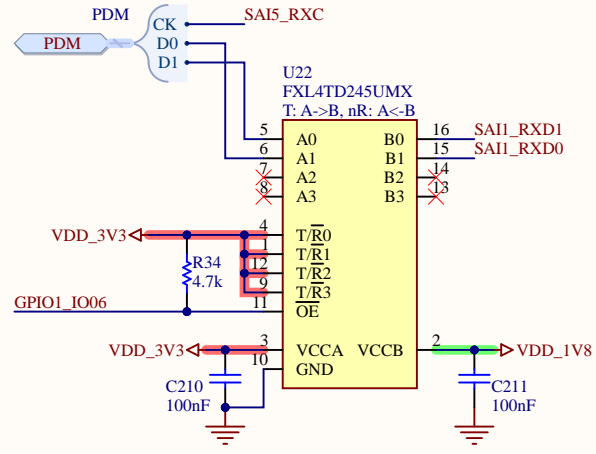
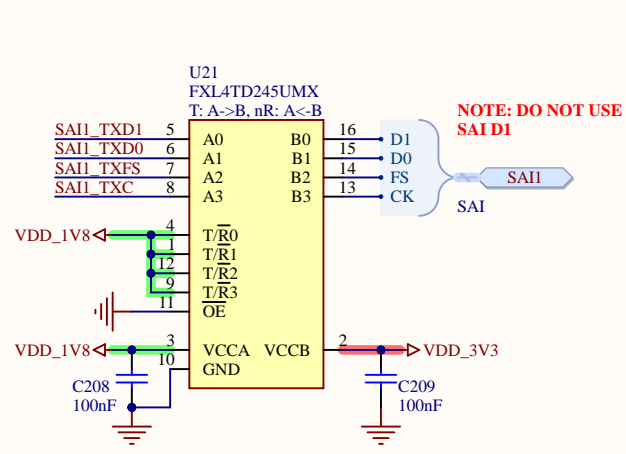
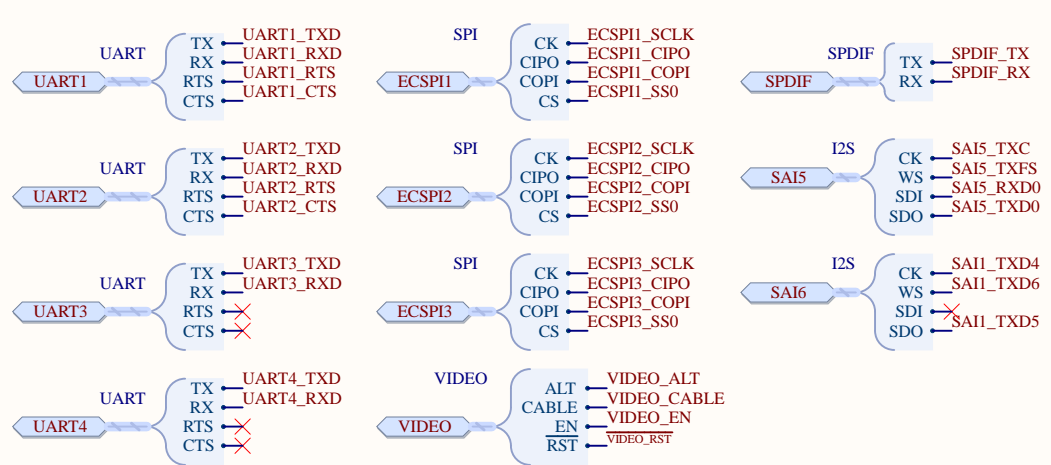


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Title: <b>WLBT</b>		Revision: <b>V4.2</b>	
ID: <b>11</b>	Date: <b>2022-02-25</b>	Time: <b>16:28:12</b>	Sheet <b>10</b> of <b>16</b>
File: <b>10-WLBT.SchDoc</b>	Author: <b>Dario Pennisi</b>		RevAuthor: <b>Silvio Navaretti</b>



# IMX8Mmini IO

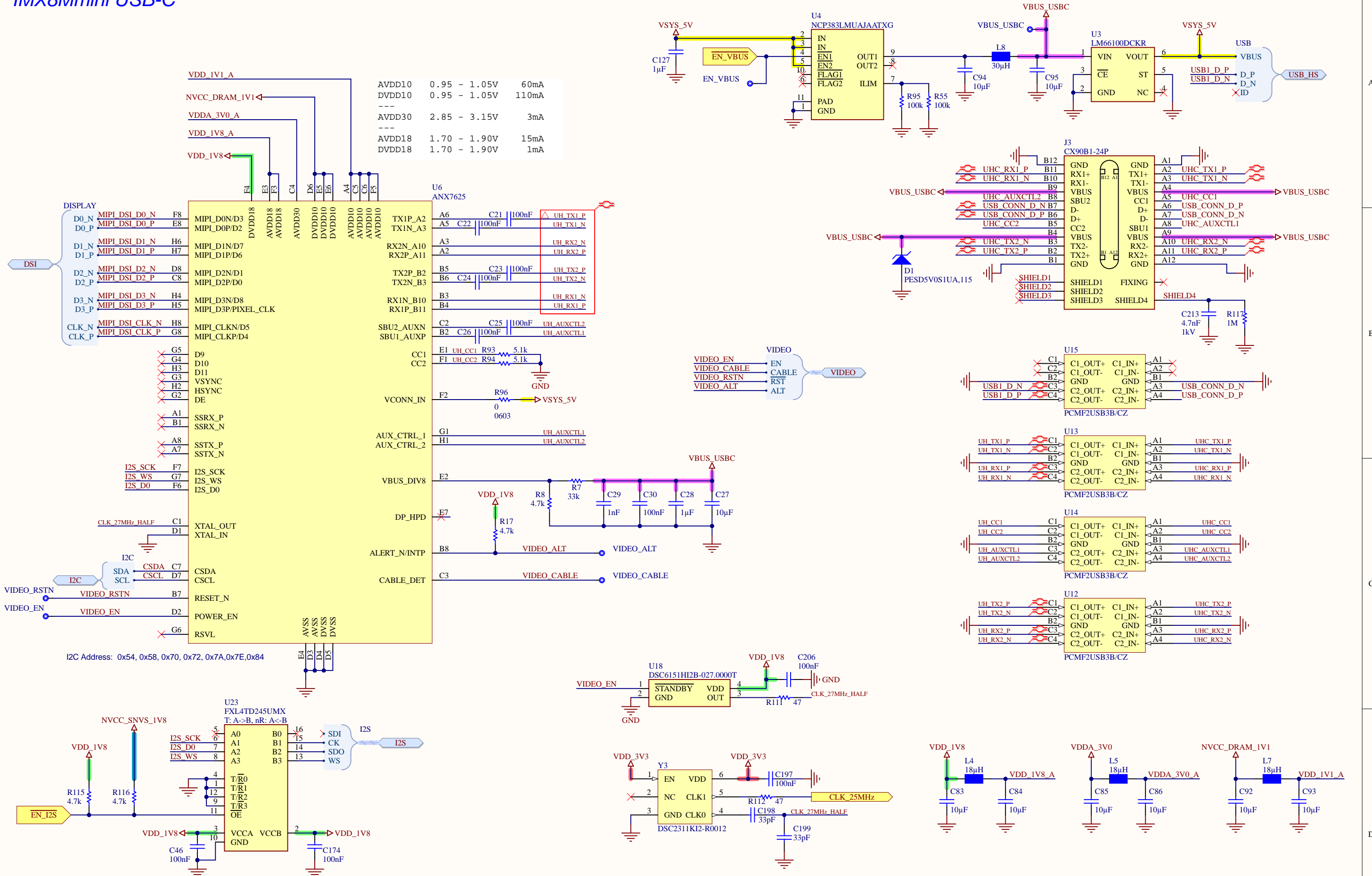


**Caution:**  
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead. All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's. See Errata e50080 for detailed information.

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<b>Title: IO</b>			
ID: 10	Revision: V4.2		
Date: 2022-02-25	Time: 16:28:13	Sheet 11 of 16	
File: 09-IO.SchDoc	Author: Dario Pennisi	RevAuthor: Silvio Navaretti	

# IMX8Mmini USB-C

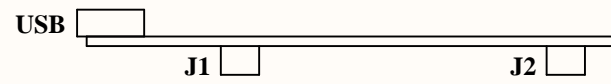


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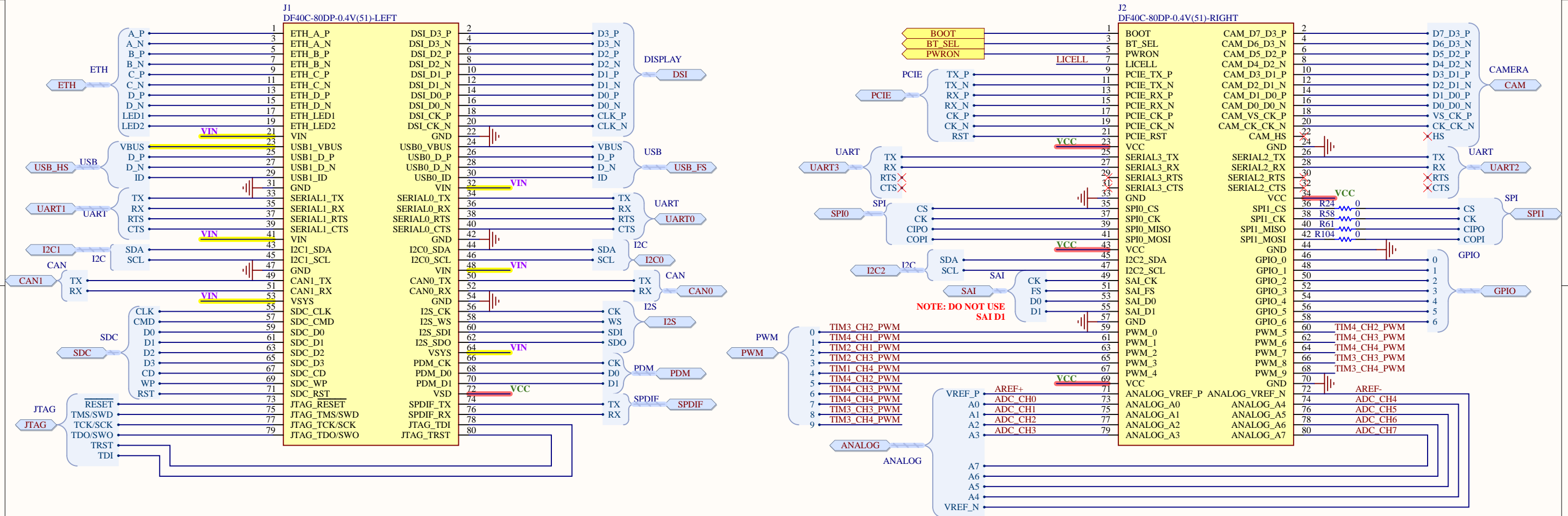
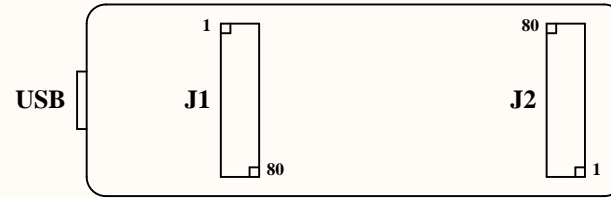
Title: VIDEO			
ID: 12	Revision: V4.2		
Date: 2022-02-25	Time: 16:28:13	Sheet 12 of 16	
File: 11-Video.SchDoc	Author: Dario Pennisi	RevAuthor: Silvio Navaretti	

# IMX8Mmini Connectors

Board side view:



Board BOTTOM view:

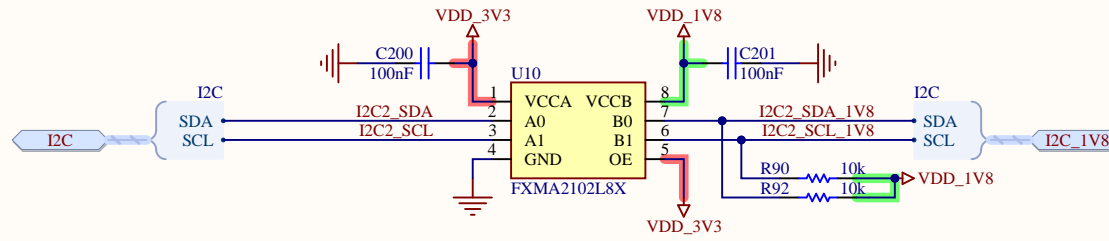


## POWER NETS TABLE



NET	TYPE	RANGES	DESCRIPTION
VIN	PORTENTA INPUT	4.1V to 6V.	Default 3.3V, PMIC (U1) programmable output.
VCC	PORTENTA OUTPUT	1.1V to 3.3V in steps, max 1A.	Default 3.3V, PMIC (U1) programmable output.
LICELL	PORTENTA INPUT	Coinc cell max 3.6V, max 46uA.	Max 4uA with PMIC (U1) in coin cell mode, max 46uA with PMIC in standby/suspend mode.

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# IMX8Mmini LevelShifter



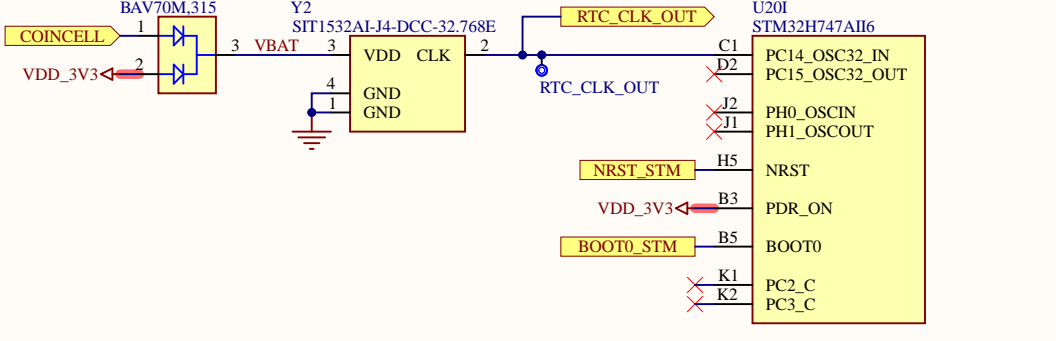
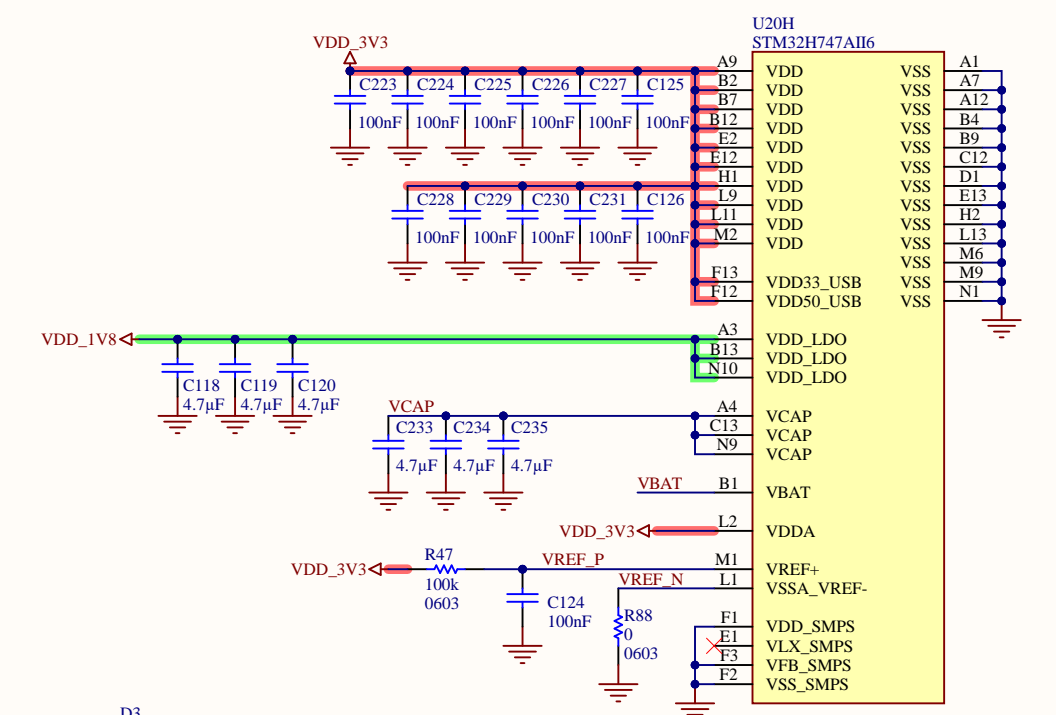
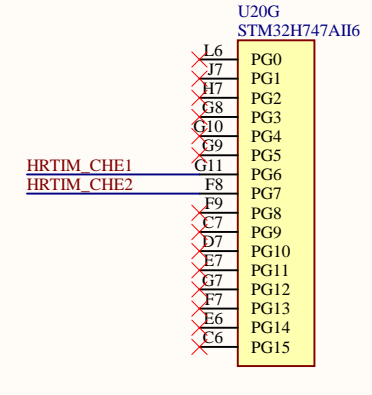
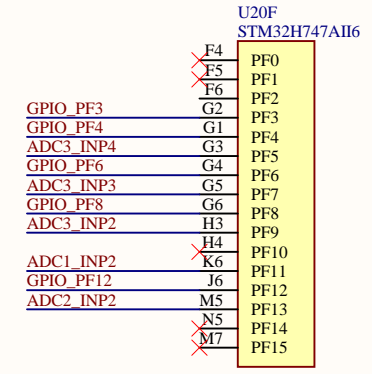
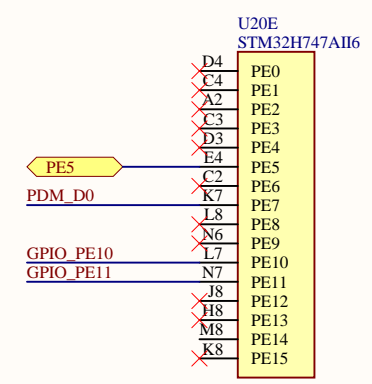
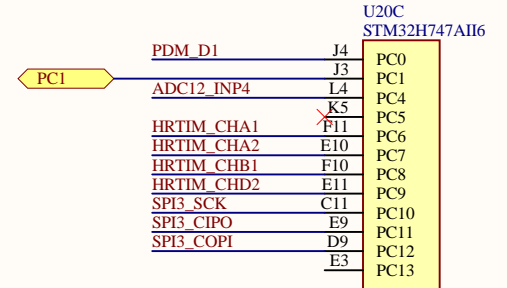
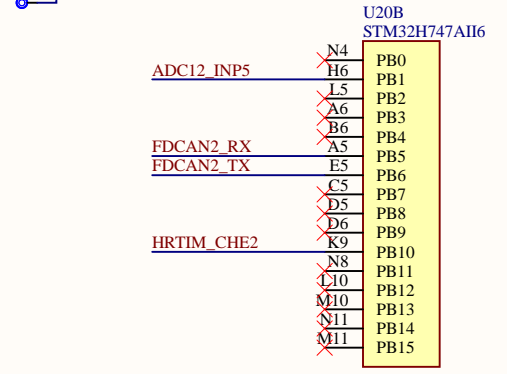
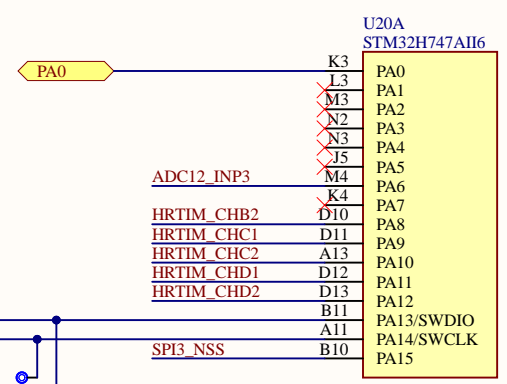
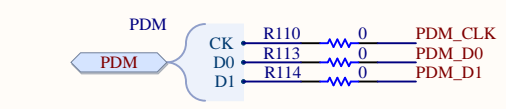
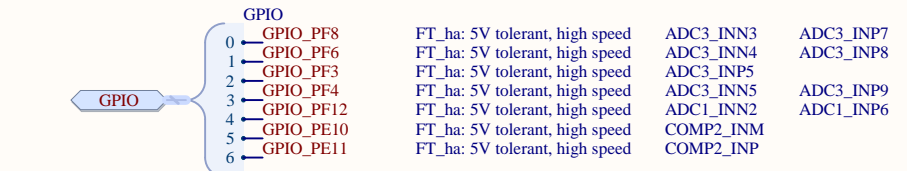
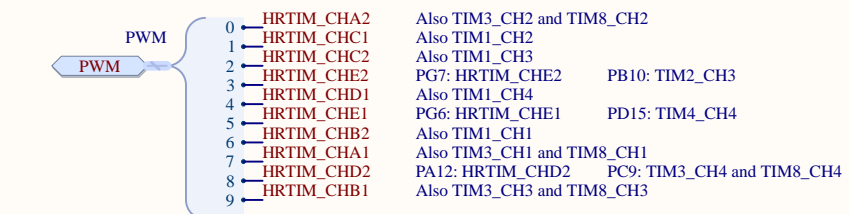
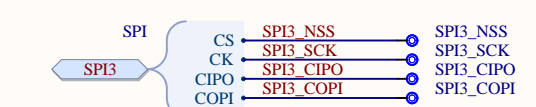
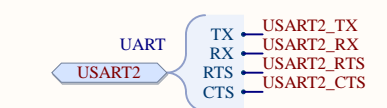
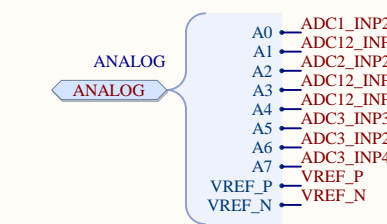
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Title: <b>LEVEL SHIFTER</b>		 	
ID: 14	Revision: V4.2		
Date: 2022-02-25	Time: 16:28:14	Sheet 14 of 16	
File: 13-LevelShifter.SchDoc	Author: Dario Pennisi	RevAuthor: Silvio Navaretti	

MCO1 test points (PA8)

MCO\_BOT HRTIM\_CHB2 MCO1 test point BOTTOM

MCO1\_TOP HRTIM\_CHB2 MCO1 test point TOP



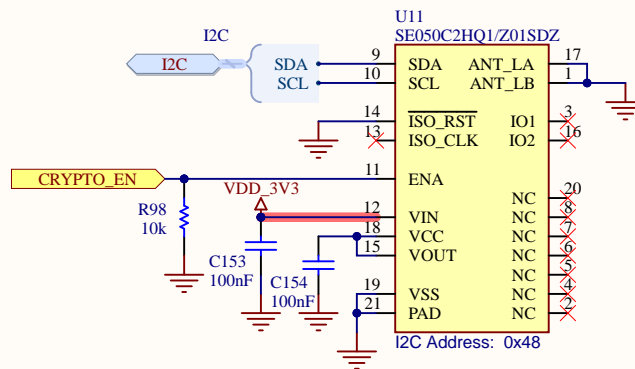
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Title: <b>STM32H7</b>			
ID: 15	Revision: V4.2		
Date: 2022-02-25	Time: 16:28:14	Sheet 15 of 16	
File: 14-STM32H747AI16.SchDoc		Author: Dario Pennisi	RevAuthor: Silvio Navaretti



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<b>Title: CRYPTO</b>		 	
<b>ID: 16</b>	<b>Revision: V4.2</b>		
<b>Date: 2022-02-25</b>	<b>Time: 16:28:14</b>	<b>Sheet 16 of 16</b>	
<b>File: 15-CRYPTO.SchDoc</b>		<b>Author: Dario Pennisi</b>	<b>RevAuthor: Silvio Navaretti</b>