SCDS006O − NOVEMBER 1992 − REVISED NOVEMBER 2004

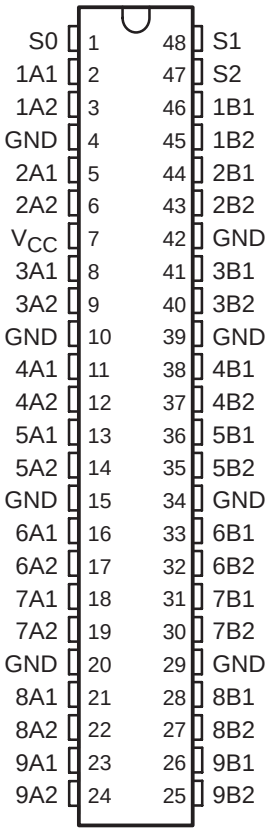
- **Members of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

## description/ordering information

The SN54CBT16209 and SN74CBT16209A devices provide 18 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switches allows connections to be made with minimal propagation delay.

The devices operate as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

**SN54CBT16209 . . . WD PACKAGE**
**SN74CBT16209A . . . DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**




**ORDERING INFORMATION**

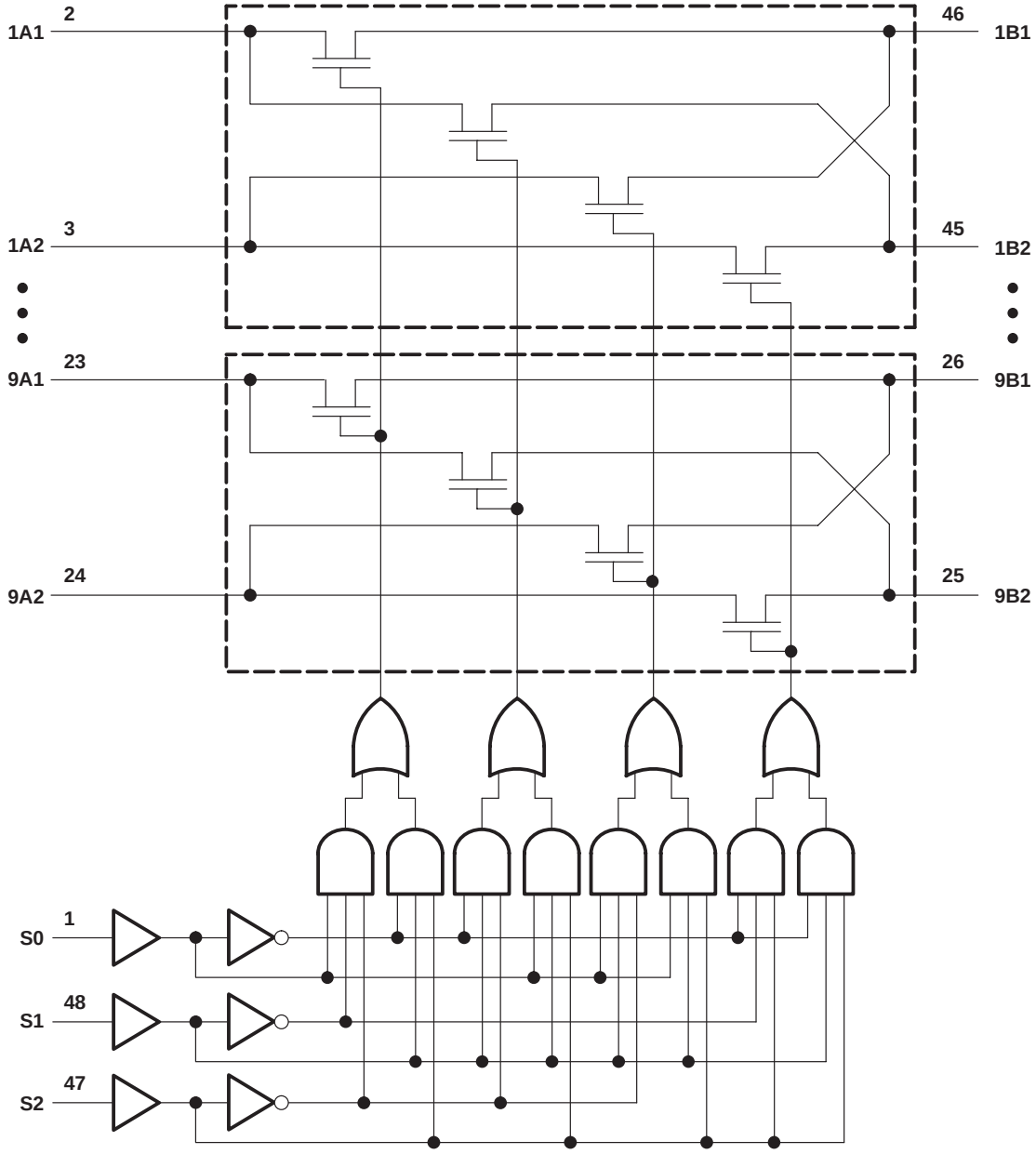
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SSOP − DL | Tube | SN74CBT16209ADL | CBT16209A |
| | | Tape and reel | SN74CBT16209ADLR | |
| | TSSOP − DGG | Tape and reel | SN74CBT16209ADGGR | CBT16209A |
| | TVSOP − DGV | Tape and reel | SN74CBT16209ADGVR | CY209A |
| −55°C to 125°C | CFP − WD | Tube | SNJ54CBT16209WD | SNJ54CBT16209WD |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**

| INPUTS | | | INPUTS/OUTPUTS | | FUNCTION |
|---|---|---|---|---|---|
| S2 | S1 | S0 | A1 | A2 | |
| L | L | L | Z | Z | Disconnect |
| L | L | H | B1 | Z | A1 port = B1 port |
| L | H | L | B2 | Z | A1 port = B2 port |
| L | H | H | Z | B1 | A2 port = B1 port |
| H | L | L | Z | B2 | A2 port = B2 port |
| H | L | H | Z | Z | Disconnect |
| H | H | L | B1 | B2 | A1 port = B1 port<br>A2 port = B2 port |
| H | H | H | B2 | B1 | A1 port = B2 port<br>A2 port = B1 port |

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . −50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 70°C/W
DGV package . . . . . 58°C/W
DL package . . . . . 63°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

| | | SN54CBT16209 | | SN74CBT16209A | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4 | 5.5 | 4 | 5.5 | V |
| $V_{IH}$ | High-level control input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level control input voltage | | 0.8 | | 0.8 | V |
| $T_A$ | Operating free-air temperature | −55 | 125 | −40 | 85 | °C |

NOTE 3: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | | −1.2 | V |
| $I_I$ | | $V_{CC}$ = 0, | $V_I$ = 5.5 V | | | | 10 | μA |
| | | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V or GND | | | | ±1 | |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $I_O$ = 0, | $V_I$ = $V_{CC}$ or GND | | | 3 | μA |
| $\Delta I_{CC}$§ | Control inputs | $V_{CC}$ = 5.5 V, | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 2.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 3 V or 0 | | | | 4 | | pF |
| $C_{io(OFF)}$ | | $V_O$ = 3 V or 0, | S0, S1, and S2 = GND | | | 7.5 | | pF |
| $r_{on}$¶ | | $V_{CC}$ = 4 V<br>TYP at $V_{CC}$ = 4 V | $V_I$ = 2.4 V, | $I_I$ = 15 mA | | 14 | 20 | Ω |
| | | $V_{CC}$ = 4.5 V | $V_I$ = 0 | $I_I$ = 64 mA | | 4 | 8 | |
| | | | | $I_I$ = 30 mA | | 4 | 8 | |
| | | | $V_I$ = 2.4 V, | $I_I$ = 15 mA | | 6 | 15 | |

‡ All typical values are at $V_{CC}$ = 5 V (unless otherwise noted), $T_A$ = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

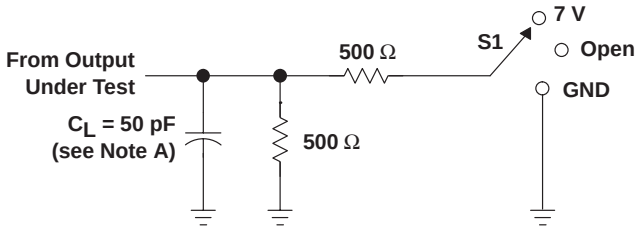
**switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54CBT16209 | | | | SN74CBT16209A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 4 V | | $V_{CC}$ = 5 V ± 0.5 V | | $V_{CC}$ = 4 V | | $V_{CC}$ = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$† | A or B | B or A | | | | 0.8* | | 0.35 | | 0.25 | ns |
| $t_{pd}$ | S | A or B | | 14 | 2 | 13.1 | | 9.9 | 1.5 | 9 | ns |
| $t_{en}$ | S | A or B | | 16 | 1.7 | 15.3 | | 10.3 | 1.5 | 9.8 | ns |
| $t_{dis}$ | S | A or B | | 14.5 | 1 | 13.2 | | 9.3 | 1.5 | 8.8 | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

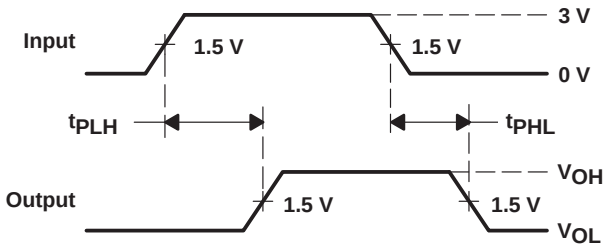
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## PARAMETER MEASUREMENT INFORMATION

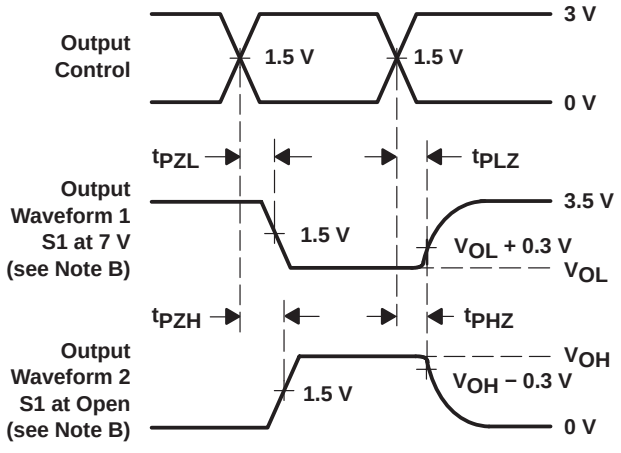



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

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