

Automotive 5 V low dropout voltage regulator

Datasheet - production data



- Programmable reset pulse delay with external capacitor
- Thermal shutdown and short-circuit protection
- Wide temperature range ($T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$)

Description

L5300RPT is a low dropout linear regulator with low voltage reset. Only a low-value ceramic capacitor is required for stability (above or equal 220 nF).

Typical quiescent current is 55 μA in light load condition.

On chip trimming results in high output voltage accuracy (+/-2%). Accuracy is kept over a wide temperature range, line and load variation.

The maximum input voltage is 40 V. The max output current is internally limited. An internal temperature protection disables the voltage regulator output.

Features

Max DC supply voltage	V_S	40V
Max output voltage tolerance	ΔV_O	+/-2%
Max dropout voltage	V_{dp}	500 mV
Output current	I_o	300 mA
Quiescent current	I_{qn}	55 $\mu\text{A}^{(1)}$

1. Typical value.



- AEC-Q100 qualified
- Operating DC supply voltage range 5.6 V to 40 V
- Low dropout voltage
- 300 mA current capability
- Low quiescent current
- Very low consumption mode
- Precision output voltage 5 V +/- 2 %
- Reset circuit sensing the output voltage

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PPAK	L5300RPT	L5300RPTTR

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1 Block diagram and pins description

Figure 1. Block diagram

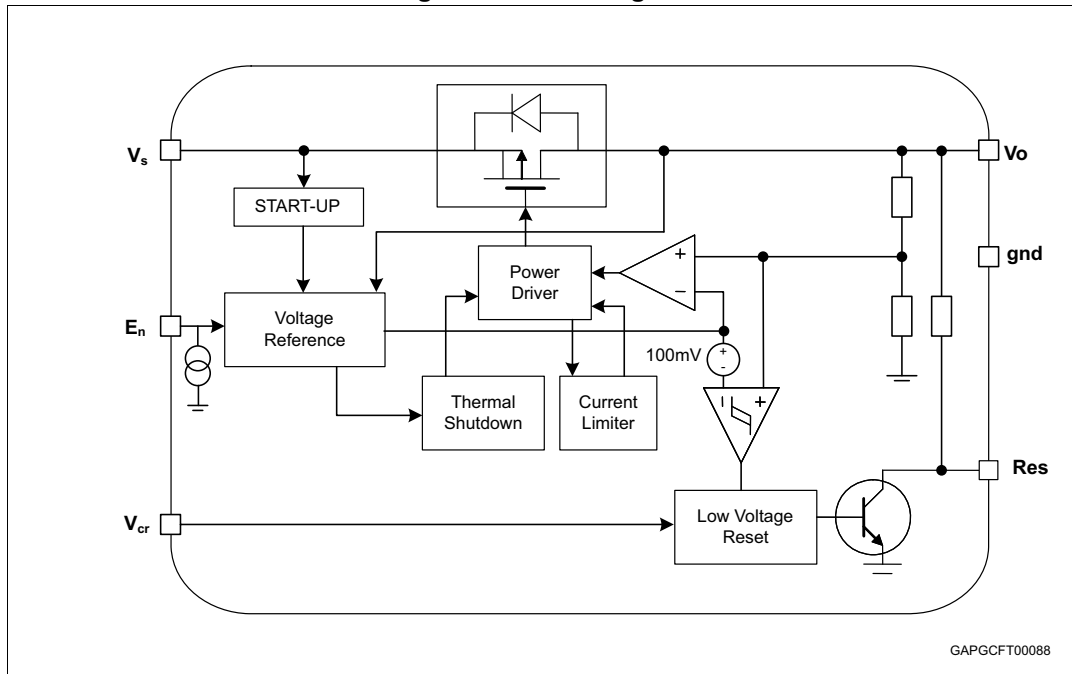
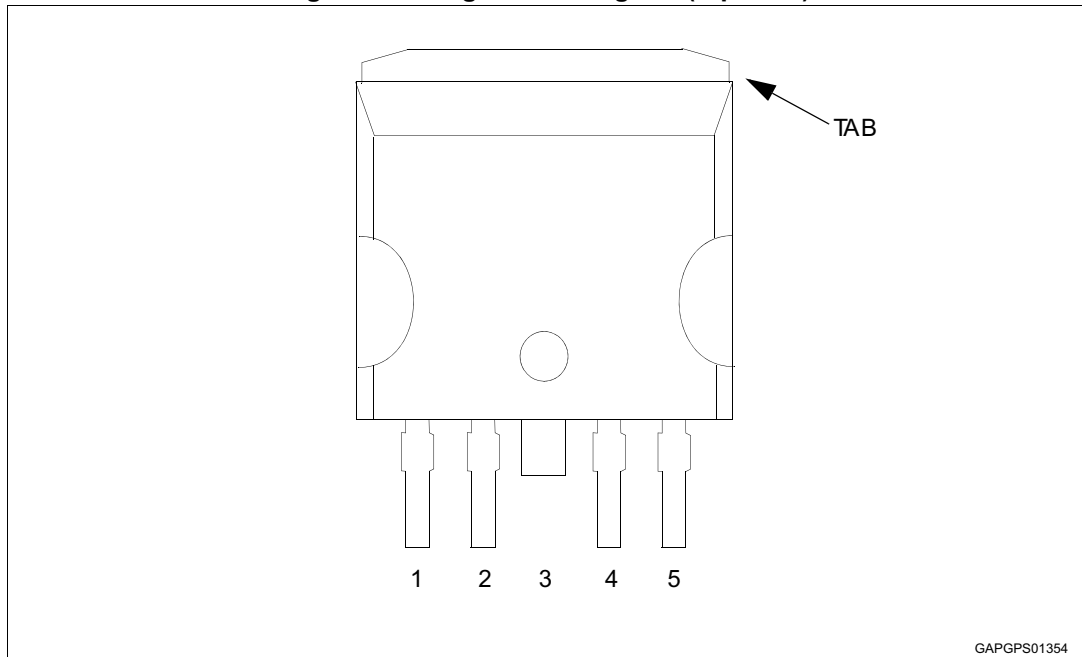


Figure 2. Configuration diagram (top view)



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Table 2. Pins description

N°	Name	Function
1	V_S	Supply voltage, block directly to GND on the IC with a capacitor.
2	R_{es}	Reset output. Internally connected to V_o through a 20 K Ω pull up resistor. This pin is pulled low when $V_o < V_{o_th}$. Keep open if not needed.
3	GND	Ground is internally electrically connected to TAB.
4	V_{cr}	Reset delay. Connect an external capacitor between V_{cr} pin and ground to adjust the reset delay time. Keep open if not needed.
5	V_o	5 V regulated output. Block to GND with a ceramic capacitor (≥ 220 nF for regulator stability).

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{sdc}	DC supply voltage	-0.3 to 40	V
I_{sdc}	Input current	Internally limited	
V_{odc}	DC output voltage	-0.3 to 6	V
I_{odc}	DC output current	Internally limited	
$V_{od Res}$	Open drain output voltage R_{es}	-0.3 to $V_{Vodc} + 0.3$	V
$I_{od Res}$	Open drain output current R_{es}	Internally limited	
V_{cr}	V_{cr} voltage	-0.3 to $V_{Vo} + 0.3$	V
T_j	Junction temperature	-40 to 150	°C
$V_{ESD HBM}$	ESD HBM voltage level (HBM-MIL STD 883C)	+/- 2	kV
$V_{ESD CDM}$	ESD CDM voltage level (CDM- AEC-Q100-011)	+/- 750	V

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction to case	5	°C/W
$R_{thj-amb}$	Thermal resistance junction to ambient	45.5	°C/W

2.3 Electrical characteristics

Values specified in this section are for $V_S = 5.6 \text{ V}$ to 31 V , $T_j = -40 \text{ }^\circ\text{C}$ to $+150 \text{ }^\circ\text{C}$ unless otherwise stated.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_o	V_{o_ref}	Output voltage	$V_S = 8 \text{ V}$ to 18 V $I_o = 8 \text{ mA}$ to 300 mA	4.9	5.0	5.1	V
V_o	V_{o_ref}	Output voltage	$V_S = 5.6 \text{ V}$ to 31 V $I_o = 8 \text{ mA}$ to 300 mA	4.85	5.0	5.15	V
V_o	V_{o_ref}	Output voltage	$V_S = 5.6 \text{ V}$ to 31 V $I_o = 0.1 \text{ mA}$ to 8 mA	4.75	5.0	5.25	V
V_o	I_{short}	Short-circuit current	$V_S = 13.5 \text{ V}$	0.8	1.8	2.6	A
V_o	I_{lim}	Output current capability ⁽¹⁾	$V_S = 13.5 \text{ V}$	0.6	1.6	2.5	A
V_S, V_o	V_{line}	Line regulation voltage	$V_S = 6 \text{ V}$ to 28 V $I_o = 50 \text{ mA}$			40	mV
V_o	V_{load}	Load regulation voltage	$V_S = 13.5 \text{ V}$ $I_o = 8 \text{ mA}$ to 300 mA $T_j = 25 \text{ }^\circ\text{C}$			40	mV
			$V_S = 8 \text{ V}$ to 18 V $I_o = 8 \text{ mA}$ to 300 mA			55	
V_S, V_o	V_{dp}	Drop voltage ⁽²⁾	$I_o = 300 \text{ mA}$			500	mV
V_S, V_o	SVR	Ripple rejection	$f_r = 100 \text{ Hz}$ ⁽³⁾		60		dB
V_o	I_{oth_H}	Normal consumption mode output current	$V_S = 8 \text{ V}$ to 18 V	8			mA
V_o	I_{oth_L}	Very low consumption mode output current	$V_S = 8 \text{ V}$ to 18 V			1.1	mA
V_o	I_{oth_Hyst}	Output current switching threshold hysteresis	$V_S = 13.5 \text{ V}$ $T_j = 25 \text{ }^\circ\text{C}$		0.8		mA
V_S, V_o	I_{qn_1}	Current consumption with regulator enabled $I_{qn_1} = I_{V_S} - I_o$	$V_S = 13.5 \text{ V}$, $I_o = 0.1 \text{ mA}$ to 1 mA ,		55	80	μA
V_S, V_o	I_{qn_300}	Current consumption with regulator enabled $I_{qn_300} = I_{V_S} - I_o$	$V_S = 13.5 \text{ V}$, $I_o = 300 \text{ mA}$,		3	4.2	mA
	T_w	Thermal protection temperature		150		190	$^\circ\text{C}$
	T_{w_hy}	Thermal protection temperature hysteresis			10		$^\circ\text{C}$

1. Measured output current when the output voltage has dropped 100 mV from its nominal value obtained at 13.5 V and $I_o = 75 \text{ mA}$.
2. $V_S - V_o$ measured dropout when the output voltage has dropped 100 mV from its nominal value obtained at 13.5V and $I_o = 75 \text{ mA}$.
3. Guaranteed by design.

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
R _{es}	V _{Res_l}	Reset output low voltage	R _{ext} = 5 kΩ V _o > 1 V			0.4	V
R _{es}	I _{Res_lkg}	Reset output high leakage current	V _{Res} = V _o			1	μA
R _{es}	R _{Res}	Pull up internal resistance	Versus V _o	10	20	40	kΩ
R _{es}	V _{o_th}	V _o out of regulation threshold	V _o decreasing	6	8	10	% below V _{o_ref}
V _{cr}	V _{Rlth}	Reset timing low threshold	V _S = 13.5 V	16	19	22	% V _{o_ref}
V _{cr}	V _{Rhth}	Reset timing high threshold	V _S = 13.5 V	47	50	53	% V _{o_ref}
V _{cr}	I _{cr}	Charge current	V _S = 13.5 V	10	20	30	μA
V _{cr}	I _{dr}	Discharge current	V _S = 13.5 V	10	20	30	μA
R _{es}	t _{rr}	Reset reaction time	V _o = V _{o_th} - 100 mV			2	μs
R _{es}	t _{rd}	Reset delay time	V _S = 13.5 V, C _{tr} = 1 nF	2	4	6	ms

2.4 Electrical characteristics curves

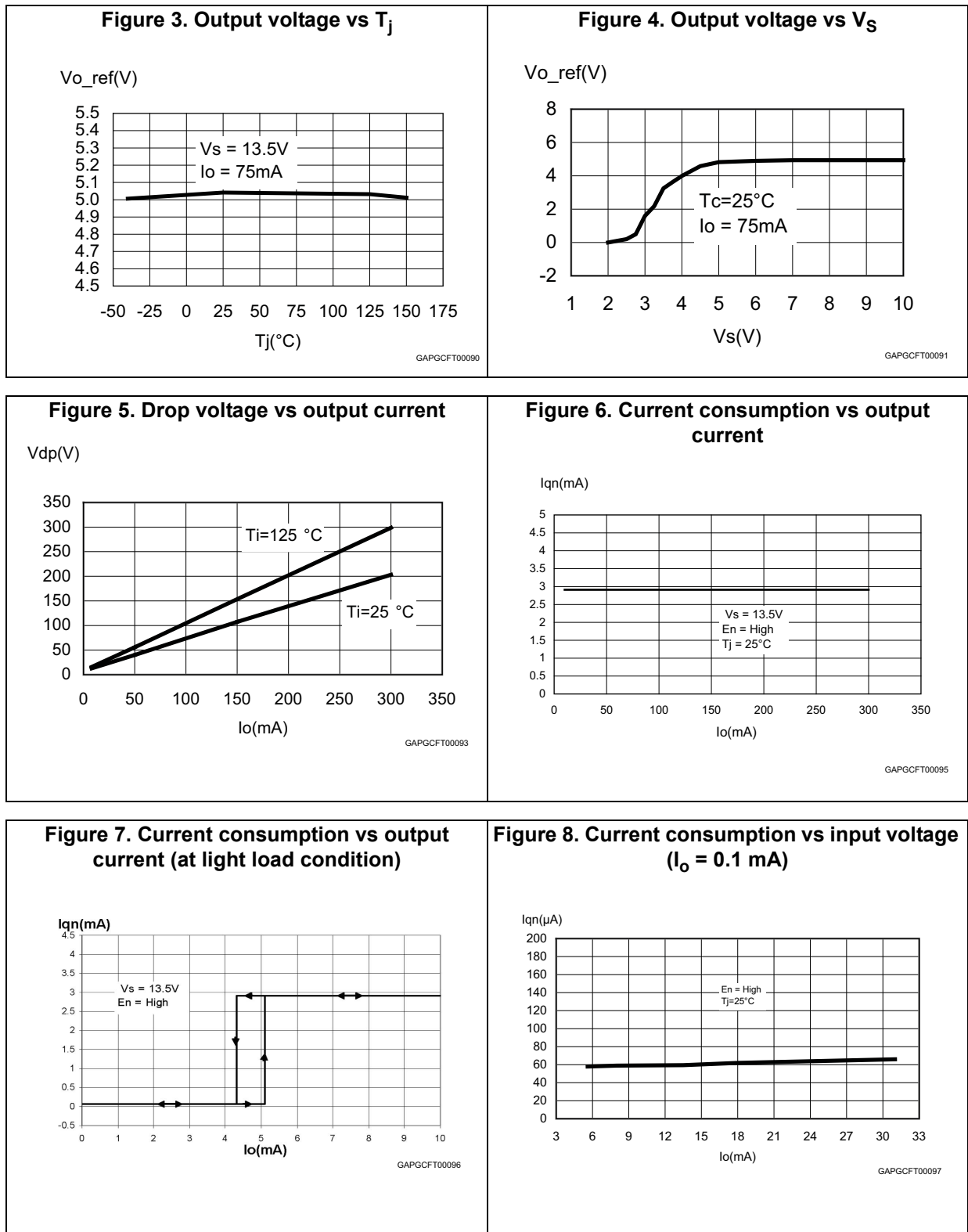
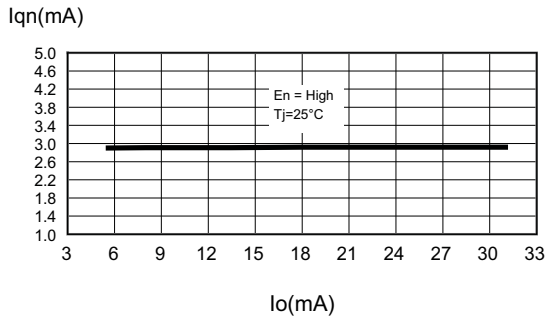
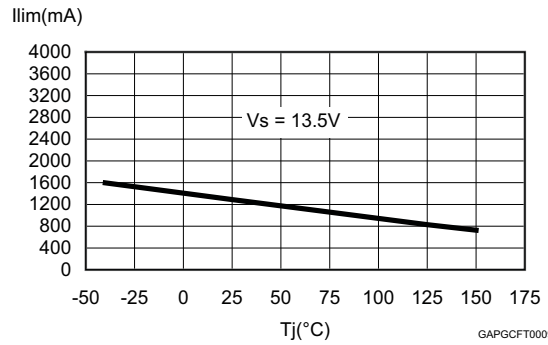


Figure 9. Current consumption vs input voltage
($I_o = 100\text{ mA}$)



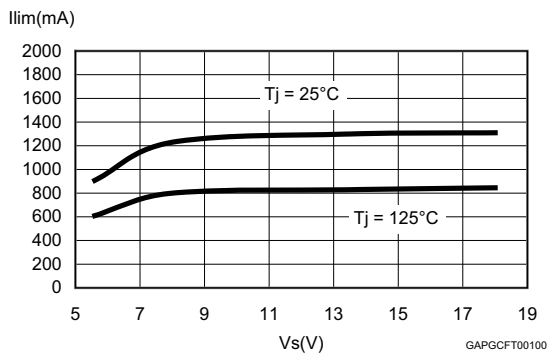
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Figure 10. Current limitation vs T_j



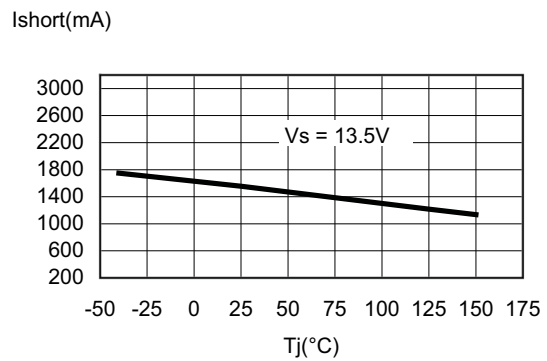
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Figure 11. Current limitation vs input voltage



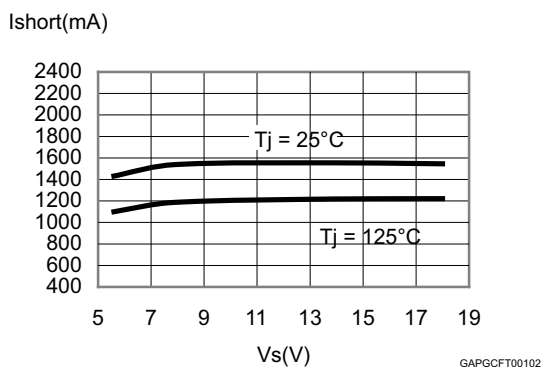
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Figure 12. Short-circuit current vs T_j



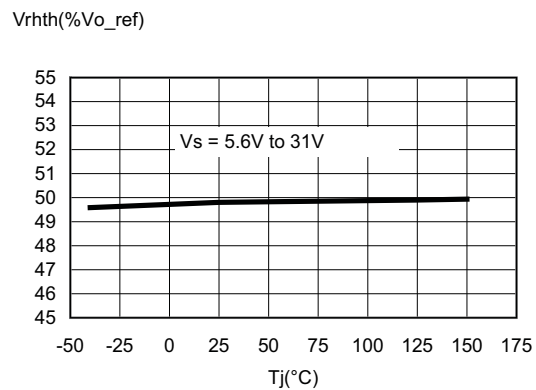
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Figure 13. Short-circuit current vs input voltage

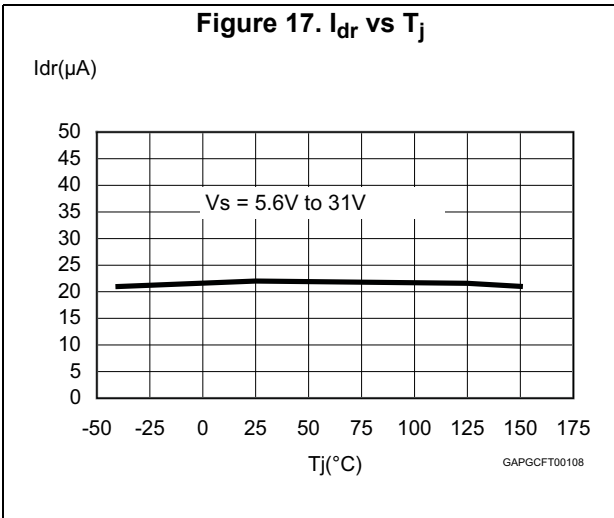
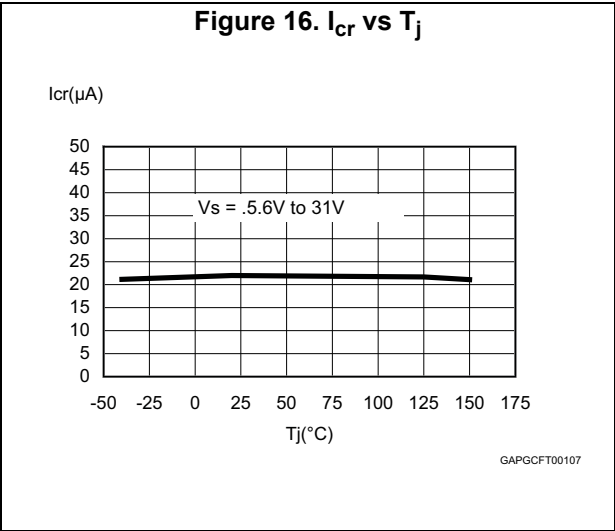
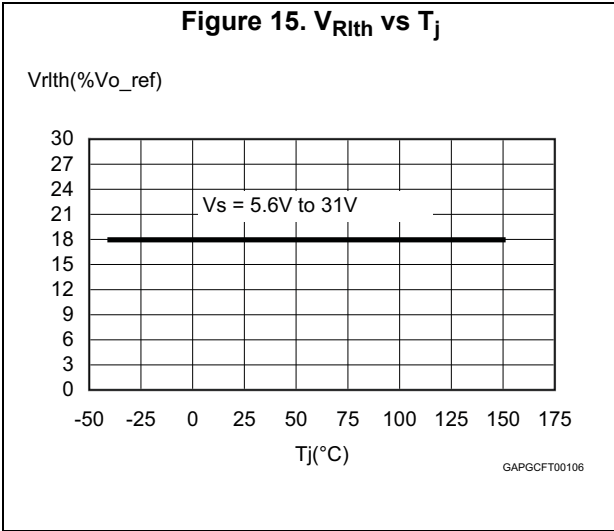


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Figure 14. V_{Rth} vs T_j



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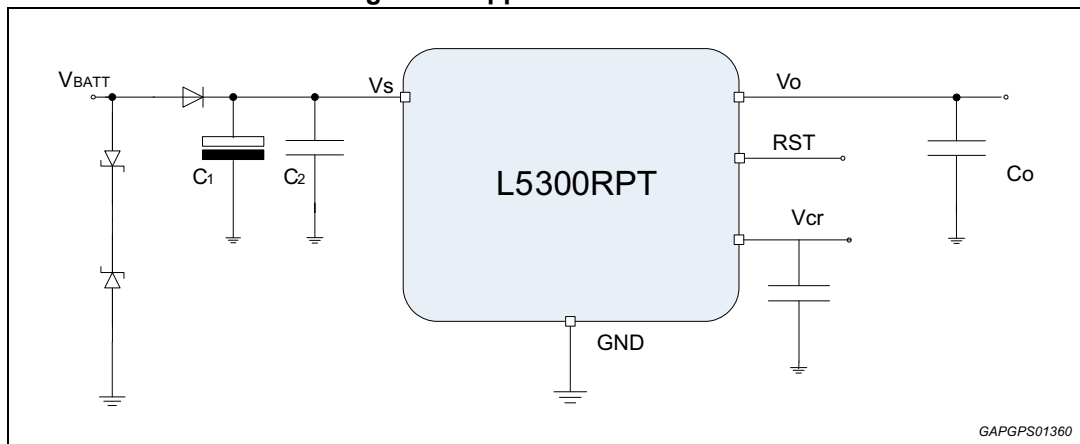


3 Application information

3.1 Voltage regulator

The voltage regulator uses a p-channel mos transistor as a regulating element. With this structure a very low dropout voltage at current up to 300 mA is obtained. The output voltage is regulated up to input supply voltage of 40 V. The high-precision of the output voltage ($\pm 2\%$) is obtained with a pre-trimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions the quiescent current goes down to 55 μA only (low consumption mode). This procedure features a certain hysteresis on the output current (see [Figure 7](#)). Short-circuit protection to GND and a thermal shutdown are provided.

Figure 18. Application schematic



The input capacitor $C_1 \geq 100 \mu\text{F}$ is necessary as backup supply for negative pulses which may occur on the line. The second input capacitor $C_2 \geq 220 \text{ nF}$ is needed when the C_1 is too distant from the V_S pin and it compensates smooth line disturbances. The C_O ceramic capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations. Suggested value is $C_O = 220 \text{ nF}$ with $\text{ESR} \geq 100 \text{ m}\Omega$.

Stability region is reported in [Figure 19](#).

Figure 19. Stability region

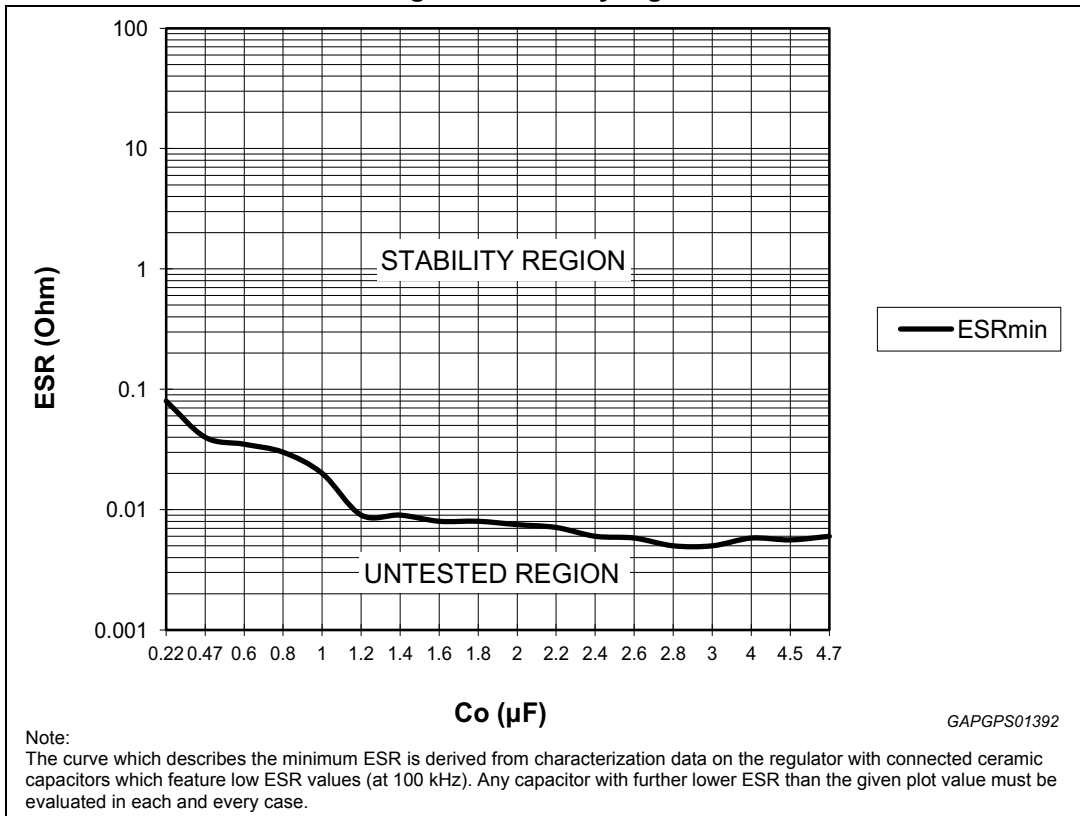
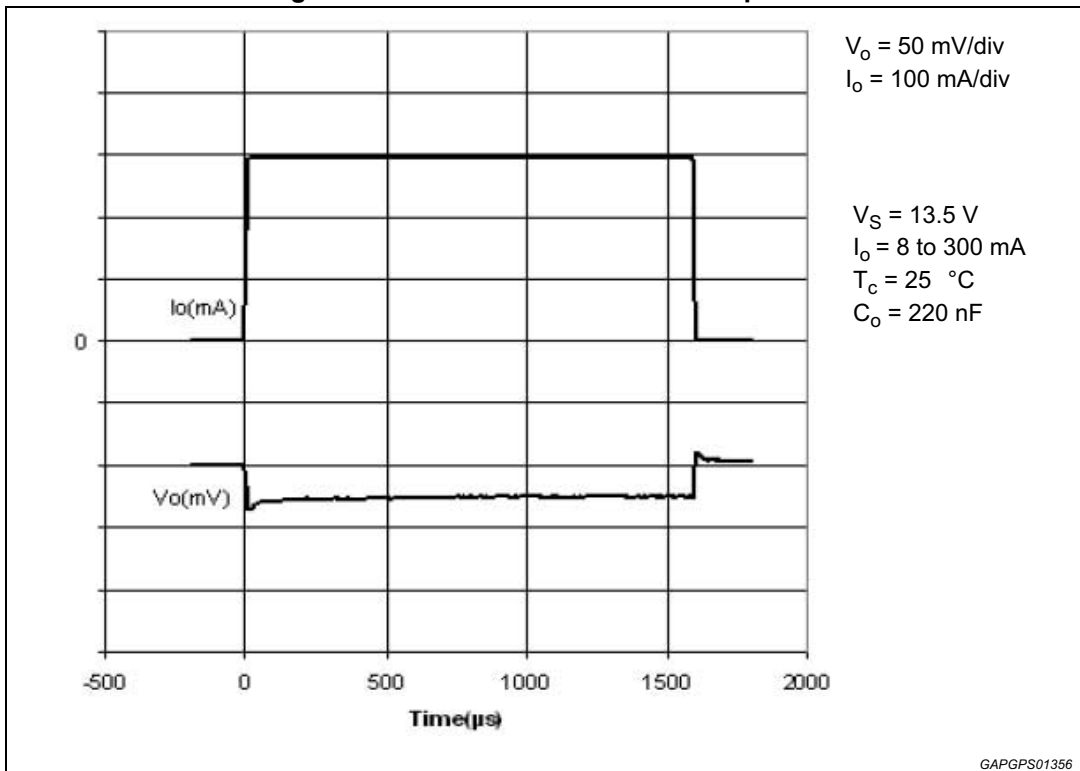


Figure 20. Maximum load variation response



3.2 Reset

The reset circuit monitors the output voltage V_o . If the output voltage becomes lower than V_{o_th} then R_{es} goes low with a delay time (t_{rr}). When the output voltage becomes higher than V_{o_th} then R_{es} goes high with a delay time t_{rd} . This delay is obtained by 32 periods of oscillator. The oscillator period is given by:

Equation 1

$$T_{osc} = [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{cr} + [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{dr}$$

and reset pulse delay t_{rd} is given by:

Equation 2

$$t_{rd} = 32 \times T_{osc}$$

Where:

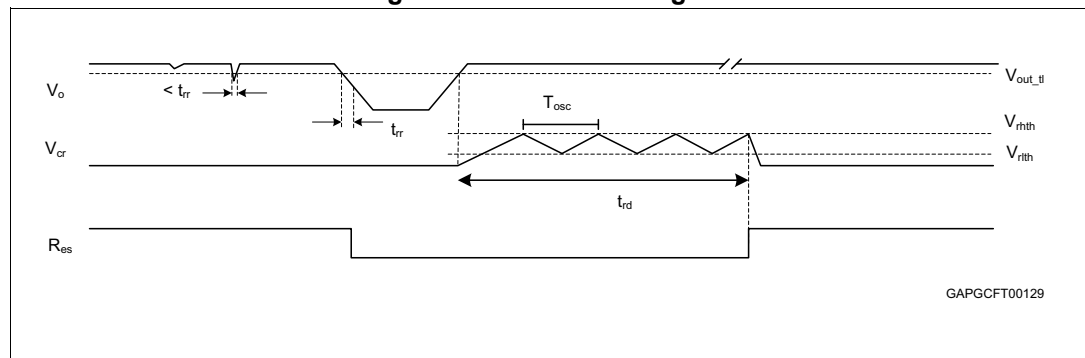
$I_{cr} = 20 \mu A$ is an internally generated charge current,

$I_{dr} = 20 \mu A$ is an internally generated discharge current,

$V_{Rhth} = 2.5 V$ (typ) and $V_{Rlth} = 0.95V$ (typ) are two voltage thresholds,

C_{tr} is an external capacitor put between V_{cr} pin and GND.

Figure 21.Reset time diagram



4 Package and PCB thermal data

Figure 22.PPAK PC board

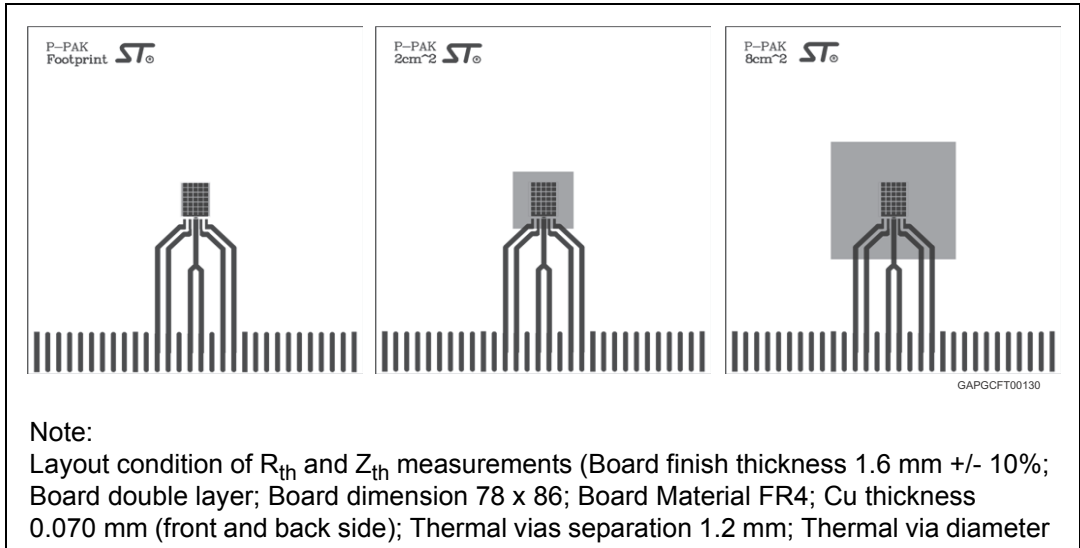


Figure 23. $R_{thj-amb}$ vs PCB copper area in open box free air condition

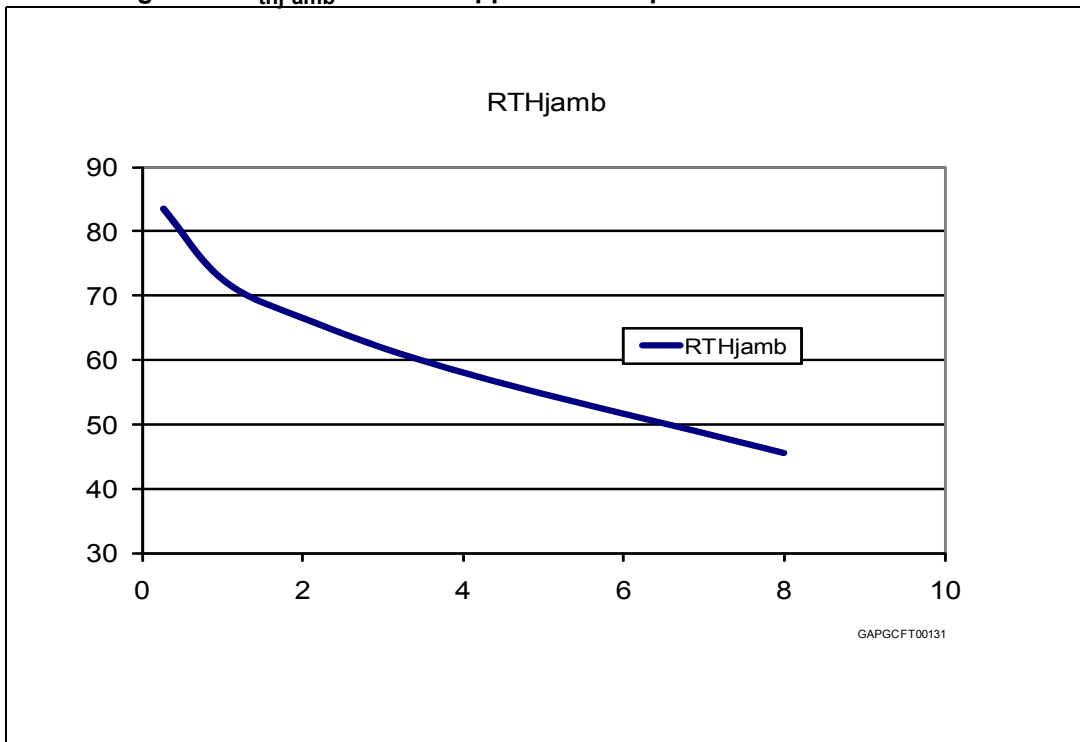
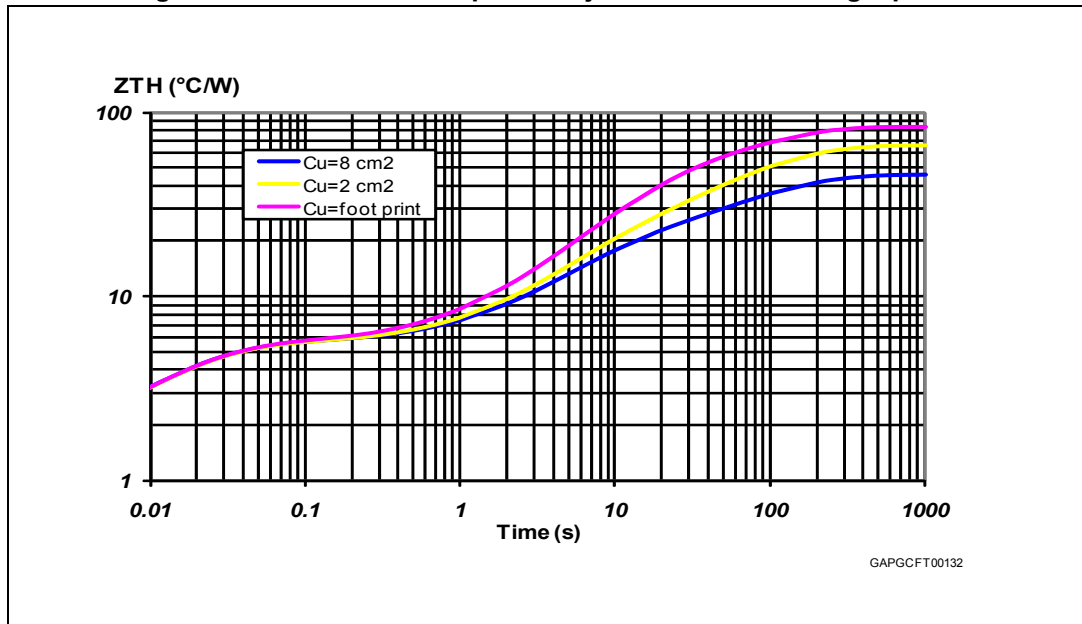


Figure 24.PPAK thermal impedance junction ambient single pulse



Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 25.Thermal fitting model of a Vreg in PPAK

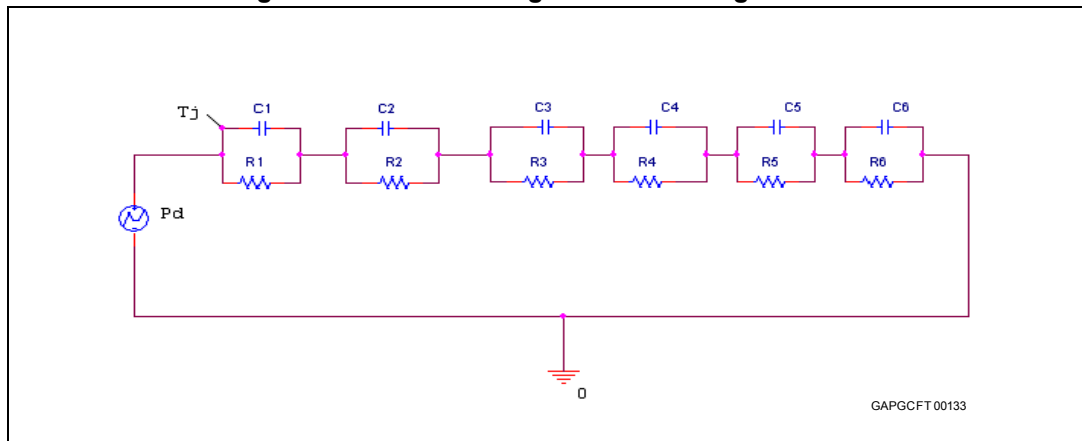


Table 7. PPAK thermal parameter

Area (cm ²)	Footprint	4	8
R1 (°C/W)	1.2		
R2 (°C/W)	1.8		
R3 (°C/W)	2.5		
R4 (°C/W)	14	12	12
R5 (°C/W)	28	22	12
R6 (°C/W)	36	27	16
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.005		
C3 (W.s/°C)	0.01		
C4 (W.s/°C)	0.6	0.6	0.6
C5 (W.s/°C)	0.8	2	4
C6 (W.s/°C)	3	5	9

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 PPAK mechanical data

Figure 26.PPAK dimension

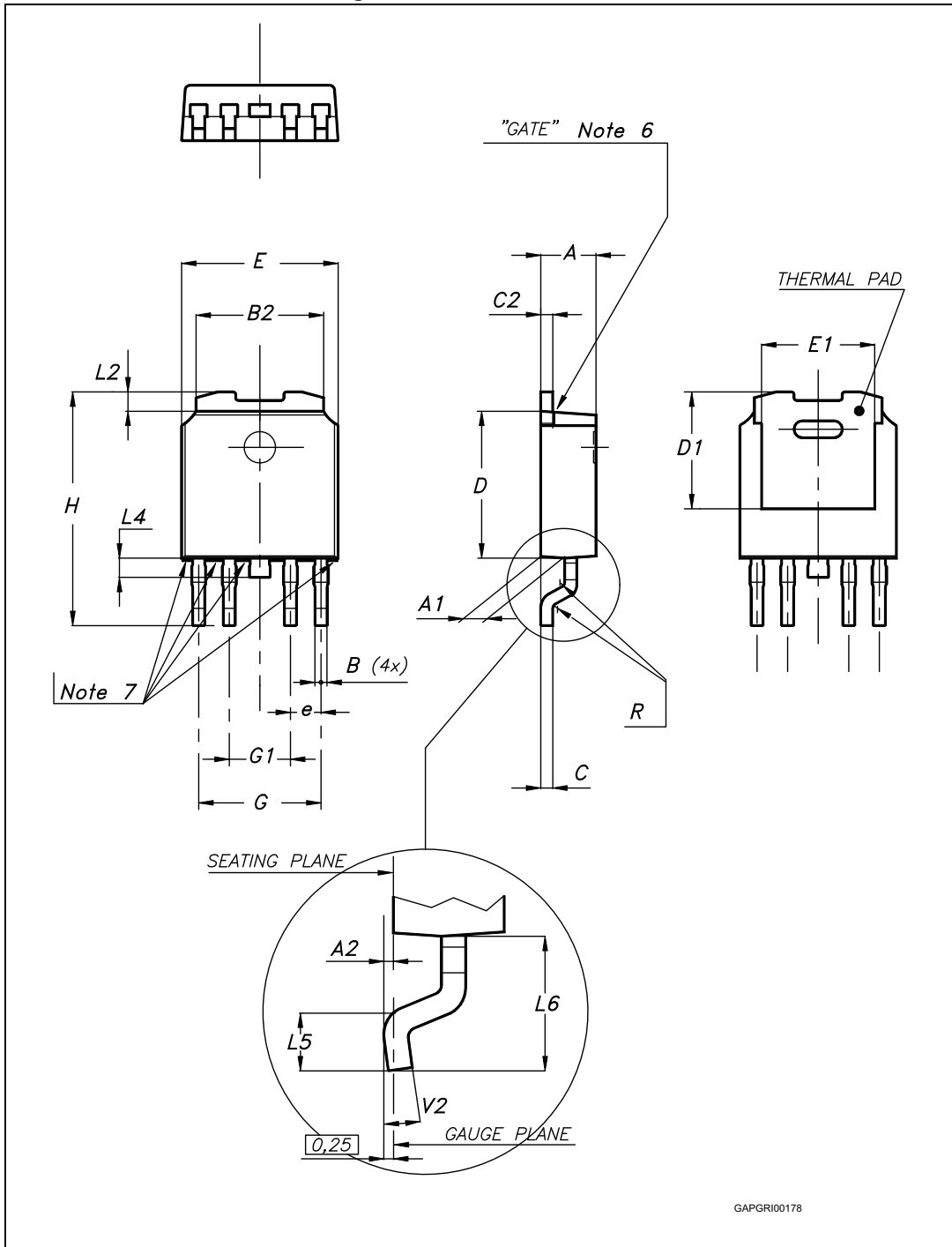


Table 8. PPAK mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
L5	1.00		
L6		2.80	
R		0.2	
V2	0°		8°
Package weight	Gr. 0.3		

5.3 PPAK packing information

Figure 27.PPAK suggested pad layout and tube shipment (no suffix)

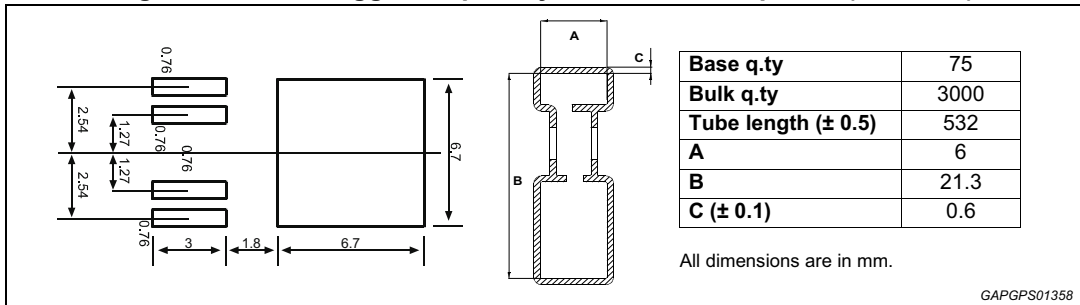
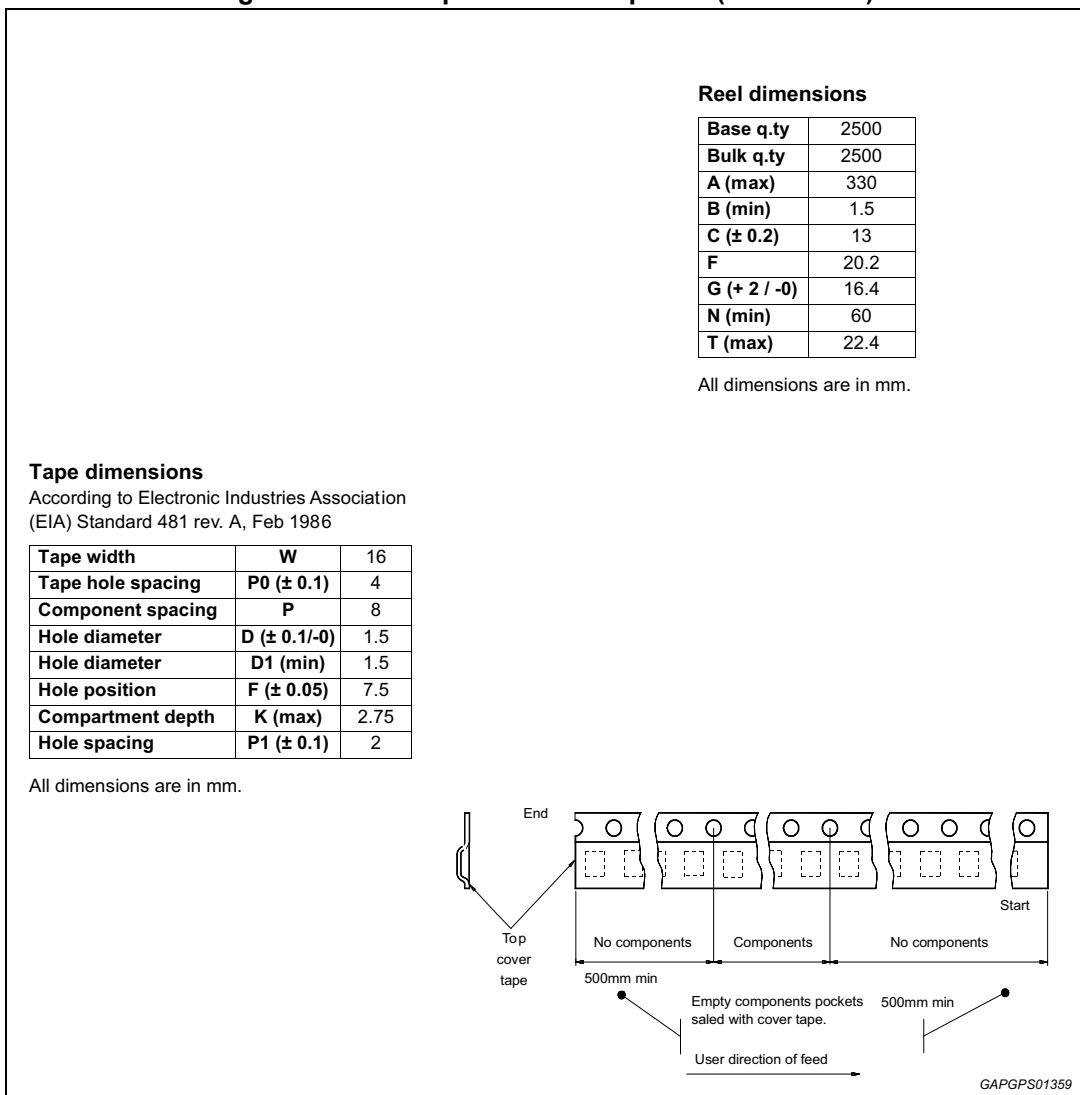


Figure 28.PPAK tape and reel shipment (suffix “TR”)



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Jul-2007	1	Initial release.
09-Aug-2007	2	Table 6: Reset - reset reaction time note deleted. Section 3.2 updated
16-Mar-2009	3	Changed features table on the cover page Table 5: General – V_{O_ref} : deleted row and added 3 new rows Table 6: Reset – I_{Res_lkg} : deleted Test condition – V_{O_th} : deleted $I_o = 1$ to 300 mA and $V_S = 5.6$ to 31V, added “ V_o decreasing” for Test condition – V_{Rlth} : changed min/typ/max values – T_{rd} : changed min/typ/max values Section 3.2: Reset – t_{rd} : changed coefficient – V_{Rlth} : changed coefficient

Table 9. Document revision history (continued)

Date	Revision	Changes
20-Sep-2010	4	<p>Changed the title of the document</p> <p><i>Features</i> in cover page</p> <ul style="list-style-type: none"> – Changed typical quiescent current value in table from 60 μA to 55 μA <p><i>Description</i> in cover page</p> <ul style="list-style-type: none"> – Changed typical quiescent current value from 60 μA to 55 μA – Changed dropped current value from 10 μA to 5 μA <p><i>Table 2: Pins description</i></p> <ul style="list-style-type: none"> – Updated pins sequence <p><i>Table 3: Absolute maximum ratings</i></p> <ul style="list-style-type: none"> – I_{SDC}: changed symbol from I_{VSDC} – I_{ODC}: changed symbol from I_{VODC} – $V_{ESD\ CDM}$: added standard for parameter <p>Updated <i>Table 4: Thermal data</i></p> <p><i>Table 5: General</i></p> <ul style="list-style-type: none"> – I_{short}: changed min/typ/max value – I_{lim}: changed min/typ/max value, changed parameter – V_{line}: changed test condition – V_{load}: changed test condition, added new spec. – SVR: deleted min value, added typ value – I_{qn_300}: changed typ/max value – I_{oth_H}, I_{oth_L}, I_{oth_Hyst}: added new rows – Updated all table footnote <p><i>Table 6: Reset</i></p> <ul style="list-style-type: none"> – V_{Res_I}: changed test condition – V_{Res_Ikg}: added test condition <p><i>Section 3.2: Reset</i></p> <ul style="list-style-type: none"> – Changed text <p>Deleted Figure 3: Behavior of output current versus regulated voltage V_o</p> <p>Added <i>Section 2.4: Electrical characteristics curves</i></p> <p>Added <i>Chapter 4: Package and PCB thermal data</i></p>
12-Oct-2010	5	Updated <i>Section 3.1: Voltage regulator</i>
27-Jan-2012	6	Updated <i>Figure 19: Stability region on page 14.</i>
07-Feb-2012	7	Modified <i>Figure 19: Stability region on page 14.</i>
04-May-2012	8	Updated <i>Figure 26: PPAK dimension on page 20</i> and <i>Table 8: PPAK mechanical data.</i>
19-Sep-2013	9	Updated Disclaimer.
20-Sep-2018	10	Updated template. Updated title and added the feature "AEC-Q100 qualified" in cover page.

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