14 GHz Divide-by-8 to 511 Programmable Integer Divider

Features

- Wide Operating Range: DC – 14 GHz
- Contiguous Divide Ratios: 8 to 511
- Large Output Swings: >1 Vpp/side
- Single-Ended and/or Differential Drive
- Size: 6mm x 6mm
- Parallel Control Lines
- Low SSB Phase Noise:
  - 147 dBc @ 10 kHz Offset

Description

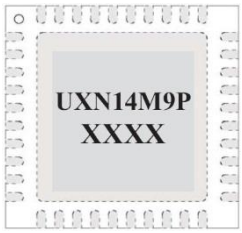
The UXN14M9P is a highly programmable integer divider covering all integer divide ratios between 8 and 511. The device features single-ended or differential inputs and outputs. Parallel control inputs are CMOS and LVTTL compatible for ease of system integration. The UXN14M9P is packaged in a 40-pin, 6mm x 6mm leadless plastic surface mount package.

Application

The UXN14M9P can be used as a general purpose, highly configurable, divider in a variety of high frequency synthesizer applications. Fast switching combined with a wide range of divide ratios make the UXN14M9P an excellent choice for fractional-N and integer-N PLLs. Fractional division may be achieved by applying a sequence to the divider control lines, such as a delta-sigma modulated sequence.

Pad Metallization

The QFN package pad metallization consists of a 300-800 micro-inch (typical thickness 435 micro-inch or 11.04um) 100% matte Sn plate. The plating covers a Cu (C194) leadframe. The packages are manufactured with a >1hr 150C annealing/heat treating process, and the matte (non-glossy) plating, specifically to mitigate tin whisker growth.



Key Specifications (T = 25˚C):
Vee = -3.3 V, Iee = 340 mA, Zo=50 Ω

Parameter	Description	Min	Typ	Max
Fin (GHz)	Input Frequency	DC*	-	14
Pin (dBm)	Input Power	-	0	+10
Pout (dBm)	Output Power	-	+4	-
PDC (W)	DC Power Dissipation	-	1.1	-
θjc (ºC/W)	Junction-Case Thermal Resistance	-	14	-

** Low frequency limit dependent on input edge speed*

Frequency Divider Application

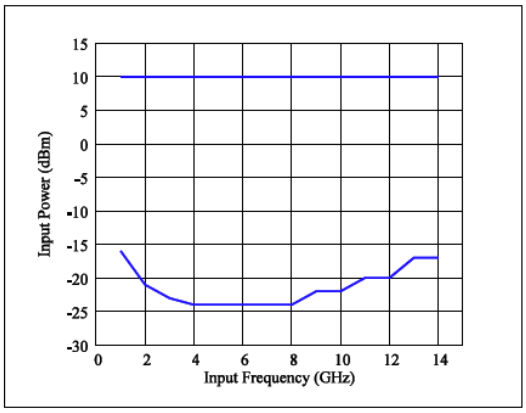


Figure 1: *Min/Max Single-Ended Input Power Input Sensitivity Window*

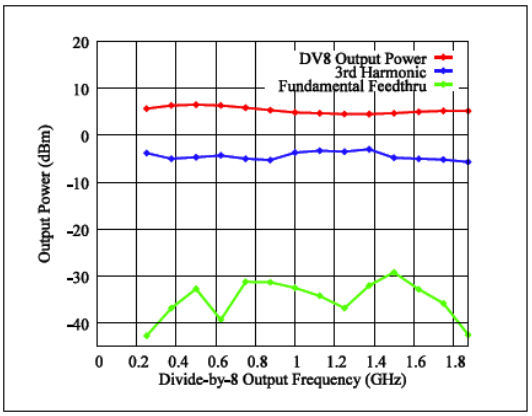
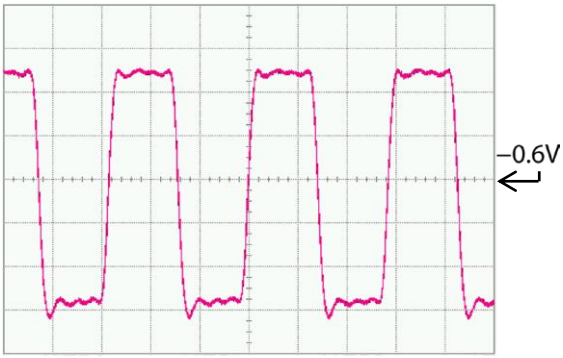
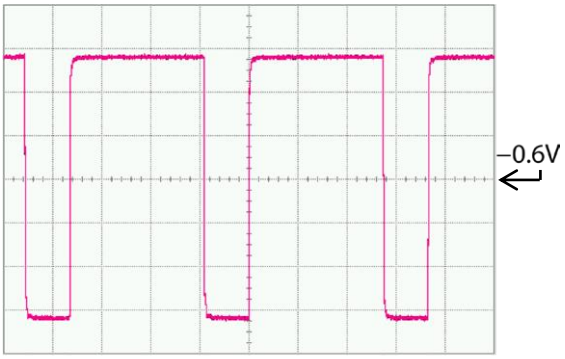


Figure 2: *Divide-by-8 Output Power, 3rd Harmonic & Input Feedthru*



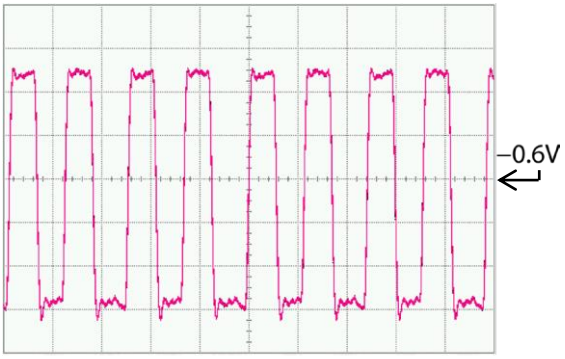
200 ps/DIV, 200mV/DIV

Figure 3: *Static Divide-by-8 Configuration Input Freq = 14 GHz*



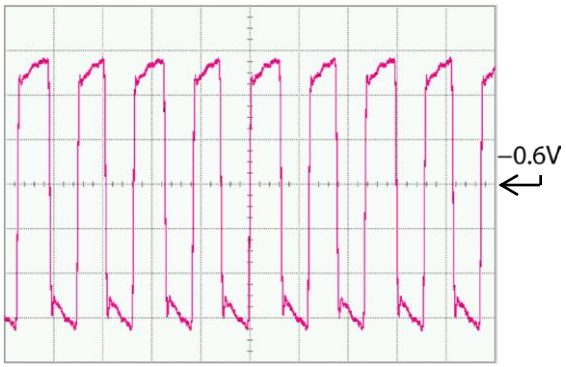
10 ns/DIV, 200mV/DIV

Figure 4: *Static Divide-by-511 Configuration Input Freq = 14 GHz*



500 ps/DIV, 200mV/DIV

Figure 5: *Dynamic Divide-by-8/9 Application Input Freq = 14 GHz*



1 ns/DIV, 200mV/DIV

Figure 6: *Dynamic Divide-by-16/17 Application Input Freq = 14 GHz*

Functional Block Diagram

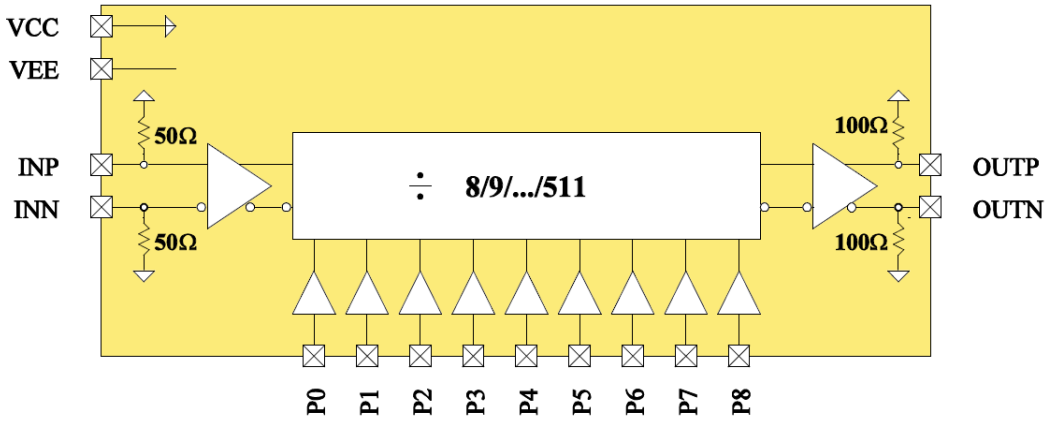


Figure 7: *Functional Block Diagram*

Table 1: Pin Description

Port Name	Description	Notes
INP	Divider Input, Positive Terminal	CML signal levels
INN	Divider Input, Negative Terminal	CML signal levels
OUTP	Divider Output, Positive Terminal	CML signal levels
OUTN	Divider Output, Negative Terminal	CML signal levels
P0-P8	Divider Modulus Control (P8=MSB)	CMOS levels, see Equation 1, defaults to logic 0
Vcc	RF & DC Ground	The paddle is connected to +Vcc inside the package
Vee	-3.3 V @ 340 mA	Negative Supply Voltage

Equation 1:

$$\text{Divider Modulus} = N = P_0 \cdot 2^0 + P_1 \cdot 2^1 + P_2 \cdot 2^2 + \ldots + P_8 \cdot 2^8 \qquad \text{for } 8 \le N \le 511$$

Table 2: CMOS Levels for control line P0-P8

Logic Level	Minimum	Typical	Maximum
1 (High)	Vcc-1.25 V	Vcc-0.8V	Vcc-0.8V
0 (Low)	Vee	Vee	Vee+1.25 V

Simplified Control Logic Schematic

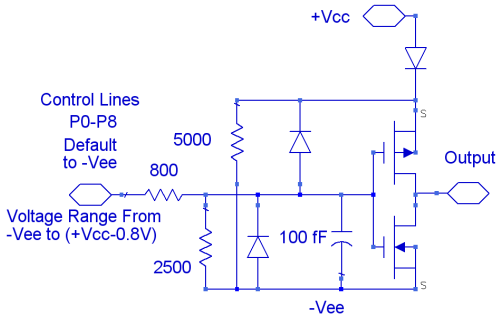


Figure 8: *Simplified Control Logic Schematic*

Application Notes

Low Frequency Operation:

Low frequency operation is limited by external bypass capacitors and the slew rate of the input clock. The next paragraph shows the calculations for the bypass capacitors. If DC coupled, the device operates down to DC for square-wave inputs. Sine-wave inputs are limited to ~50 MHz due to the 10 dBm max input power limitation.

The values of the coupling capacitors for the high-speed inputs and outputs (I/O's) are determined by the lowest frequency the IC will be operated at.

$$C >> \frac{1}{2 \bullet \pi \bullet 50\Omega \bullet f_{lowest}}$$

For example to use the device below 30 kHz, coupling capacitors should be larger than 0.1uF.

IC Assembly:

The device is designed to operate with either single-ended or differential inputs. Figures 9, 10 & 11 show the IC assembly diagrams for positive and negative supply voltages. In either case the supply should be capacitively bypassed to the ground to provide a good AC ground over the frequency range of interest. The backside of the chip should be connected to a good thermal heat sink.

All RF I/O's are connected to VCC through on-chip termination resistors. This implies that when VCC is not DC grounded (as in the case of positive supply), the RF I/O's should be AC coupled through series capacitors unless the connecting circuit can generate the correct levels through level shifting.

ESD Sensitivity:

Although SiGe IC's have robust ESD sensitivities, preventive ESD measures should be taken while storing, handling, and assembling.

Inputs are more ESD susceptible as they could expose the base of a BJT or the gate of a MOSFET. For this reason, all the inputs are protected with ESD diodes. These inputs have been tested to withstand voltage spikes up to 400V.

Table 3: CML Logic Levels for DC Coupling (T=25 °C) Assuming 50Ω terminations at inputs and outputs

Parameter				Minimum	Typical	Maximum
Input	Differential	{	Logic Input$_{high}$	Vcc	Vcc	Vcc
			Logic Input$_{low}$	Vcc - 0.05 V	Vcc - 0.3 V	Vcc - 1 V
	Single	{	Logic Input$_{high}$	Vcc + 0.05 V	Vcc + 0.3 V	Vcc + 1 V
			Logic Input$_{low}$	Vcc - 0.05 V	Vcc - 0.3 V	Vcc - 1 V
Output	Differential & Single	{	Logic Input$_{high}$	Vcc - 0.9 V	Vcc – 0.6 V	Vcc – 0.5 V
			Logic Input$_{low}$	Vcc – 1.1 V	Vcc – 1.6 V	Vcc – 1.7 V

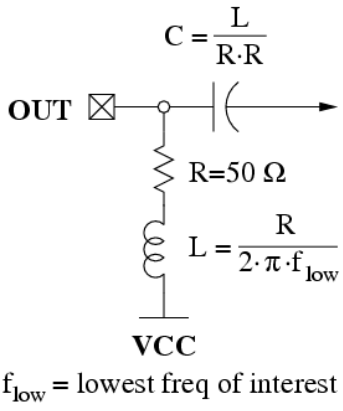
Differential vs. Single-Ended:

The UXN14M9P is fully differential to maximize signal-to-noise ratios for high-speed operation. All high speed inputs and outputs are terminated to Vcc with on-chip resistors (refer to functional block diagram for specific resistor values). The maximum DC voltage on any terminal must be limited to Vcc +/- 1V to prevent damaging the termination resistors with excessive current. Regardless of bias conditions, the following equation should be satisfied when driving the inputs differentially:

$$VCC -1 < VAC/4 + VDC < VCC +1$$

where VAC is the input signal p-p voltage and VDC is common-mode voltage.

The outputs require a DC return path capable of handling ~30mA per side. If DC coupling is employed, the DC resistance of the receiving circuits should be 50 ohms to Vcc. If AC coupling is used, a bias tee circuit should be used such as shown below. The discrete R/L/C elements should be resonance free up to the maximum frequency of operation for broadband applications.



f_{low} = lowest freq of interest

In addition to the maximum input signal levels, single-ended operation imposes additional restrictions: the average DC value of the waveform at IC should be equal to Vcc for single-ended operation. In practice, this is easily achieved with a single capacitor on the input acting as a DC block. The value of the capacitor should be large enough to pass the lowest frequencies of interest.

Note that a potential oscillation mechanism exists if both inputs are static and have identical DC voltages; a small DC offset on either input is sufficient to prevent possible oscillations Connecting a 10k ohm resistor between the unused input and Vee should provide sufficient offset to prevent oscillation.

Negative Supply (DC Coupling)

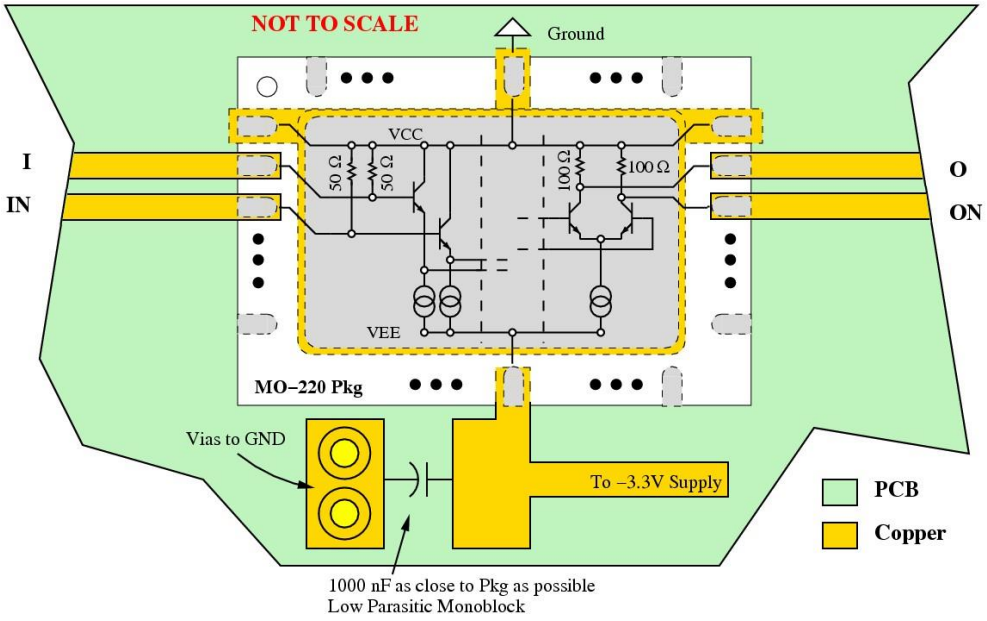


Figure 9: *Negative Supply- DC Coupling*

Negative Supply (AC Coupling)

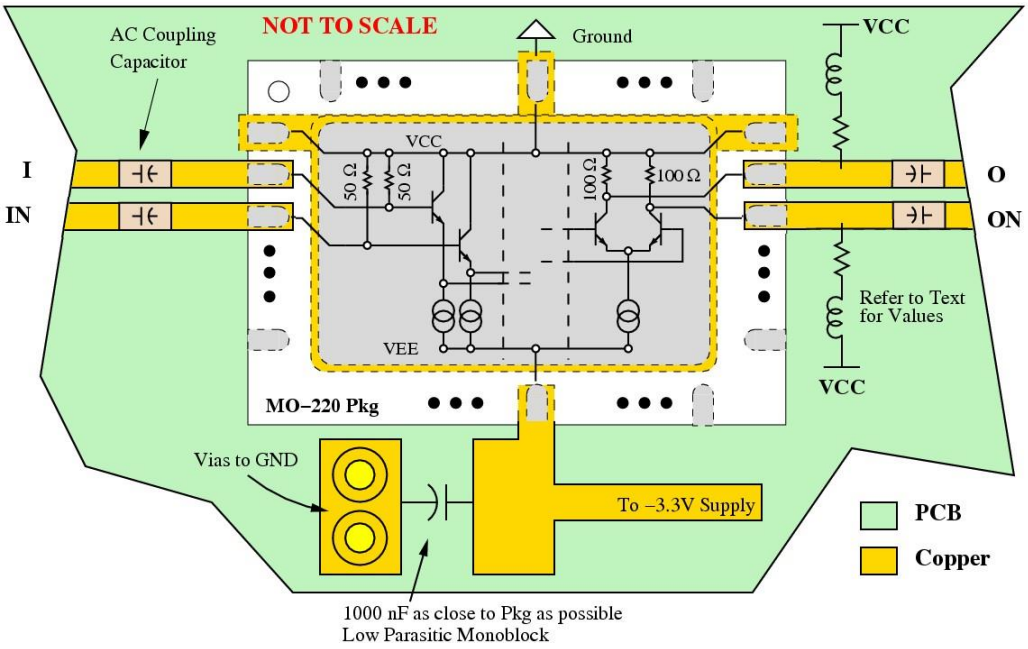


Figure 10: *Negative Supply- AC Coupling*

Differential vs. Single-Ended:

(Note that the metalized backside of the QFN package – the paddle – is internally connected to Vcc, therefore will be at +3.3V potential for the positive supply case. The paddle needs to be soldered to a pad on the pcb to provide heatsinking for the divider; special attention to the pcb design is required to isolate the pcb pad from ground.)

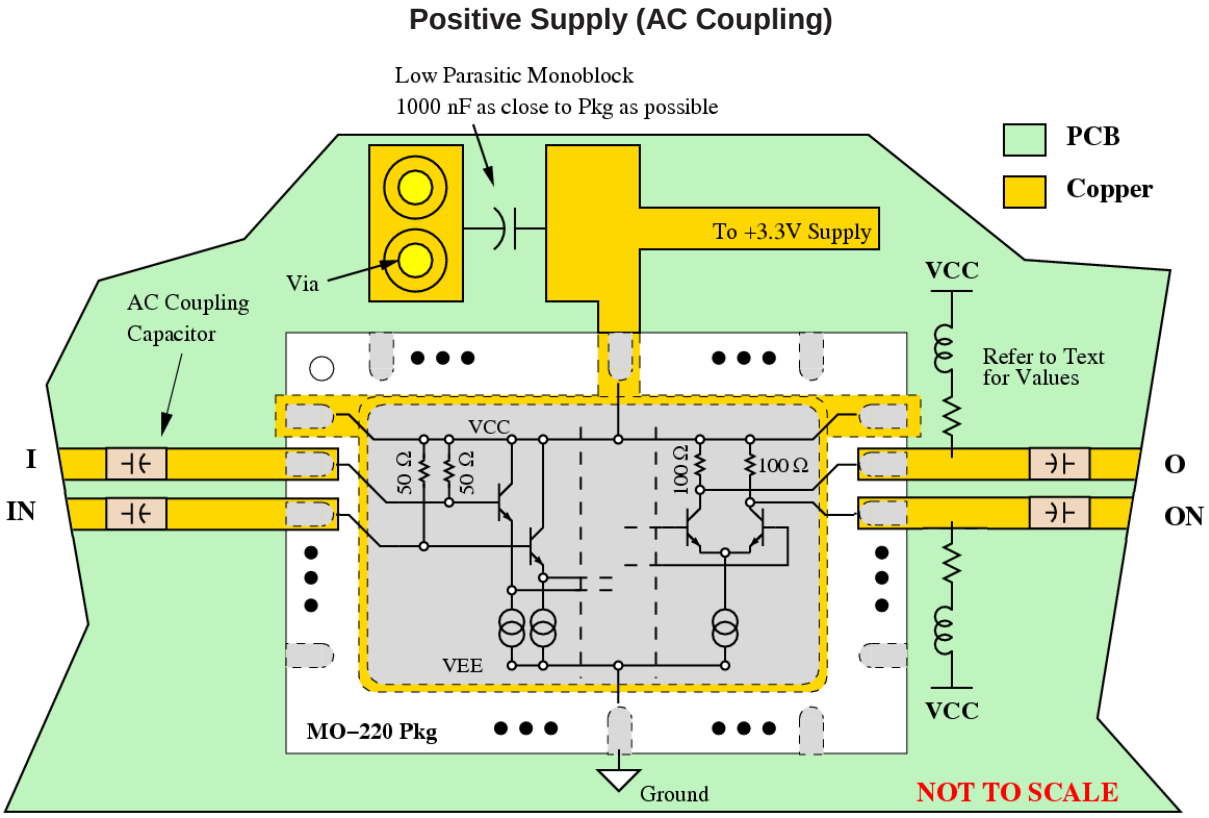


Figure 11: *Positive Supply- AC Coupling*

Duty Cycle:

The UXN14M9P output duty cycle varies between 25% and 64% as a function of the divide ratio. For divide ratios between 16 and 511, the pulse width remains constant in each octave band (e.g. between 128 and 255), and gives a duty cycle of 50% for powers of 2. Thus, the duty cycle is bounded between 25 and 50% for divide ratios between 16 and 511. For divide ratios between 8 and 15, the pulse width does not stay fixed, but varies with the divide ratio. The duty cycle ranges from 33% to 64% for these divide ratios. Table 4 shows pulse width and other necessary information for computing the duty cycle, given the divide ratio. The equation provided below allows calculation of the duty cycle based on the information supplied by the table. A chart below summarizes the duty cycles for all possible divide ratios.

$$\text{Duty Cycle (\%)} = \frac{\text{Pulse Width}}{\text{Divide Ratio}} \text{ x } 100\%$$

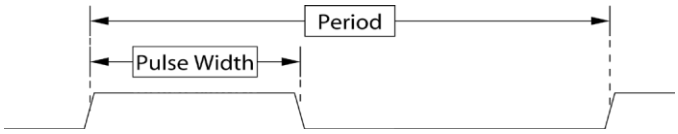
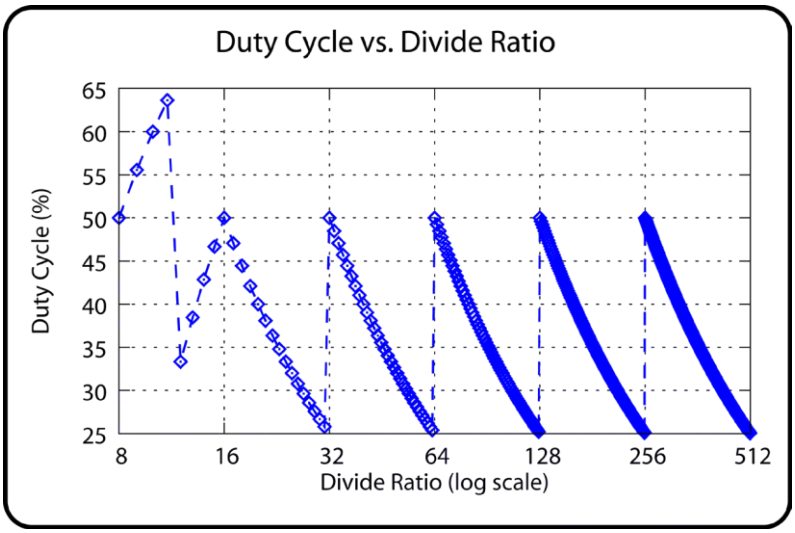


Table 4: Duty Cycle Summary

Divide Ratio	Pulse Width (Input Cycles)	Duty Cycle (%)
8	4	50
9	5	55.6
10	6	60
11	7	63.6
12	4	33.3
13	5	38.5
14	6	42.9
15	7	46.7
16-31	8	50-25
32-63	16	50-25
64-127	32	50-25
128-255	64	50-25
256-511	128	50-25



Application Notes: Frequency Range Selector

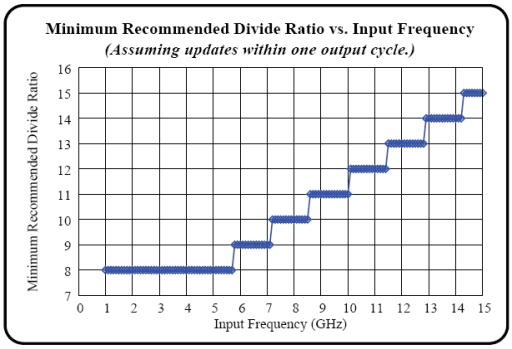
The UXN14M9P achieves contiguous divisions by retiming the input controls for the divide ratio each output cycle. This feature is fitting for applications where the divide ratio requires quick programmability, such as in fractional-N synthesizers. A representative diagram of how the part might be used in such an application is shown below. In this setup the divider output is used to clock (or update) the control circuitry. The polarity of the output edge is chosen by the user depending on the relative timing of the control transistions to the output edge.

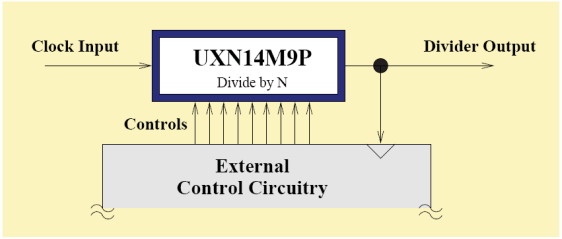
T setup as defined in the timing diagram, is given by the following formula:

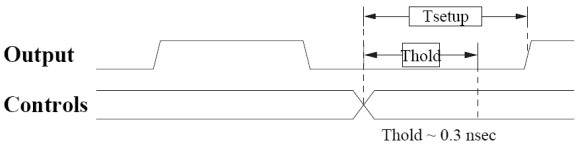
$$T\ setup = 4*Tinput + 0.7nsec$$

where Tinput=input period. Notice that for N=8 and input frequencies above 6 GHz (Tinput<165 psec), T setup exceeds the output period. Thus, an appropriate latency must be introduced to achieve proper updating. Thold shows the region to avoid updating of the control signal.

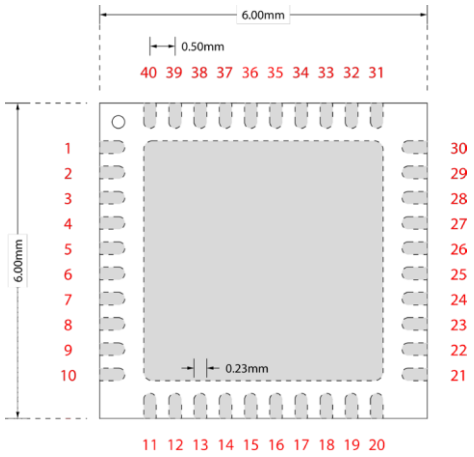
Assuming that the divide controls are updated within one output cycle of the output rising edge, a chart is provided showing the recommended minimum divide ratios plotted against input frequency. This means for a given input frequency, all divide ratios above the minimum recommended divide ratio will achieve smooth divisions, whereas any divide ratio below the minimum may produce momentary errors. These values are a general guideline and may vary depending on the exact situation in which it is used.







UXN14M9P Physical Characteristics



Pkg size:	6.00 x 6.00 mm
Pkg size tolerance:	+/- 0.25 mm
Pkg thickness:	0.9 +/- 0.1 mm
Pad dimensions:	0.23 x 0.4 mm
Center paddle:	4.20 x 4.20 mm
JEDEC designator:	MO-220

Top View

Table 5: UXN14M9P Pin Definition

Pin Number	Function	Notes
1,6,11,17-20,23-29,padddle (Vcc)	RF and DC Ground	0 V
2,3,7-10,12-14,21,22,30,40 (Vee)	Negative Supply Voltage	Nominally -3.3 V
4 (INN)	Divider Input	Negative Terminal of differential input
5 (INP)	Divider Input	Positive Terminal of differential input
15 (OUTP)	Divider Output	Positive Terminal of differential output
16 (OUTN)	Divider Output	Negative Terminal of differential output
31 (P8)	Divide Modulus Control (MSB)	Defaults to logic 0, connect to Vcc-0.8V for logic 1
32 (P7)	Divide Modulus Control	Defaults to logic 0, connect to Vcc-0.8V for logic 1
33 (P6)	Divide Modulus Control	Defaults to logic 0, connect to Vcc-0.8V for logic 1
34 (P5)	Divide Modulus Control	Defaults to logic 0, connect to Vcc-0.8V for logic 1
35 (P4)	Divide Modulus Control	Defaults to logic 0, connect to Vcc-0.8V for logic 1
36 (P3)	Divide Modulus Control	Defaults to logic 0, connect to Vcc-0.8V for logic 1
37 (P2)	Divide Modulus Control	Defaults to logic 0, connect to Vcc-0.8V for logic 1
38 (P1)	Divide Modulus Control	Defaults to logic 0, connect to Vcc-0.8V for logic 1
39 (P0)	Divide Modulus Control (LSB)	Defaults to logic 0, connect to Vcc-0.8V for logic 1
Paddle (Backside of Package)	Vcc, heatsink	Should be tied to Vcc. Paddle is also used for heat dissipation. Need to isolate paddle from ground if using positive supply (i.e., Vcc = +3.3V)

Table 6: Absolute Maximum Ratings

Parameter	Value	Unit
Supply Voltage (Vcc-Vee)	4	V
RF Input Power (INP, INN)	10	dBm
Operating Temperature	-40 to 85	ºC
Storage Temperature	-85 to 125	ºC
Junction Temperature	125	ºC

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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