

# CM-BF537

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## Hardware User Manual

Version 12

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**CM-BF537** – Hardware User Manual

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Warning

Due to technical requirements components may contain dangerous substances.

# 1 Introduction

The Core-Module CM-BF537 is characterized by its field of application, performance and configuration possibility. The module integrates processor, RAM, flash, external peripheral controllers and power supply at a size of 31.5x36.5mm! It is based at the high performance ADSP-BF537 from Analog Devices. The Core-Module is designed for commercial and industrial usage (depending on temperature range). It addresses up to 64MByte SDRAM via its 16bit wide SDRAM bus, has an onboard NOR-flash of 4MByte and offers a CAN interface. In addition, there is an extra Ethernet physical transceiver (10/100Mbit) onboard.

## 1.1 Overview

The current hardware version (see Version Information) of Core Module CM-BF537-C-C-Q25S32F4 (CM-BF537E) consists of the following components. Parts of mounting options of CM-BF537 are listed in addition.

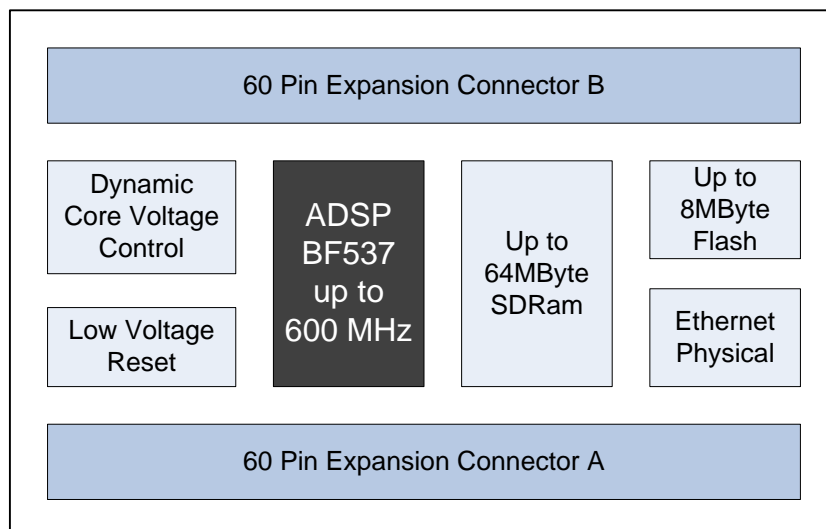


Figure 1-1: Main components of the CM-BF537 Core Module

- **Analog Devices Blackfin Processor BF537**
  - Industrial version (see chapter 8.1)
    - ADSP-BF537SBBCZ-5A (-40° - 85°C)
  - Commercial version (see chapter 8.1)
    - ADSP-BF537SKBCZ-6AV (0° - 70°C)
- **SDRAM**
  - 32MByte SDRAM Version (see chapter 8.1)
    - SDRAM Clock up to 133MHz
    - MT48LC16M16A2BG-7 (16Mx16, 256Mbit at 3.3 V)
  - 64MByte SDRAM Version (see chapter 8.1)

- SDRAM Clock up to 143MHz
- IS42S16320B-7BL (8M x16x4, 512Mbit at 3.3 V)
  
- **4 MByte of Addressable Flash**
  - PF48F2000P0ZBQ0 (4Mx16 32Mbit at 3.3 V; default only 4MByte addressable)
  
  - Additional flash memory can be connected through the expansion board as parallel flash using asynchronous chip select lines or as an SPI flash.
  
- **Ethernet Physical Transceiver**
  - Microchip KSZ8041NLI
  
- **Low Voltage Reset Circuit**
  - Resets module if power supply goes below 2.93 V for at least 140 ms
  
- **Dynamic Core Voltage Control**
  - Core voltage is adjustable by setting software registers on the Blackfin processor
  - Core voltage range: 0.8 – 1.32V
  
- **Expansion Connector A**
  - Data Bus
  - Address Bus
  - Control Signals
  - Power Supply
  - Ethernet Pins
  
- **Expansion Connector B**
  - SPORT0
  - JTAG
  - UART0/UART1
  - CAN
  - TWI (I<sup>2</sup>C compatible)
  - SPI
  - PPI (Parallel Port Interface)
  - GPIO's

## 1.2 Key Features

- The CM-BF537 is very compact and measures only 36.5x31.5mm
- Allows quick prototyping of product that comes very close to the final design
- Reduces development costs, faster time to market
- Very cost effective for small and medium volumes

## 1.3 Applications

- Robotics
- Video security
- Video surveillance
- Industrial distributed control
- Industrial factory automation
- Remote monitoring devices
- Point-of-sale terminals
- VoIP
- Biometrics/security
- Instrumentation
- Medical appliances
- Consumer appliances



## 2 General Description

### 2.1 Functional Description

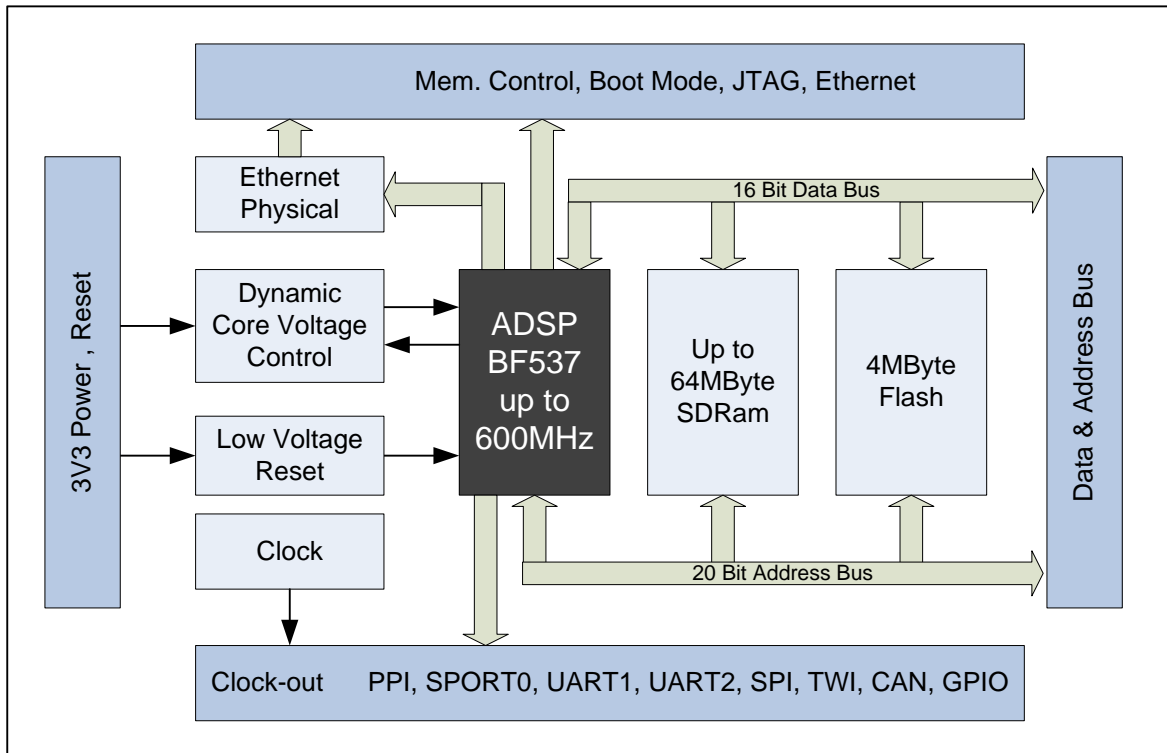


Figure 2-1: Detailed block diagram

Figure 2-1 shows a detailed block diagram of the CM-BF537. Other than the SDRAM control pins the CM-BF537 has all other pins of the Blackfin processor on its two main 60 pin connectors.

A special feature of the Core Module CM-BF537 is the on-board physical Ethernet transceiver from Microchip (KSZ8041NLI).

Dynamic voltage control allows reducing power consumption to a minimum adjusting the core voltage and the clock frequency dynamically in accordance to the required processing power. A low voltage reset circuit guarantees a power on reset and resets the system when the input voltage drops below 2.93V.

### 2.2 Boot Mode

By default, the boot mode = 000 (BMODE2 = low, BMODE1 = low, BMODE0 = low). All BMODE pins have internal pull-down resistors.

Connect BMODE0 to  $V_{CC}$  and leave BMODE1, BMODE2 pins open for boot mode 001 equals to 8- or 16-bit PROM/FLASH boot mode, this is the default boot mode of BLACKSheep® OS. See Blackfin Datasheets or Eval/DevBoard manuals for more details.

## 2.3 Memory Map

### 2.3.1 Core Module Memory

Memory Type	Start Address	End Address	Size	Comment
<b>FLASH Bank0 (PF4 Flag low)</b>	0x20000000	0x201FFFFFF	2MB	1/8 of 16MB NOR Flash, IS29GL256-70DLEB
<b>FLASH Bank1 (PF4 Flag high)</b>	0x20000000	0x201FFFFFF	2MB	1/8 of 16MB NOR Flash, IS29GL256-70DLEB
<b>FLASH Bank2 (PF5 Flag low) <sup>1)</sup></b>	0x20000000	0x201FFFFFF	2MB	1/8 of 16MB NOR Flash, IS29GL256-70DLEB
<b>FLASH Bank3 (PF5 Flag high) <sup>1)</sup></b>	0x20000000	0x201FFFFFF	2MB	1/8 of 16MB NOR Flash, IS29GL256-70DLEB
<b>SD-RAM<sub>32</sub></b>	0x00000000	0x01FFFFFF	32MB	16Bit Bus, Micron IS29GL256-70DLEB
<b>SD-RAM<sub>64</sub></b>	0x00000000	0x1FFFFFFF	64MB	16Bit Bus, ISSI IS42S16320B-7BL

Table 2-1: Memory map

**Note 1)** not usable in default configuration. This PF5 is routed to the connector (see 2.3.2).

The maximum amount of addressable memory by a single asynchronous memory bank is 2MByte. In order to be able to use more than 2MByte on a single bank 2 GPIOs are used to select which 2MB section of flash is active in the memory window of the Blackfin processor. This frees up the remaining banks for the user.

The maximum amount of memory addressable by the processor is 8MByte.

### 2.3.2 Board modifications

By default, PF5 is routed to the connector of the Core Module. Nevertheless, this pin can be used to select bank2/3 of the flash memory. To realize this, the 0 Ω resistor R18 must be removed and soldered to resistor R19 position on the Core Module. In this case PF5 is routed to the flash memory instead to the connector!

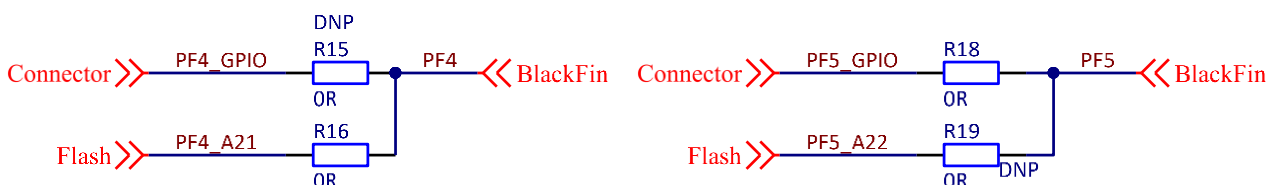


Figure 2-2: PF4 and PF5 routing

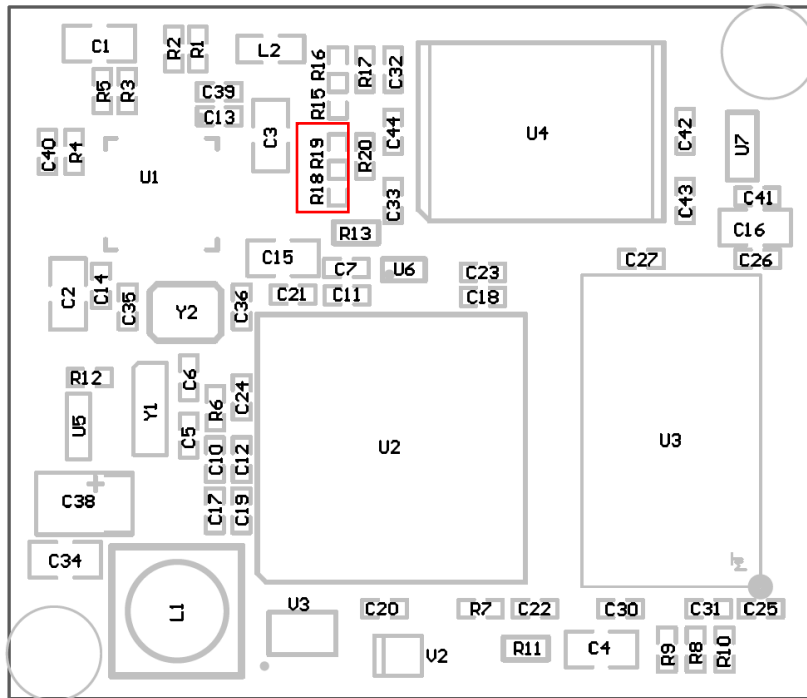


Figure 2-3: Assembly drawing top view



**Warning**

BECOM Systems cannot take responsibility for customer-modified boards. If you need modifications, please request a quote at [office.systems@becom-group.com](mailto:office.systems@becom-group.com).

**2.3.3 Externally Addressable Memory (on connector)**

The Blackfins External Bus Interface (EBI) allows connecting devices via an asynchronous memory interface.

AMS Line	Start Address	End Address	Max. Size
nAMS2	0x20200000	0x202FFFFFFF	1MB
nAMS3	0x20300000	0x203FFFFFFF	1MB

Table 2-2: Externally addressable memory

## 3 Specifications

### 3.1 Electrical Specifications

#### 3.1.1 Maximum Ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only. Operation of the device at these or any other conditions greater than those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
$V_{IO}$	Input or output voltage	-0.5	3.8	V
$V_{IN}$	Input supply voltage	3.0	3.6	V
$I_{OH}/I_{OL}$	Current per pin	0	10	mA
$T_{AMBI}$	Ambient temperature (industrial)	-40	85	°C
$T_{AMBC}$	Ambient temperature (commercial)	0	70	°C
$T_{STO}$	Storage temperature	-55	150	°C
$T_{SLD}$	Solder temperature for 10 seconds		260	°C
$\varphi_{AMB}$	Relative ambient humidity		90	%

Table 3-1: Absolute maximum ratings

#### 3.1.2 Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IN}$	Input supply voltage	3.0	3.3	3.6	V
$I_{3V3}^{3)}$	3.3V current	-	350	-	mA
$V_{OH}$	High level output voltage	2.8	-	-	V
$V_{OL}$	Low level output voltage	-	-	0.5	V
$I_{IH}$	IO input current	-	-	10	μA
$I_{OZ}$	Three state leakage current	-	-	10	μA
$I_{DEEPSLEEP}$	$V_{IN}$ current in deep sleep mode	-	16	-	mA
$I_{SLEEP}$	$V_{IN}$ current in sleep mode	-	19.5	-	mA
$I_{IDLE}$	$V_{IN}$ current in idle mode	-	24	-	mA
$I_{TYP}$	$V_{IN}$ current in with core running at 400 MHz	-	138	-	mA
$I_{HIBERNATE}^{1)}$	$V_{IN}$ current in hibernate state at 400 MHz	-	-	70	mA
$I_{RTC}$	$V_{RTC}$ current	-	20	-	μA
$f_{CCLKC}$	Core clock frequency (commercial grade)	100	-	600	MHz
$f_{CCLKI}$	Core clock frequency (industrial grade)	100	-	500	MHz

Table 3-2: Electrical characteristics

**Note 1)**  $V_{DDINT}=1.10V$  @  $T_J=25^{\circ}C$

**Note 3)** Average load @  $25^{\circ}C$  ambient temperature

### 3.1.3 ESD Sensitivity



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## 4 Connector Description

### 4.1 Connector X1

Pin No.	Signal Name	Type	Function
1	RSCLK0 / TACLK2	I/O	SPORT
2	DR0PRI / TACLK4	I	SPORT
3	TSCLK0 / TACLK1	I/O	SPORT
4	DT0PRI / SSEL2	O	SPORT
5	CLKBUF	O	25MHz buffered clock output
6	SDA	I/O	I <sup>2</sup> C
7	PF4 / TMR5 / SSEL6: MO1 <sup>3)</sup> NC: MO2, MO3 <sup>3)</sup>	I/O	GPIO / Timer / SPI or Not connected
8	PF5 / TMR4 / SSEL5: MO1, MO2 <sup>1) 3)</sup> NC: MO3 <sup>3)</sup>	I/O	GPIO / Timer / SPI or Not connected
9	Vin 3V3	PWR	3V3 +-10% 500mA peak for supply
10	Vin 3V3	PWR	3V3 +-10% 500mA peak for supply
11	PG0 / PPI1D0	I/O	GPIO / PPI data
12	PG2 / PPI1D2	I/O	GPIO / PPI data
13	PG4 / PPI1D4	I/O	GPIO / PPI data
14	PG6 / PPI1D6	I/O	GPIO / PPI data
15	PG8 / PPI1D8 / DR1SEC	I/O	GPIO / PPI data / SPORT
16	PG10 / PPI1D10 / RSCLK1	I/O	GPIO / PPI data / SPORT
17	PG12 / PPI1D12 / DR1PRI	I/O	GPIO / PPI data / SPORT
18	PG14 / PPI1D14 / TFS1	I/O	GPIO / PPI data / SPORT
19	PPI1SY3 / PF7 / TMR2	I/O	GPIO / PPI sync / Timer
20	PPI1SY1 / PF9 / TMR0 <sup>1)</sup>	I/O	GPIO / PPI sync / Timer
21	PPI1SY1 / PF9 / TMR0 <sup>1)</sup>	I/O	GPIO / PPI sync / Timer
22	PF3 / Rx1 / TMR6 / TACI6	I/O	GPIO / Timer
23	PF1 / DMAR1 / TACI1 / Rx0	I/O	GPIO / UART
24	PF11 / MOSI	I/O	GPIO / SPI
25	PF13 / SCK	I/O	GPIO / SPI
26	BMODE0 <sup>2)</sup>	I - 10k pull down	Boot mode
27	GND	PWR	Power
28	TCK <sup>2)</sup>	I - 10k pull up	JTAG
29	TDI <sup>2)</sup>	I - 10k pull up	JTAG
30	TRST <sup>2)</sup>	I - 4k7 pull down	JTAG
31	EMU	O	JTAG
32	TMS <sup>2)</sup>	I - 10k pull up	JTAG
33	TDO	O	JTAG
34	BMODE2 <sup>2)</sup>	I - 10k pull down	Boot mode

35	N.C.	-	NC
36	BMODE1 <sup>2)</sup>	I - 10k pull down	Boot mode
37	PF12 / MISO	I/O	GPIO / SPI
38	PF0 / DMAR0 / Tx0	I/O	GPIO / UART
39	PF14 / SPI_SS	I/O	GPIO / SPI
40	PF2 / Tx1 / TMR7	I/O	GPIO /UART / Timer
41	PPI1Clk / PF15 / TMRCLK	I/O	GPIO / PPI clock
42	PPI1Sy2 / PF8 / TMR1	I/O	GPIO / PPI sync / Timer
43	PG15 / PPI1D15 / DT1PRI	I/O	GPIO / PPI data / SPORT
44	PG13 / PPI1D13 / TSCLK1	I/O	GPIO / PPI data / SPORT
45	PG11 / PPI1D11 / RFS1	I/O	GPIO / PPI data / SPORT
46	PG9 / PPI1D9 / DT1SEC	I/O	GPIO / PPI data / SPORT
47	PG7 / PPI1D7	I/O	GPIO / PPI data
48	PG5 / PPI1D5	I/O	GPIO / PPI data
49	PG3 / PPI1D3	I/O	GPIO / PPI data
50	PG1 / PPI1D1	I/O	GPIO / PPI data
51	GND	PWR	Power
52	GND	PWR	Power
53	PF5 / TMR4 / SSEL5: MO1, MO2 <sup>1) 3)</sup> NC: MO3 <sup>3)</sup>	I/O	GPIO / Timer / SPI or Not connected
54	PF6 / TMR3 / SSEL4	I/O	GPIO / Timer / SPI
55	PF10 / SSEL1	I/O	GPIO / SPI
56	SCL	I/O	I <sup>2</sup> C
57	DT0SEC / SSEL7 / CANTx	O	SPORT / SPI / CAN
58	TFS0 / SSEL3	I/O	SPORT / SPI
59	DR0SEC / TACIO / CANRx	I	SPORT / CAN
60	RFS0 / TACLK3	I/O	SPORT

Table 4-1: Connector description X1

**Note 1)** Pin 8 and 53 as well as pin 20 and 21 are identical.

**Note 2)** Please mind the mounted pull-up and pull-down resistors on the Core Module.

**Note 3)** For mount option details see chapter 8.1.

## 4.2 Connector X2

Pin No.	Signal Name	Type	Function
61	A1	O	Address Bus
62	A3	O	Address Bus
63	A5	O	Address Bus
64	A7	O	Address Bus
65	A9	O	Address Bus
66	A11	O	Address Bus
67	A13	O	Address Bus
68	A15	O	Address Bus
69	A17	O	Address Bus
70	A19	O	Address Bus
71	ABE1/SDQM1	O	Memory Control Bus
72	LED_ACT	O	Indicates Ethernet activity
73	GND	-	AGND use as GND for Ethernet
74	RX+	I - 47R pull up to 3V3	Ethernet receive +
75	RX-	I - 47R pull up to 3V3	Ethernet receive -
76	ADRY	I - 10k pull up	Memory Control Bus
77	BG	O	Memory Control Bus
78	CLK_OUT	O	CLKOUT Pin of Blackfin
79	GND	PWR	
80	AMS3	O	Memory Control Bus
81	AWE	O	Memory Control Bus
82	NMI	I - 10k pull up	Non-Maskable Interrupt
83	D0	I/O	Data Bus
84	D2	I/O	Data Bus
85	D4	I/O	Data Bus
86	D6	I/O	Data Bus
87	D8	I/O	Data Bus
88	D10	I/O	Data Bus
89	D12	I/O	Data Bus
90	D14	I/O	Data Bus
91	D15	I/O	Data Bus
92	D13	I/O	Data Bus
93	D11	I/O	Data Bus
94	D9	I/O	Data Bus
95	D7	I/O	Data Bus
96	D5	I/O	Data Bus
97	D3	I/O	Data Bus
98	D1	I/O	Data Bus



Pin No.	Signal Name	Type	Function
99	RESET	I – see chapter 5.2	Reset
100	AOE	O	Memory Control Bus
101	ARE	O	Memory Control Bus
102	AMS2	O	Memory Control Bus
103	VDD-RTC	PWR	Backup battery supply
104	BGH	O	Memory Control Bus
105	BR	I - 10k pull up	Memory Control Bus
106	VA33	PWR	Ethernet transformer voltage reference
107	TX-	O - 47R pull up to 3V3	Ethernet transmit -
108	TX+	O - 47R pull up to 3V3	Ethernet transmit +
109	NC		
110	LED_SPEED	O	Full duplex LED, High = Full duplex active, Low = inactive
111	ABE0/SDQM0	O	Memory Control Bus
112	A18	O	Address Bus
113	A16	O	Address Bus
114	A14	O	Address Bus
115	A12	O	Address Bus
116	A10	O	Address Bus
117	A8	O	Address Bus
118	A6	O	Address Bus
119	A4	O	Address Bus
120	A2	O	Address Bus

Table 4-2: Connector description X2

**Note:** Please mind the mounted pull-up and pull-down resistors on the Core Module.

## 5 Application Information

### 5.1 Supply Voltage Decoupling

For a better stability we recommend to add a 100nF capacitor for each power supply pin and a 47uF tantalum capacitor to the  $V_{IN}$  voltage rail next to the module.

### 5.2 Reset circuit

The reset of the flash and the processor are connected to a power monitoring IC. The output can be used as power on reset for external devices, see Figure 5-1.

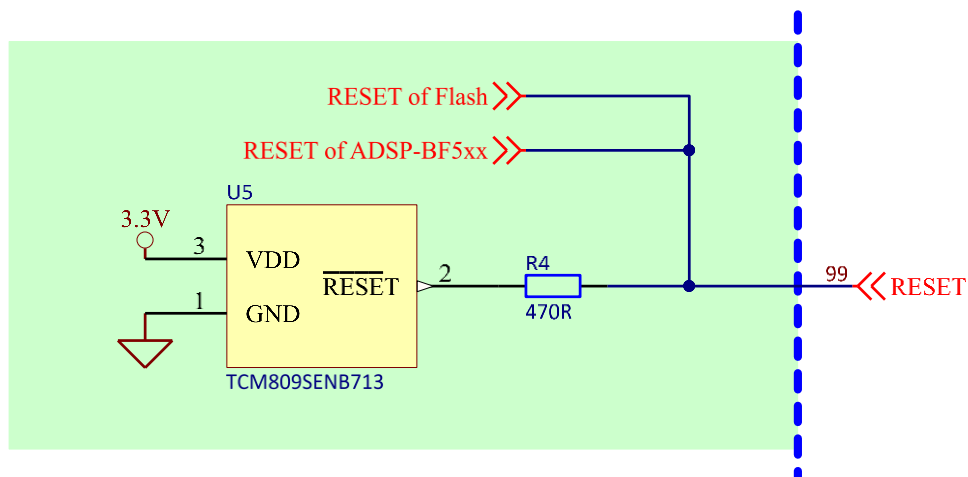


Figure 5-1: Schematic of reset circuit on the Core Module

## 5.3 Application Example Schematics

### 5.3.1 RJ45 schematic

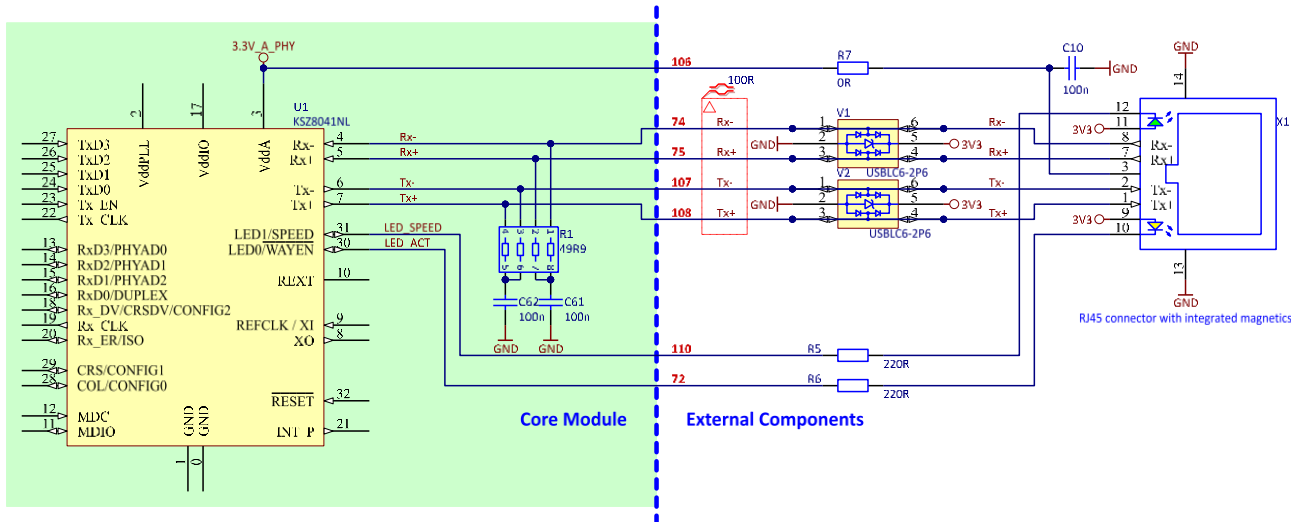


Figure 5-2: Schematic for RJ45 Connection

Designator	Value	Type	Description	Quantity
X1		RJLBC-060TC1	RJ45 with magnetics	1
R5, R6	220 Ω	Resistor	Resistor	2
R7	0 Ω	Resistor	Resistor	1
C1	10 uF	Capacitor	Capacitor	1
V1, V2		USBLC6-2P6	TSV-Diode	2

Table 5-1: Parts List RJ45

## 5.4 Sample Schematic

In this minimum configuration the CM-BF537 is used as a high-performance network connected processor module.

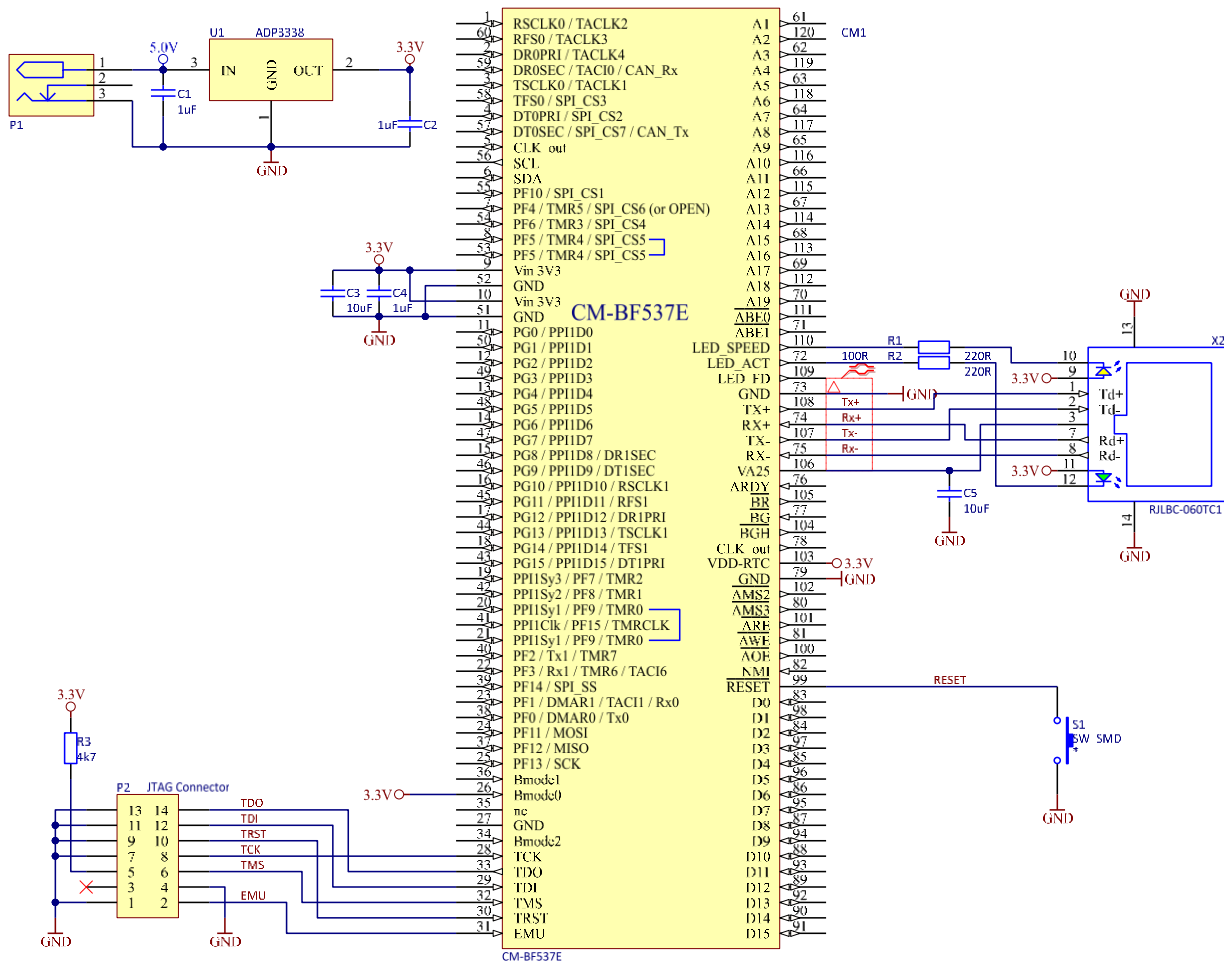


Figure 5-3: Configuration with Ethernet and JTAG Connector

Designator	Value	Type	Description	Quantity
<b>C1, C2, C4</b>	1uF		Capacitor	3
<b>C3, C5</b>	10uF		Capacitor	1
<b>CM1</b>			CM-BF537	1
<b>X1</b>		DC-8	Power connector DC-8	1
<b>X2</b>		RJLBC-060TC1	RJ45 with transformer	1
<b>X3</b>			Header, 7-Pin, dual row	1
<b>R3</b>	4k7		Resistor	1
<b>R8, R9</b>	220R		Resistor	2
<b>S1</b>			Push Button	1
<b>U1</b>		ADP3338	Low dropout regulator	1

Table 5-2: Bill of Material of sample circuit

## 5.5 Stand-alone Ethernet based MPEG webcam

The CM-BF537 module can be used as a stand-alone module for a camera system requiring only power supply and the direct attachment of a compatible video camera. An extender board including a camera is available at BECOM Systems ([EXT-BF5xx-CAM](#)).

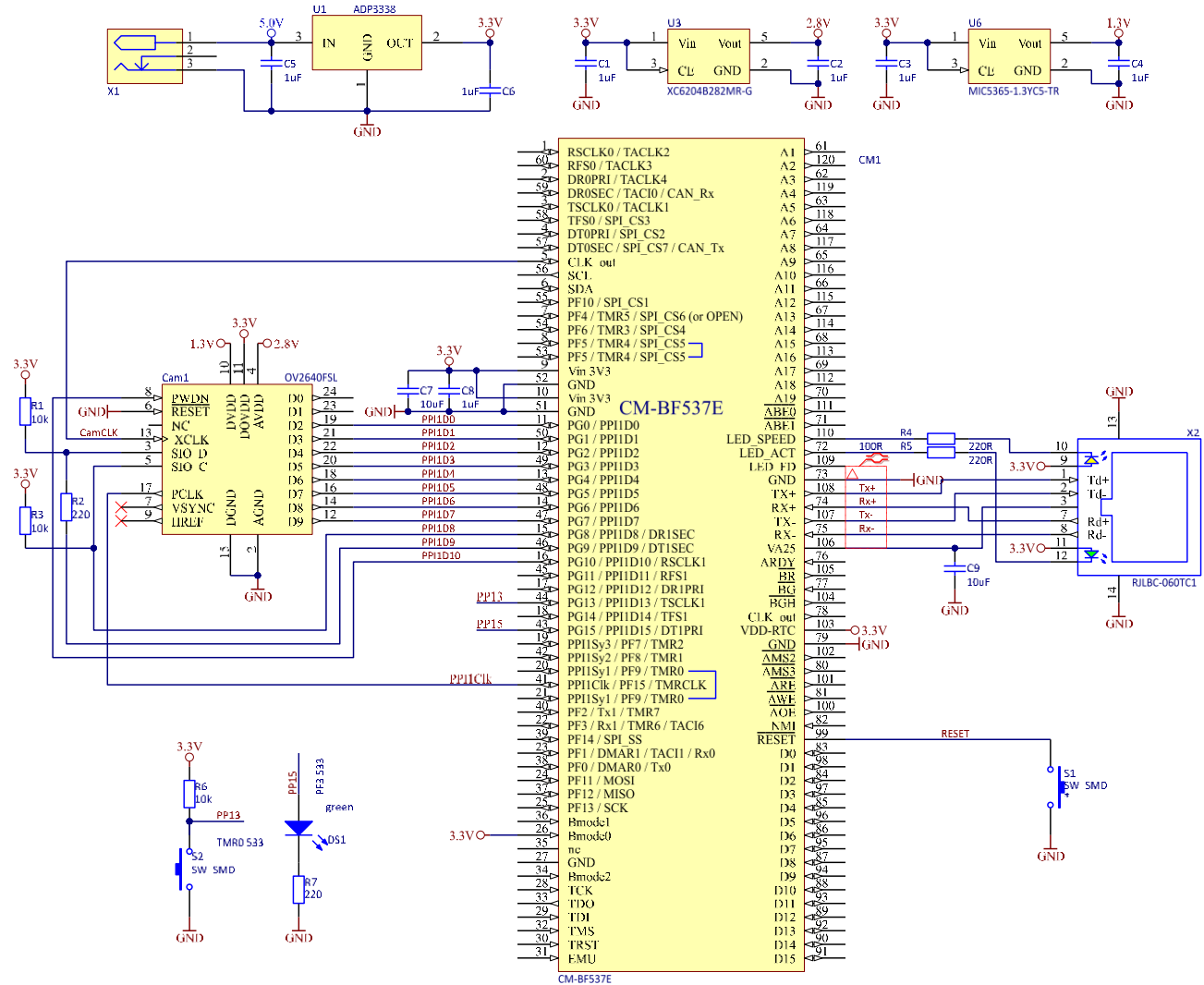


Figure 5-4: Stand-alone Ethernet based MPEG webcam

Designator	Value	Type	Description	Quantity
<b>C1, C2, C3, C4, C5, C6, C8</b>	1uF	X7R	Capacitor	7
<b>C7, C9</b>	10uF	X7R	Capacitor	2
<b>Cam1</b>		OV7660FSx	Camera module	1
<b>CM1</b>		CM-BF537	CM-BF537	1
<b>DS1</b>	green		SMD LED	1
<b>X1</b>		DC-8	Power connector DC-8	1
<b>X2</b>		RJLBC-060TC1	RJ45 with transformer	1

<b>R1, R3, R6</b>	10k	Resistor	3
<b>R2, R4, R5</b>	220R	Resistor	3
<b>S1, S2</b>		Push button	1
<b>U1</b>	ADP3338	Low dropout regulator	1
<b>U2</b>	XC6204B282MR-G	XC6204 high speed LDO	1
<b>U3</b>	MIC5365-1.3YC5-TR	MIC5365 LDO	1

Table 5-3: Bill of Materials of a Stand-alone Ethernet based MPEG Webcam

Have a look at our DEV-BF5xxDA-lite schematics, which can be found at [support.systems.becom-group.com/wiki/CM-BF537](http://support.systems.becom-group.com/wiki/CM-BF537) to get application examples.

## 6 Mechanical Outline

### 6.1 Top View

Figure 6-1 shows the bottom view of the CM-BF537. All dimensions are given in millimeters. Take 0.5 mm as a tolerance for the boarder of the board since it is broken out from a multi-board panel and some additional boarder may remain.

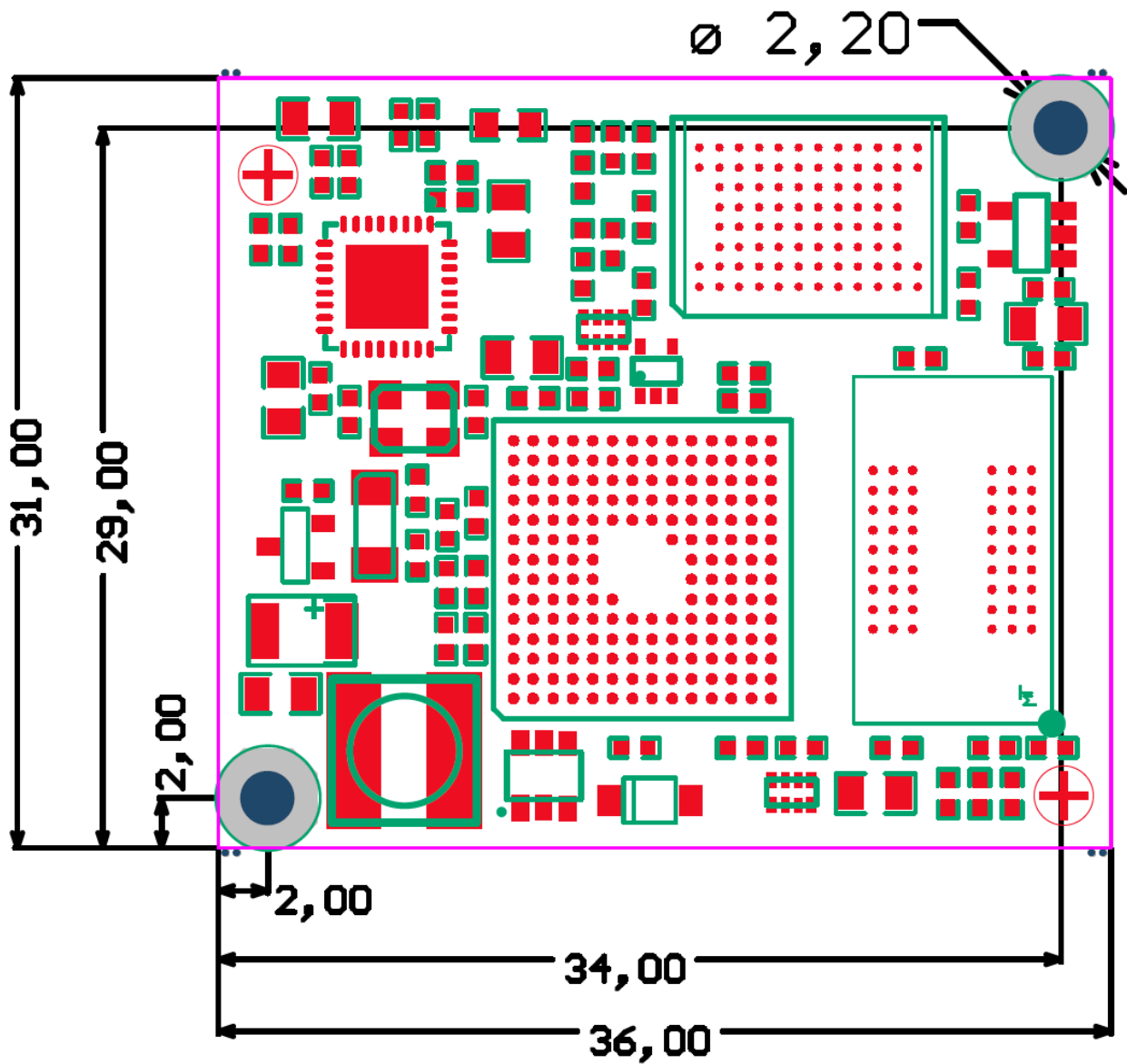


Figure 6-1: Mechanical outline (top view)

## 6.2 Bottom View

Figure 6-2 shows the TOP VIEW of the bottom side components (through the Board View) of the CM-BF537 Core Module. All dimensions are given in millimeters.

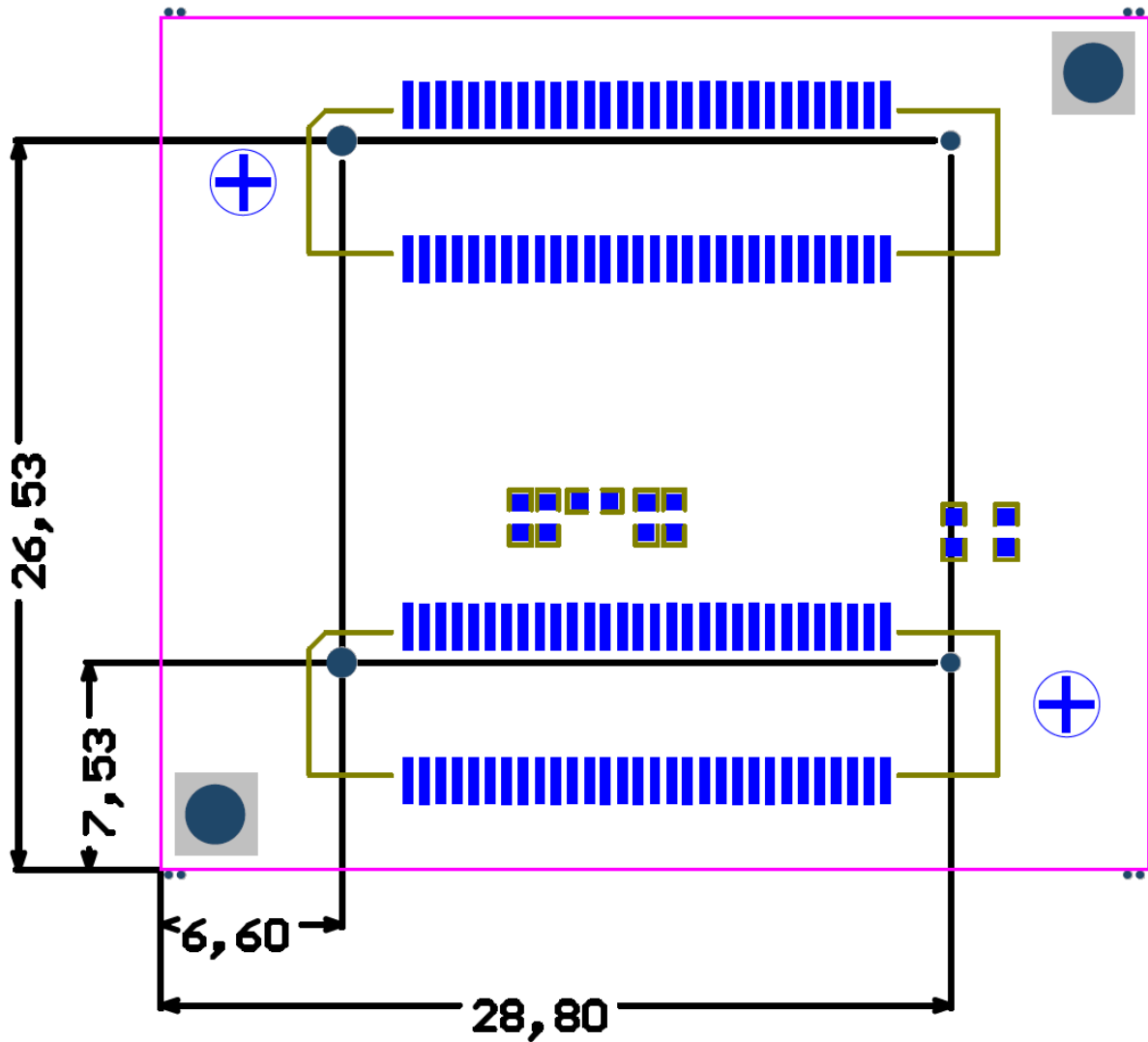


Figure 6-2: Mechanical outline and Bottom Connectors (Top View)

## 6.3 Side View

Figure 6-3 shows the side view of the CM-BF537. All dimensions are given in millimeters.

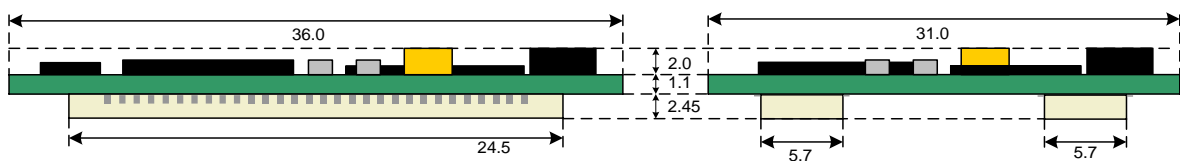


Figure 6-3: Side view with mounted connectors



The total minimum mounting height including receptacle at the motherboard is 6.1mm.

## 6.4 Footprint

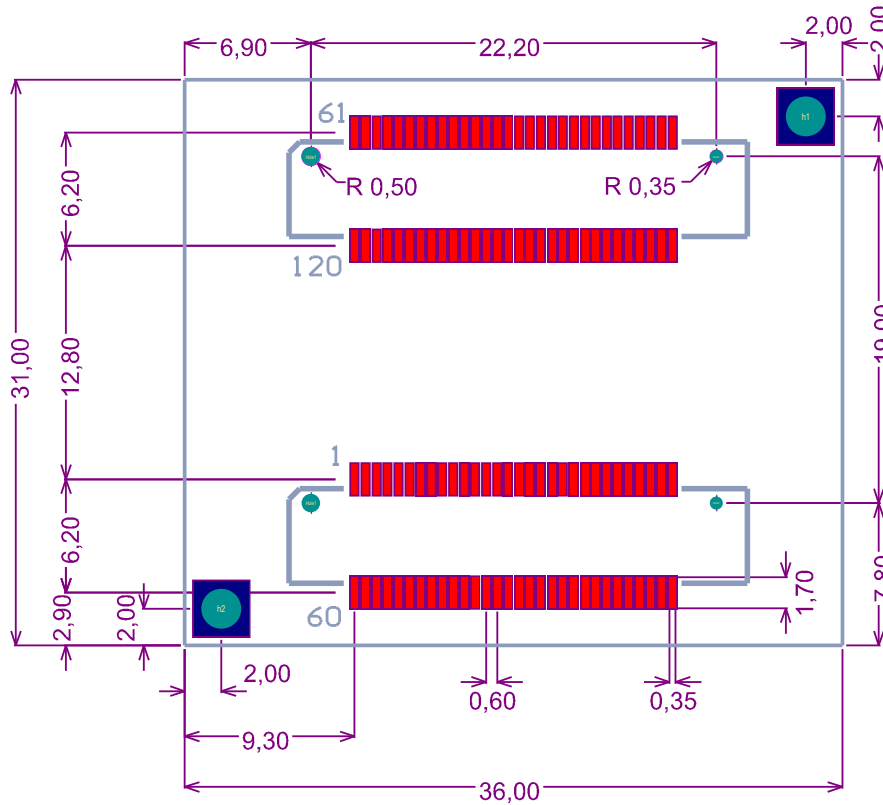


Figure 6-4: Recommended footprint for the Core Module (top view)

The footprint of the CM-BF537 for Altium Designer is available on request. The used connectors can be found in Table 6-1. For detailed dimensions of the connectors please see the datasheet from the manufacturer's website.

## 6.5 Connectors

The Core Module features a Hirose 0.6mm pitch connectors. The base board has to use the complementary connector.

Board	Designator	Manufacturer	Manufacturer Part No.
Core Module	X1, X2	Hirose	FX8-60P-SV
Base board	X1, X2	Hirose	FX8-60S-SV

Table 6-1: Core Module connector types

## 7 Support

### 7.1 General Support

General support for products can be found at BECOM Systems support site [support.systems.becom-group.com](http://support.systems.becom-group.com)

### 7.2 Board Support Packages

Board support packages and software downloads are for registered customers only [support.systems.becom-group.com](http://support.systems.becom-group.com)

### 7.3 Blackfin® Software Support

#### 7.3.1 [BLACKSheep® OS](#)

BLACKSheep® OS stands for a powerfully and multithreaded real-time operating system (RTOS) originally designed for digital signal processing application development on Analog Devices Blackfin® embedded processors. This high-performance OS is based on the reliable and stable real-time VDK kernel from Analog Devices that comes with VDSP++ IDE. Of course, BLACKSheep® OS is fully supported by all BECOM Systems Core-Modules and development hardware.

#### 7.3.2 LabVIEW

You can get LabVIEW embedded support for BECOM Systems Core Modules by Schmid-Engineering AG <http://www.schmid-engineering.ch>.

#### 7.3.3 uClinux

You can get uClinux support (boot loader and uClinux) for BECOM Systems Core Modules at <http://blackfin.uClinux.org>.

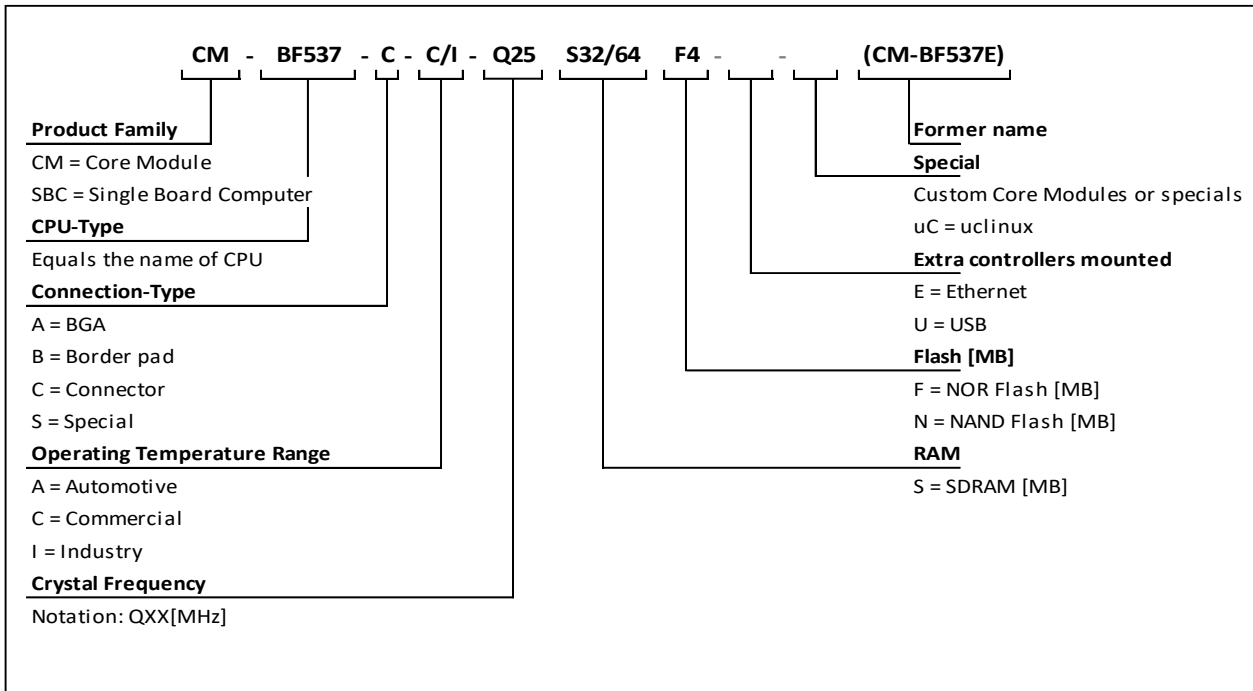
### 7.4 Blackfin® Design Services

Based on more than seven years of experience with Blackfin, BECOM Systems offers development assistance as well as custom design services and software development.

#### 7.4.1 Upcoming Products and Software Releases

Keep up to date with all product changes, releases and software updates of BECOM Systems at [systems.becom-group.com](http://systems.becom-group.com)

## 8 Ordering Information



Article Number	Name	Temperature Range	Max Coreclk Freq. [MHz]	Preflashed Firmware
100-1221-3	CM-BF537-C-C-Q25S32F4 (CM-BF537E)	0°C to 70°C	600	bsboot
100-1229-3	CM-BF537-C-I-Q25S32F4 (CM-BF537E-I)	-40°C to 85°C	500	bsboot
100-1273-3	CM-BF537-C-C-Q25S64F4 (CM-BF537E-64SD)	0°C to 70°C	600	bsboot
100-1274-3	CM-BF537-C-I-Q25S64F8	-40°C to 85°C	500	custom
100-1275-3	CM-BF537-C-I-Q25S64F8	-40°C to 85°C	500	bsboot

Table 8-1: Ordering information



**Note**

Custom Core Modules are available on request! Please contact BECOM Systems ([office.systems@becom-group.com](mailto:office.systems@becom-group.com)) if you are interested in custom Core Modules.

The mount options of the Core Module CM-BF537 are shown in Table 8-2.

Mount Option	Flash	Comment
MO1	2MB	PF4 available on pin 7 on connector X1
MO2	4MB	default
MO3	8MB	PF5 not available on connector X1

Table 8-2: Mount options

## 9 Dependability

### 9.1 MTBF

Please keep in mind that a part stress analysis would be the only way to obtain significant failure rate results, because MTBF numbers just represent a statistical approximation of how long a set of devices should last before failure. Nevertheless, we can calculate an MTBF of the Core Module using the bill of material. We take all the components into account. The PCB and solder connections are excluded from this estimation. For test conditions we assume an ambient temperature of 30°C of all Core Module components except the Blackfin® processor (80°C) and the memories (70°C). We use the MTBF Calculator from ALD (<http://www.aldservice.com/>) and use the reliability prediction MIL-217F2 Part Stress standard.

This method resulted in a MTBF of 439232 hours for the CM-BF537E.

## 10 Product History

### 10.1 Version Information

For information about changes and updates please refer to our revision report at [https://support.bluetechnix.at/wiki/Revision\\_Report\\_CM-BF537E](https://support.bluetechnix.at/wiki/Revision_Report_CM-BF537E)

### 10.2 Anomalies

Version	Date	Description
3.2	2011 04 27	No anomalies reported.
3.0	2010 10 12	No anomalies reported.

Table 10-1: Overview product anomalies

## 11 Document Revision History

Version	Date	Document Revision
12	2020 10 19	Updated ordering information Updated revision report link
11	2019 11 28	Update Links
10	2019 03 26	Update for hardware revision V3.5.0 (new flash, different ethernet termination)
9	2012 05 24	Description of Pin 78 and Pin 5 of Core Module corrected
8	2012 02 07	Dependability added Memory table update, description for PF5 added
7	2011 11 14	Pin out and connector description corrected
6	2011 10 18	Table 3-2: Electrical characteristics update
5	2011 09 06	Pin out and connector description corrected
4	2011 04 27	Updated HUM to current design. Added industrial version and 64MByte version to this HUM.
3	2010-02-02	Redesign of Manual
2	2009-11-05	Picture 3-7, 6-1, 6-2, Table 6-1, 6-2 updated
1	2009-08-31	First release V1.0 of the document copied from CM-BF537 V1.2 and updated to Revision 3.0

Table 11-1: Revision history

## 12 List of Abbreviations

Abbreviation	Description
<b>ADI</b>	Analog Devices Inc.
<b>AI</b>	Analog Input
<b>AMS</b>	Asynchronous Memory Select
<b>AO</b>	Analog Output
<b>CM</b>	Core Module
<b>DC</b>	Direct Current
<b>DSP</b>	Digital Signal Processor
<b>eCM</b>	Enhanced Core Module
<b>EBI</b>	External Bus Interface
<b>ESD</b>	Electrostatic Discharge
<b>GPIO</b>	General Purpose Input Output
<b>I</b>	Input
<b>I<sup>2</sup>C</b>	Inter-Integrated Circuit
<b>I/O</b>	Input/Output
<b>ISM</b>	Image Sensor Module
<b>LDO</b>	Low Drop-Out regulator
<b>MTBF</b>	Mean Time Between Failure
<b>NC</b>	Not Connected
<b>NFC</b>	NAND Flash Controller
<b>O</b>	Output
<b>OS</b>	Operating System
<b>PPI</b>	Parallel Peripheral Interface
<b>PWR</b>	Power
<b>RTOS</b>	Real-Time Operating System
<b>SADA</b>	Stand Alone Debug Agent
<b>SD</b>	Secure Digital
<b>SoC</b>	System on Chip
<b>SPI</b>	Serial Peripheral Interface
<b>SPM</b>	Speech Processing Module
<b>SPORT</b>	Serial Port
<b>TFT</b>	Thin-Film Transistor
<b>TISM</b>	Tiny Image Sensor Module
<b>TSC</b>	Touch Screen Controller
<b>UART</b>	Universal Asynchronous Receiver Transmitter
<b>USB</b>	Universal Serial Bus
<b>USBOTG</b>	USB On The Go
<b>ZIF</b>	Zero Insertion Force

Table 12-1: List of abbreviations

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