TUSB4041PAP Evaluation Module

This user's guide describes the characteristics, hardware overview and set up, installation, and use of the TUSB4041PAP Evaluation Module (EVM). A complete schematic diagram and bill of materials (BOM) are included in this document.

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1 Introduction

The Texas Instruments TUSB4041PAP evaluation module is a functional board design of a single device that implements a USB 2.0 hub. The EVM can support USB 2.0 (HS, FS, and LS) operation on its USB ports. This EVM is intended for use in evaluating system compatibility, developing optional EEPROM firmware, and validating interoperability. This EVM also acts as a hardware reference design for any implementation of the TUSB4041.

Upon request, layout files for the EVM can be provided to illustrate techniques used to route the differential pairs, use of split power planes, placement of filters and other critical components, and methods used to achieve length-matching of critical signals.

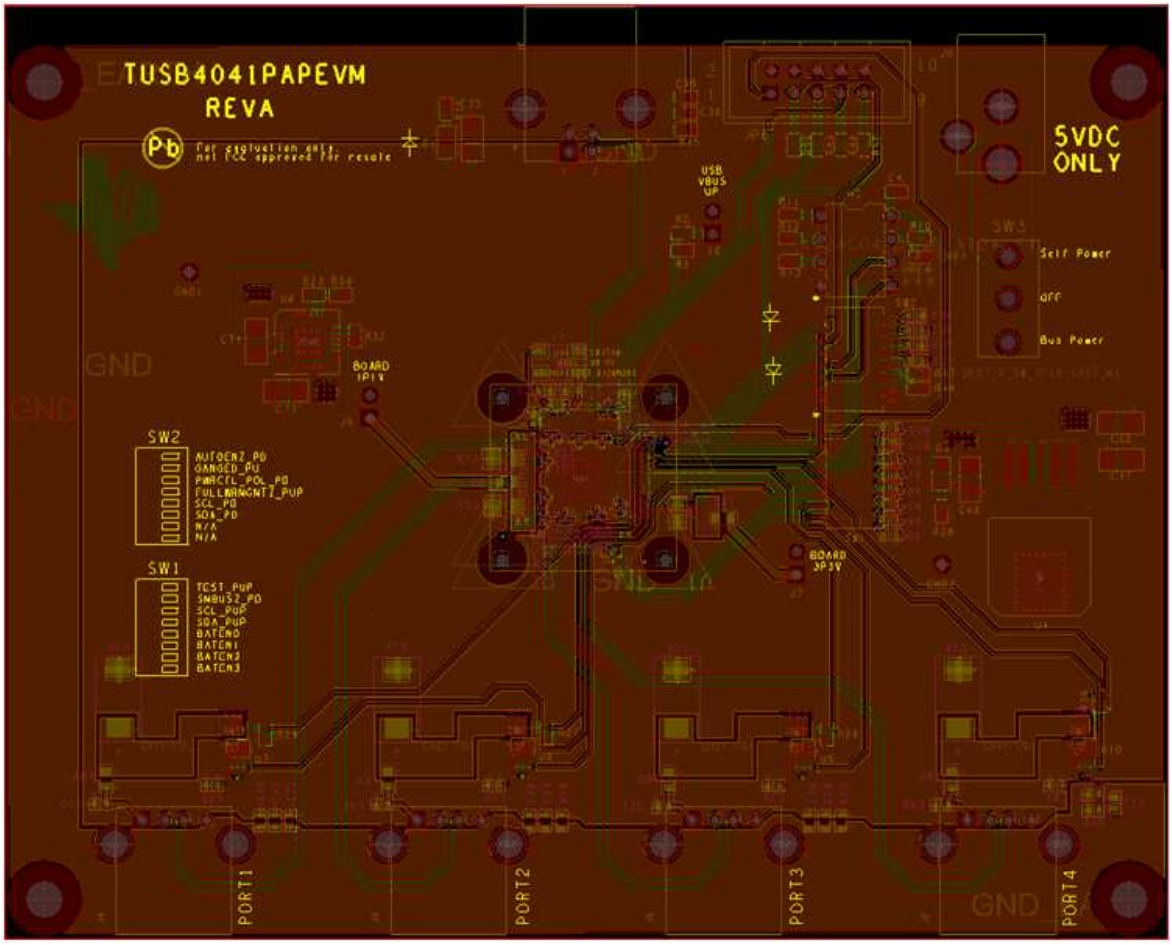

Figure 1. TUSB4041PAPEVM Top Layer Layout

2 Hardware Overview

The TUSB4041PAPEVM board hardware can be divided into six functional areas:

2.1 TUSB4041PAP

The TUSB4041PAPEVM (U2 on the schematic) operates as a functional interconnect between an upstream connection to a USB host or hub and up to two directly-connected downstream devices or hubs. More devices and hubs can be supported if arranged in tiers. The TUSB4041 is capable of supporting operation at High-Speed (HS), Full Speed (FS), or Low Speed (LS). In general, the speed of the upstream connection of the TUSB4041PAPEVM limits the downstream connections to that speed (HS and FS) or lower.

The TUSB4041 requires a 24-MHz low-ESR crystal, Y1 with a 1-MΩ feedback resistor. The crystal should be fundamental mode with a load capacitance of 12 pF – 24 pF and a frequency stability rating of ±100 PPM or better. To ensure a proper startup oscillation condition, a maximum crystal equivalent series resistance (ESR) of 50 Ω is recommended.

The TUSB4041 can also use an oscillator or other clock source. When using an external clock source such as an oscillator, the reference clock should have ±100 PPM (or better) frequency stability and have less than 50-ps absolute peak-to-peak jitter (or less) than 25-ps peak-to-peak jitter after applying the USB 3.0 jitter transfer function.

2.2 USB Port Connectors

The TUSB4041PAPEVM is equipped with five standard USB2.0 port connectors. One of these five connectors, J1, is a Type-B connector designed to interface with an upstream USB host or hub. The remaining connectors, J2, J3, J4, and J5 are Type-A connectors for connection to downstream devices or hubs. Standard size connectors were used on the EVM design but USB micro connectors can be used, if desired.

The USB ports can be attached via a standard USB cable to any USB 2.0 host, hub, or device. The TUSB4041 will automatically connect to any upstream USB 2.0 host or hub at HS.

2.2.1 USB Port Connector - Power

VBUS is received from the upstream host or hub on J1. The TUSB4041 can be configured as a self-powered or bus-power hub, just setting SW3 in the required option.

When the EVM is set for self-power there is not any significant current draw by the EVM from VBUS. The TUSB4041 does monitor the VBUS input after filtering through a resistor divider network of a 90.9-kΩ, 1% resistor, R2, and a 10-kΩ, 1% resistor, R3. VBUS cannot be directly connected to the TUSB4041 device. A bulk capacitor of at least 1 μF is required on the upstream port VBUS input to comply with the USB specification. The TUSB4041PAPEVM uses a 10-μF capacitor, C35.

VBUS, sourced by the 5-V wall power input, J6, is provided to the downstream port connectors. The USB 2.0 specification limits the current consumption of a USB 2.0 device to 500 mA at 5 V. The current-limiting parameter of the TPS2001C device, U7, is configured to 2.2 A to avoid any spurious overcurrent events due to bus-powered HDD spin-up power fluctuations or unnecessary limiting during USB charging. A production implementation could place stricter limits on this power consumption. An overcurrent event on any of the downstream port connectors will be reported to the TUSB4041 via the OVERCURxZ inputs.

2.2.2 USB Port Connector – Noise Filtering

Each downstream VBUS output has a 150-μF bulk capacitor (C70, C71, C76, C79) as recommended by the TPS2001C data manual (SLVSAU6) to prevent in-rush current events on the downstream devices. In addition, there are ferrite beads and small capacitors on the VBUS lines to reduce noise and address ESD/EMI concerns.

The TUSB4041PAPEVM also implements optional isolation using two small noise-filtering capacitors and a 1-MΩ resistor between the earth ground of each connector and the digital ground of the EVM, this is not a requirement but should be used if ground isolation is desired.

2.3 Optional Serial EEPROM

Each TUSB4041PAPEVM is equipped with an onboard EEPROM/socket placeholder, U2. A small I^2C EEPROM can be installed to set the configuration registers as defined in the TUSB4041 data manual (SLLSEK3A). In its default setting, the EVM does not have an EEPROM installed and instead uses the configuration inputs to determine any optional settings of the TUSB4041.

The EEPROM interface defaults to programmable (not write-protected) so that any installed EEPROM's contents may be modified to test various settings. If an EEPROM data change is required, the values may be changed using the register access methods outlined in the TUSB4041 data sheet. In addition, a Microsoft® Windows® based EEPROM utility is available upon request.

2.4 Power

The TUSB4041PAPEVM operates from the power provided by a 5-V wall power adapter, J6, or bus power supplied by a USB host. It is recommended to use a wall power adapter that is capable of sourcing 4 A to 5 A because the hub must be able to source significant power on its downstream ports (500 mA per port).

The TUSB4041PAPEVM uses a single-channel LDO voltage regulator to drop 5 V to 3.3 V. The TPS7A4533, U4, is a 1.5-A output linear regulator (SLVS720). The 1.1-V core voltage required by the TUSB4041 is sourced by the 3.3-V rail to reduce unnecessary heat dissipation. The TPS74801, U6, is a 1.5-A output single-channel LDO linear regulator (SBVS074). Both regulators require few external passive components and are appropriately rated for heat dissipation.

2.5 Hub Configuration

The TUSB4041PAPEVM can be configured by setting several inputs to the TUSB4041 that are sampled at power-on reset or using an optional serial EEPROM or SMBUS host. A production implementation without EEPROM or SMBUS could either rely on the default internal pullup or pulldown resistor for each configuration input or over-ride it with an external pullup or pulldown resistor. The settings can be modified using SW1 and SW2 on the EVM. Descriptions of the possible configuration changes are included in Section 3.1.

2.6 Optional Circuitry

The following list provides the optional circuitry available on the TUSB4041PAPEVM:

- D4 – Indicates BOARD_3P3V is active
- The switch (SW1, SW2) and headers (J8, JP6) provided on the TUSB4041PAPEVM are intended for lab evaluation only and are not required for production designs.

3 Hardware Set Up

3.1 Configuration Switch

The TI TUSB4041PAPEVM has a set of switches to facilitate configuration changes. Changing these switch settings without a complete understanding of the result is not recommended. Configuration inputs are only read by the TUSB4041 during power on reset, changing the switch settings while the EVM is powered on will have no effect. Please refer to the EVM schematics for additional information (included in the appendix).

The switch definitions are as follows, with the standard setting in parenthesis:

SW1_1 (off): TEST_TRSTZ. This pin is reserved for factory test.

SW1_2 (off): SMBUSz Switch. The TUSB4041 has an internal pullup on this terminal, so I^2C interface mode is enabled by default. If the switch is set to the ON position, the terminal is pulled low and SMBUS mode is enabled.

SW1_3 (off): SCL_SMBCLK Switch. The TUSB4041 has an internal pulldown on this terminal, so the serial EEPROM/SMBUS interface is disabled. If the switch is set to the ON position, a pullup resistor is connected to the serial clock terminal to indicate that an I^2C EEPROM may be attached (along with a pullup resistor on SDA).

SW1_4 (off): SDA_SMBDAT Switch. The TUSB4041 has an internal pulldown on this terminal, so the serial EEPROM/SMBUS interface is disabled. If the switch is set to the ON position, a pullup resistor is connected to the serial clock terminal to indicate that an I^2C EEPROM may be attached (along with a pullup resistor on SCL).

SW1_5 (off): PWRCTL1_BATEN1 Switch. The TUSB4041 has an internal pulldown on this terminal, so USB Battery Charging mode on Port 1 is disabled by default. If the switch is set to the ON position, the terminal is pulled high and battery charging is enabled on downstream Port 1.

SW1_6(off): PWRCTL2_BATEN2 Switch. The TUSB4041 has an internal pulldown on this terminal, so USB Battery Charging mode on Port 2 is disabled by default. If the switch is set to the ON position, the terminal is pulled high and battery charging is enabled on downstream Port 2.

SW1_7 (off): PWRCTL1_BATEN1 Switch. The TUSB4041 has an internal pulldown on this terminal, so USB Battery Charging mode on Port 3 is disabled by default. If the switch is set to the ON position, the terminal is pulled high and battery charging is enabled on downstream Port 3.

SW1_8(off): PWRCTL2_BATEN2 Switch. The TUSB4041 has an internal pulldown on this terminal, so USB Battery Charging mode on Port 4 is disabled by default. If the switch is set to the ON position, the terminal is pulled high and battery charging is enabled on downstream Port 4.

SW2_1 (on): AUTOENZ Switch. Automatic charge mode enable/HS suspend status The value of the pin is sampled at the deassertion of reset to determine if automatic mode is enabled as follows:

0 = Automatic mode is enabled on ports that are enabled for battery charging when the hub is unconnected. Note that CDP is not supported on Port 1 when operating in automatic mode.

1 = Automatic mode is disabled.
This value is also used to set the autoEnz bit in the Battery Charging Support Register. After reset, this signal indicates the high-speed USB suspend status of the upstream port if enabled through the Additional Feature Configuration Register. When enabled, a value of 1 indicates the connection is suspended.

SW2_2 (on): GANGED_HS_UP Switch. The TUSB4041 has an internal pulldown on this terminal, so individual port power control mode is enabled by default. If the switch is set to the ON position, the terminal is pulled high and ganged mode is enabled. Since the TUSB4041PAPEVM does implement individual port power controls, this terminal should be set low.

SW2_3 (off): PWRCTL_POL_TDO Switch. The TUSB4041 has an internal pulldown on this terminal, so port power control polarity defaults to active high. If the switch is set to the ON position, the terminal is pulled high and the port power control polarity changes to active low.

SW2_4 (on): FULLPWRMGMTZ. The TUSB4041 has an internal pulldown on this terminal, so the TUSB4041 defaults to a full power management mode. If the switch is set to the ON position, the terminal is pulled high and full power management mode is disabled. In full power management mode, the TUSB4041 reports that it supports downstream port power switching in the USB descriptors it sends to the USB host. Since the TUSB4041PAPEVM implements downstream port power switching, full power management mode should be enabled.

SW2_5 (off): SCL_SMBCLK Switch. The TUSB4041 has an internal pulldown on this terminal, so the serial EEPROM/SMBUS interface is disabled. If the switch is set to the ON position, a pullup resistor is connected to the serial clock terminal to indicate that an I^2C EEPROM may be attached (along with a pullup resistor on SDA).

SW2_6 (off): SDA_SMBDAT Switch. The TUSB4041 has an internal pulldown on this terminal, so the serial EEPROM/SMBUS interface is disabled. If the switch is set to the ON position, a pullup resistor is connected to the serial clock terminal to indicate that an I^2C EEPROM may be attached (along with a pullup resistor on SCL).

SW2_7 (NC): Not connected

SW2_8 (NC): Not connected

4 EVM Installation

To install the EVM, perform the following steps:

1. Attach a 5-V, 3-A wall power source to J6. LEDs D4 should be lit.
2. Attach a USB cable between J4 and a USB host. LEDs D1, should be lit.

5 Troubleshooting

Case 1: Device function(s) are “banged out” in Device Manager.

- Make sure that the latest updates are installed for the operating system
- Make sure that the latest drivers are installed for the host controller

Case 2: The EVM does not work at all.

- Verify that all switches are in their default state and the EVM is powered on with a 5-V source with adequate current to support any bus-powered devices (3 A+).
- If installed, remove the serial EEPROM from the EEPROM socket. The EVM does not require an EEPROM to operate.
- In the case where a 12-V power supply has been attached to the EVM, the fault is non-recoverable.

A.1 TUSB4041PAPEVM Bill of Materials

This appendix contains the TUSB4041PAPEVM BOM.

Table 1. TUSB4041PAPEVM BOM

Item	Qty	Reference	Part	Manufacturer	Part Number
1	2	C1,C2	18pF	AVX	04025A180JAT2A
2	1	C3	1uF	Samsung	CL05B105KQ5NQNC
3	18	C4,C38,C40,C41,C46,C48,C50,C51,C56,C58,C66,C69,C72,C75,C77,C78,C80,C81	0.1uF	Yageo	CC0402KRX5R6BB104
4	1	C5	1uF	TDK	CL21B105KPFNNNE
5	11	C6,C9,C12,C15,C19,C22,C25,C28,C32,C83,C86	0.001uF	TDK	C0603X7R1E102K030BA
6	11	C7,C10,C13,C16,C20,C23,C26,C29,C33,C85,C88	0.01uF	Yageo	CC0201KRX7R7BB103
7	11	C8,C11,C14,C17,C21,C24,C27,C30,C34,C84,C87	0.1uF	TDK	C0603X5R0J104M
8	8	C18,C31,C35,C67,C68,C73,C74,C82	10uF	Murata Electronics	GRM31CR71C106KAC7L
9	5	C39,C47,C49,C57,C59	0.001uF	TDK	C1005X7R1H102K
10	4	C70,C71,C76,C79	150uF	Kemet	T495D157K010ATE100
11	2	D1,D4	LED Green 0805	Lite On	LTST-C171GKT
12	6	FB1,FB2,FB3,FB4,FB5,FB6	220 @ 100MHZ	Murata	BLM18PG221SN1D
13	2	GND1,GND2	TEST POINT	Wurth Electronics Inc	61300111121
14	1	JP6	Conn 2x5 shroud	3M	N2510-6002-RB
15	1	J1	Type B USB-Shield	FCI	61729-1011BLF
16	4	J2,J3,J4,J5	Type A USB-Shield	TE Connectivity AMP Connectors	292303-1
17	1	J6	2.1mm x 5.5mm	CUI Inc.	PJ-202AH (PJ-002AH)
18	3	J7,J8,J9	Header 1x2	3M	961102-6404-AR
19	6	R1,R15,R17,R18,R19,R20	1M	Rohm Semiconductor	MCR01MZPJ105
20	1	R2	90.9K	Rohm Semiconductor	RMCF0402FT90K9
21	5	R3,R26,R27,R29,R36	10K	Rohm Semiconductor	MCR01MZPF1002
22	14	R4,R5,R11,R12,R13,R14,R22,R23,R24,R25,R38,R39,R46,R47	1K	Rohm Semiconductor	MCR01MRTJ102
23	4	R6,R7,R8,R9	4.7K	Rohm Semiconductor	MCR01MZPJ472
24	0	R10,R32,R42,R43,R44,R45	10K NOPOP	Rohm Semiconductor	MCR01MZPF1002
25	2	R16,R28	330	Rohm Semiconductor	MCR01MZPJ331
26	1	R21	9.53K	Rohm Semiconductor	MCR01MRTF9531
27	1	R33	1.87K	Vishay / Dale	CRCW04021K87FKED
28	1	R34	4.99K	Vishay / Dale	CRCW04024K99FKED
29	2	SW1,SW2	8-POS 50-MIL SMT	C&K Components	TDA08H0SB1R
30	1	SW3	MS13ANW03	NKK Switches	MS13ANW03
31	1	U1	TUSB4041	Texas Instruments	TUSB4041IPAP
32	1	U2	24AA04-I/P	Microchip Technology	24AA04-I/P
33	1	U4	TPS7A4533	Texas Instruments	TPS7A4533KTT
34	1	U6	TPS74801RGW	Texas Instruments	TPS74801RGW
35	4	U7,U8,U9,U10	TPS2001C	Texas Instruments	TPS2001CDGN
36	1	Y1	ECS-24MHZ	ECS	ECS-240-20-30B-TR

A.2 TUSB4041PAPEVM Schematics

Figure 2 through Figure 4 illustrate the TUSB4041PAPEVM schematics.

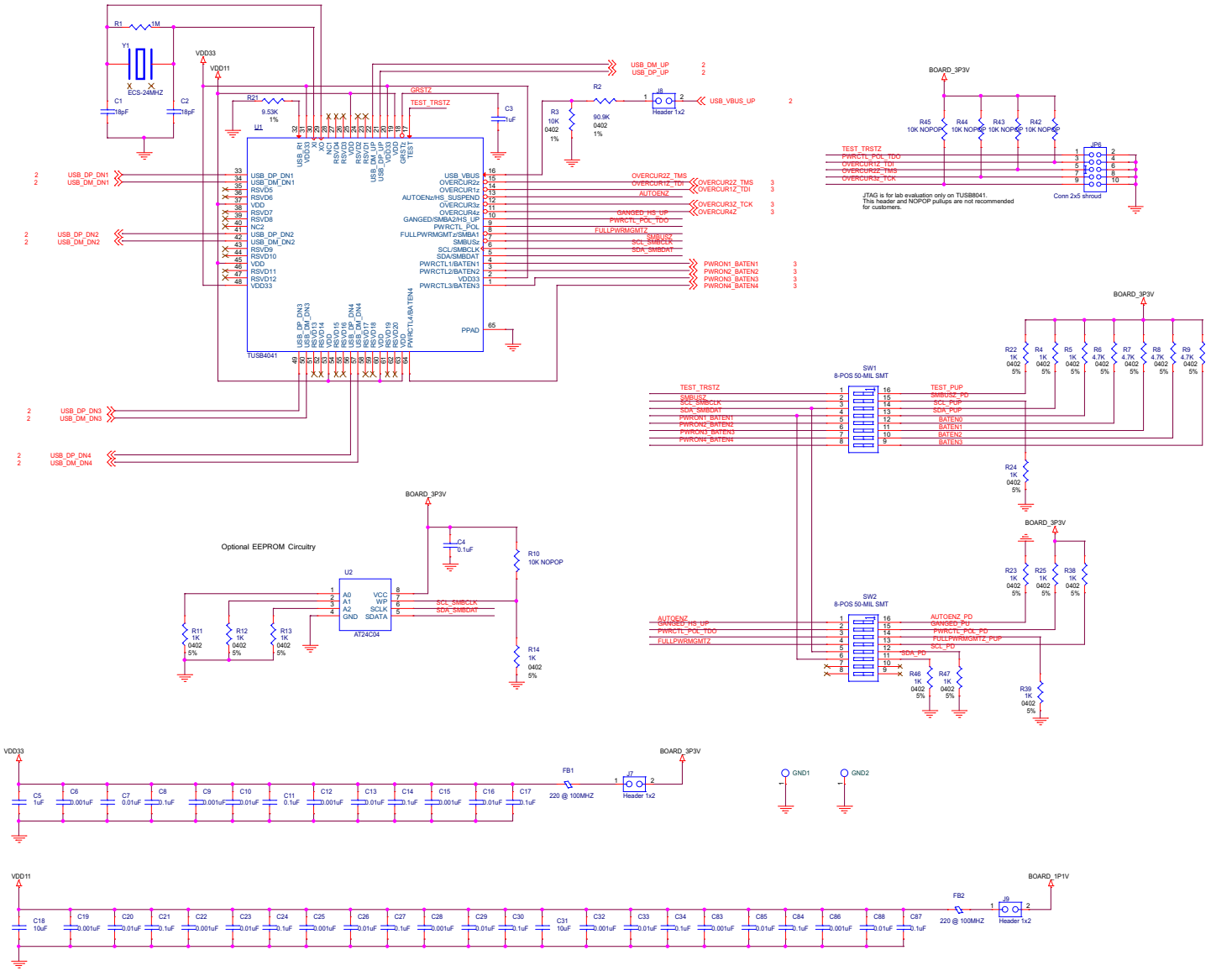

Figure 2. TUSB4041PAPEVM Schematics

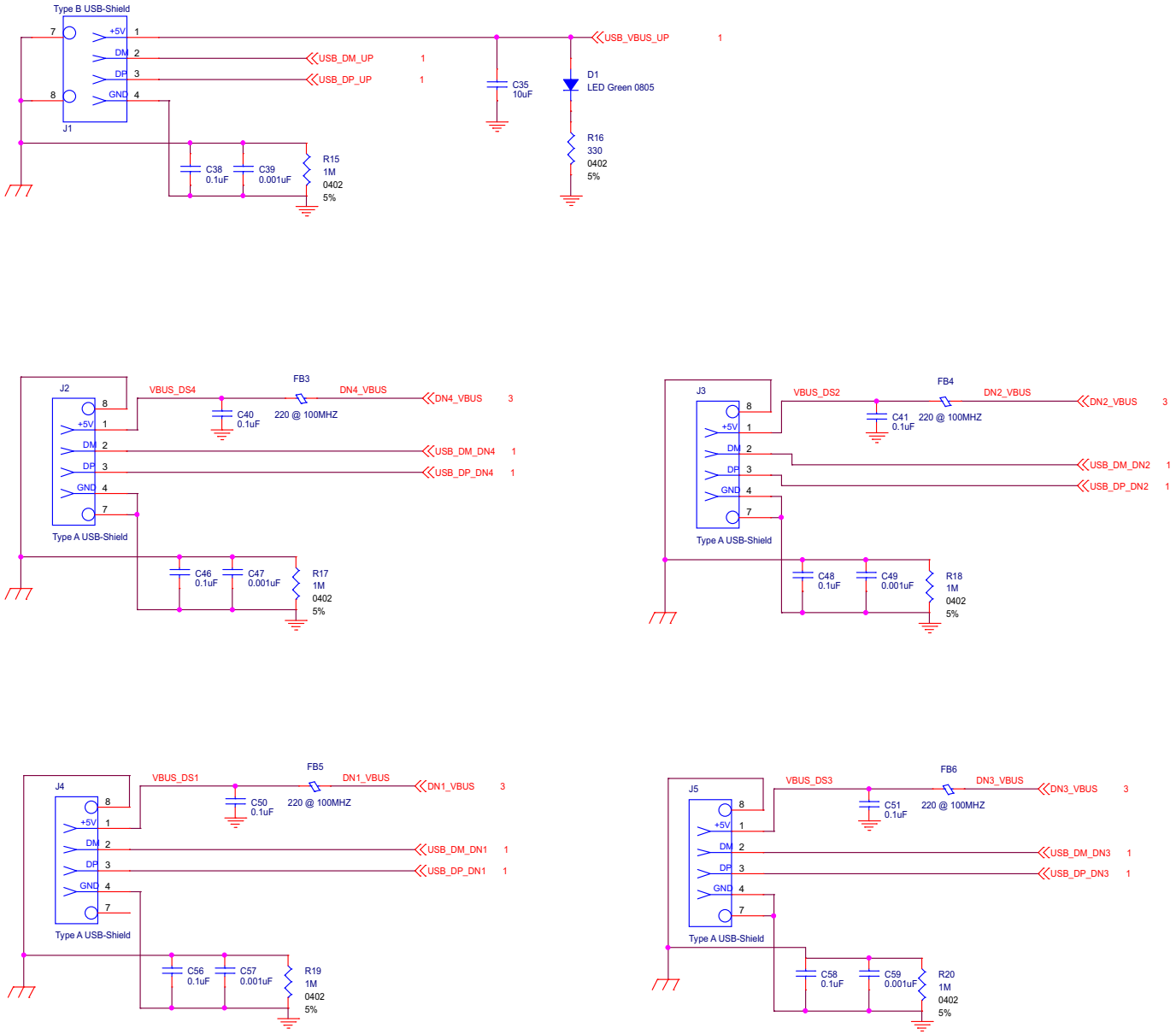

Figure 3. TUSB4041PAPEVM USB2 Connector Schematics

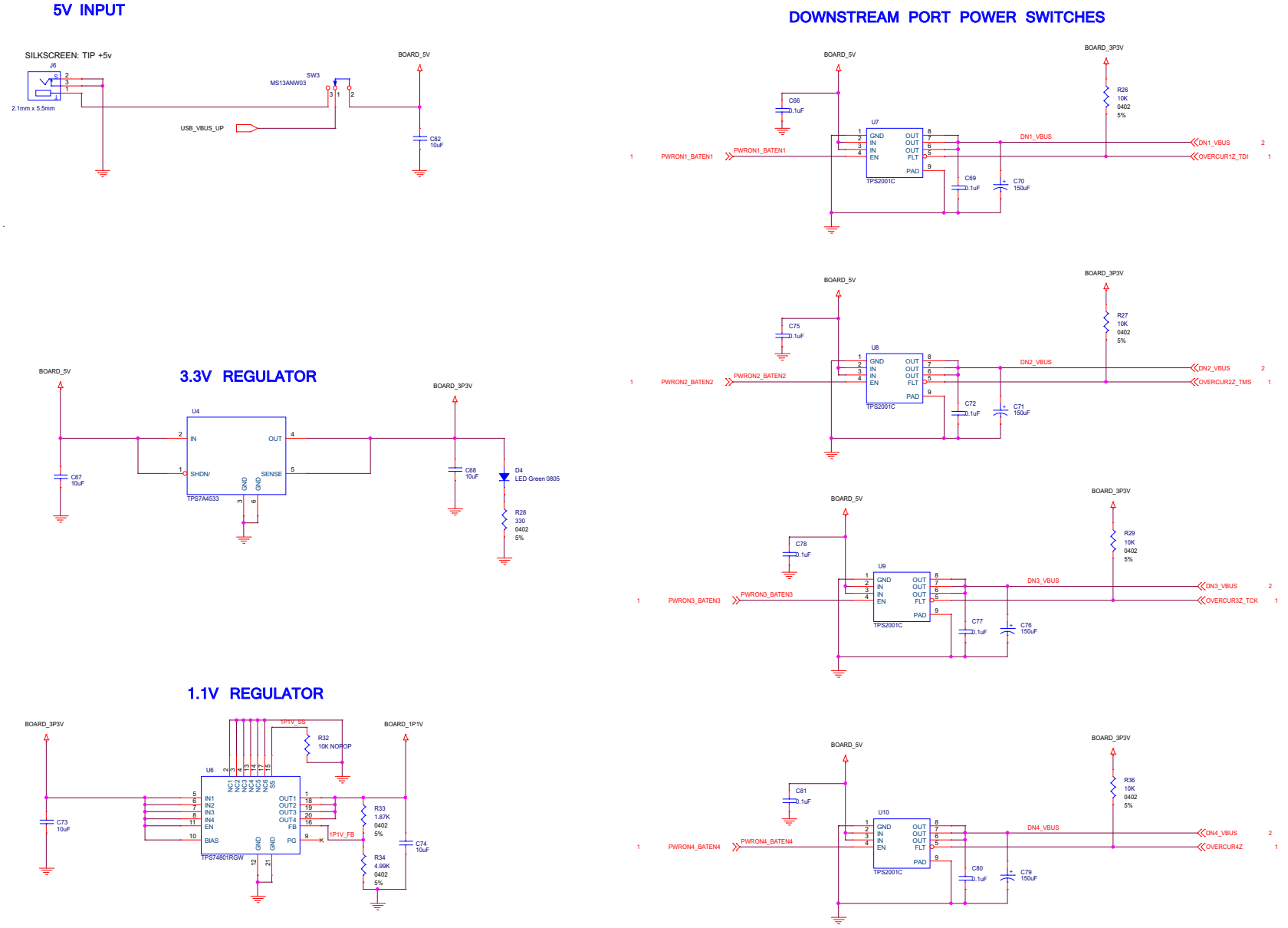

Figure 4. TUSB4041PAPEVM Power Schematics

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2015) to A Revision	Page
• Changed SW2_2 and SW2_4 descriptions	5

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