FX-700

Low Jitter Frequency Translator

Helping Customers Innovate, Improve & Grow
FX-700
FX-700

Description

The FX-700 is a crystal-based frequency translator used in communications applications where low jitter is paramount. Performance advantages include superior jitter performance, high output frequencies and small package size. Advanced custom ASIC technology results in a highly robust, reliable and predictable device. The device is packaged in a 16 pad ceramic package with a hermetic seam welded lid.

Features

- 5.0 x 7.5 mm, Hermetically sealed SMD package
- Frequency Translation to 77.760 MHz
- 3.3 Volt or 5.0 Volt Supply
- Tri-State Output allows board test
- Lock Detect
- Commercial or Industrial Temp. Range
- CMOS Output
- Absolute Pull Range Performance to +/-100 ppm
- Capable of locking to an 8 kHz pulse/BITS clock
- Product is free of lead and compliant to EC RoHS Directive

Applications

- Frequency Translation, Clock Smoothing
- Telecom - SONET/SDH/ATM
- Datacom – DSLAM, DSLAR, Access Nodes
- Base Station – GSM, CDMA
- Cable Modem Head End

Block Diagram

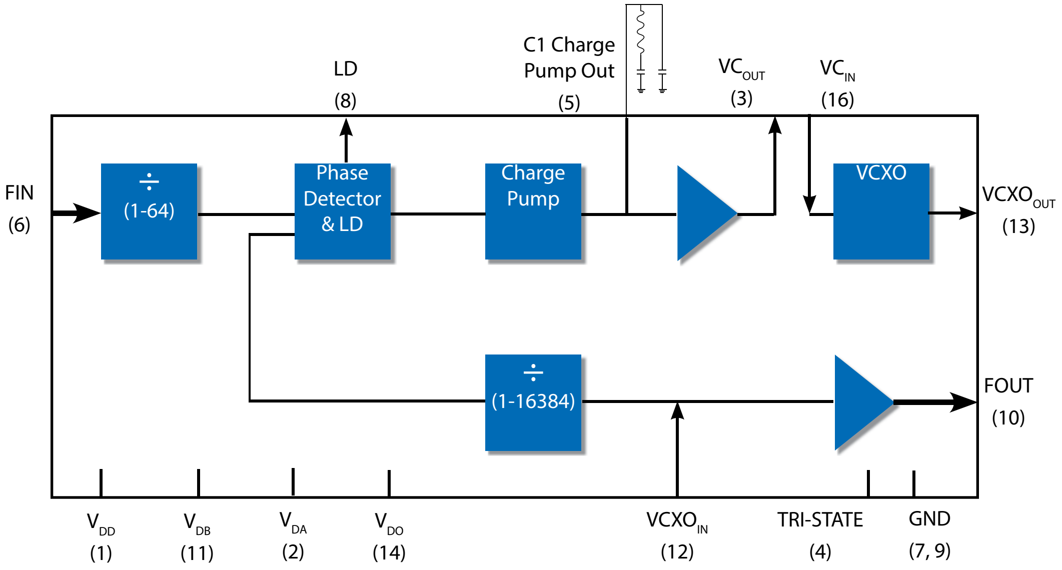

LD
(8)
C1 Charge
Pump Out
(5)
VC_OUT
(3)
VC_IN
(16)
FIN
(6)
÷
(1-64)
Phase
Detector
& LD
Charge
Pump
VCXO
VCXO_OUT
(13)
÷
(1-16384)
FOUT
(10)
V_DD
(1)
V_DB
(11)
V_DA
(2)
V_DO
(14)
VCXO_IN
(12)
TRI-STATE
(4)
GND
(7, 9)

Figure 1. Functional block diagram

Performance Specifications

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Frequency[4]					
Input Frequency	F_{IN}	0.001		77.76	MHz
Output Frequency	F_{OUT}	0.1		80.0	MHz
Capture Range (ordering option)	APR	±50, ±80, or ±100			ppm
Supply					
Voltage [1] (V_{DD}, V_{DB}, V_{DA}, V_{DO})	V_{DD}	4.5	5.0	5.5	V
	V_{DD}	2.97	3.3	3.63	V
Current [5]	I_{DD}			40	mA
Input					
Input High Voltage	V_{IH}	$0.7*V_{DD}$			V
Input Low Voltage	V_{IL}			$0.3*V_{DD}$	V
Output					
Output High Voltage	V_{OH}	$0.9*V_{DD}$			V
Outpuit Low Voltage	V_{OL}			$0.1*V_{DD}$	V
Output					
Rise Time [2]	t_R			3.0	ns
Fall Time [2]	t_F			3.0	ns
Duty Cycle [3]	SYM	40	50	60	%
Jitter Generation - 80.0MHz output	Φ_J		4.7		ps-rms
Operating Temp (ordering option)	T_{OP}	0/70, -40/85			ºC

1. A 0.01uF high frequency ceramic capacitor in parallel with a 0.1uF low frequency tantalum bypass capacitor is recommended

2. Figure 2 defines the waveform parameters. Figure 3 illustrates the standard test conditions under which these parameters are tested and specified.

3. Duty Cycle is defined as (on time/period) with Vs = Vdd/2 per Figure 2. Duty Cycle is measured with a 15pf load per Figure 3.

4. Other frequencies may be available, please contact factory.

5. Combined Current From VDD, VDO, VDA, and VDB

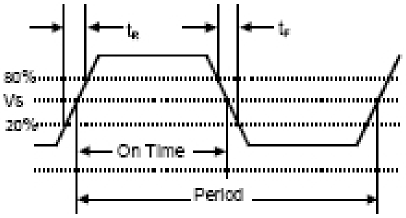


Figure 2. Output Waveform

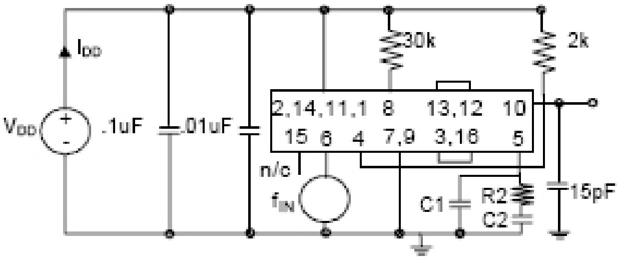


Figure 3. Output Test Conditions (25°C ±5°C)

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	7	V
Storage Temperature	T_{STR}	-55 to 125	ºC

Reliability

The FX-700 is capable of meeting the following qualification tests

Table 3. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016
Moisture Sensitivity Level	MSL1
Contact Pads	Gold (1.5 um min) over Nickel (1.9 um min)
Weight	220 mg

Handling Precautions

Although ESD protection circuitry has been designed into the the FX-700, proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance=1.5Kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes

Table 4. Predicted ESD Ratings

Model	Minimum	Conditions
Human Body Model	1500 V	MIL-STD 883, Method 3015
Charged Device Model	1000 V	JEDEC, JESD22-C101

Solder Reflow Profile

Table 5. Reflow Profile (IPC/JEDEC J-STD-020C)

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-700 device is hermetically sealed so an aqueous wash is not an issue.

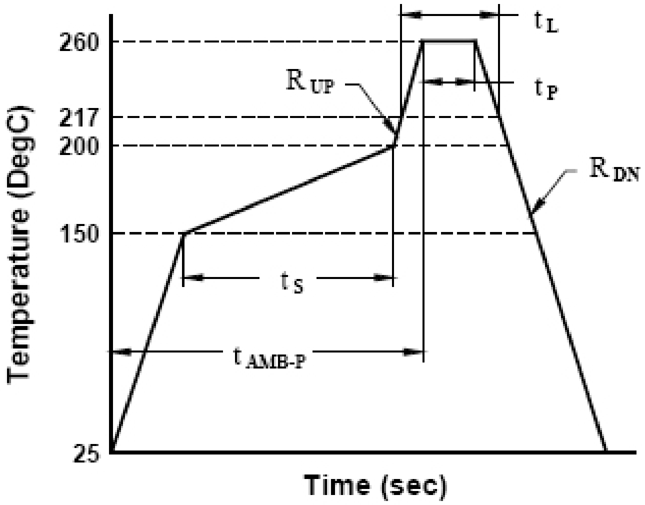
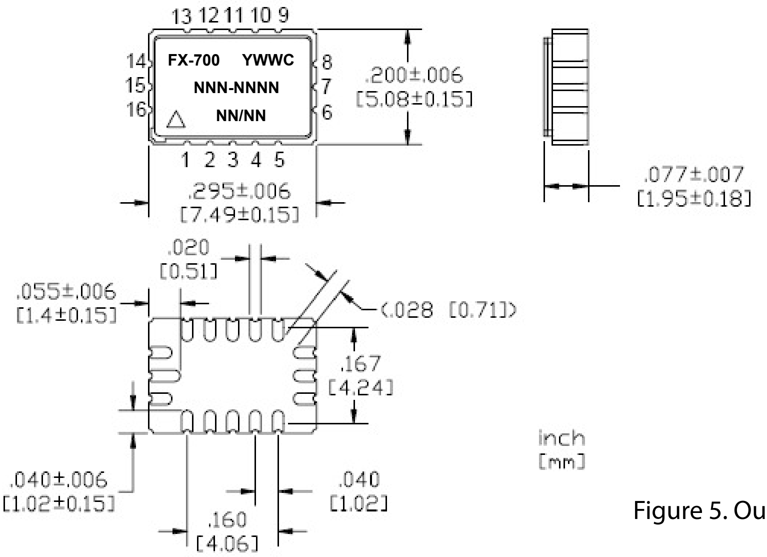


Figure 3. Suggested IR Profile

Outline Drawing

Suggested Pad Layout

Dimensions in mm.


13 12 11 10 9
14
15
16
FX-700 YWWC
NNN-NNNN
NN/NN
8
7
6
1 2 3 4 5
.200±.006
[5.08±0.15]
.295±.006
[7.49±0.15]
.077±.007
[1.95±0.18]
.020
[0.51]
.055±.006
[1.4±0.15]
(.028 [0.71])
.167
[4.24]
.040±.006
[1.02±0.15]
.160
[4.06]
.040
[1.02]
inch
[mm]

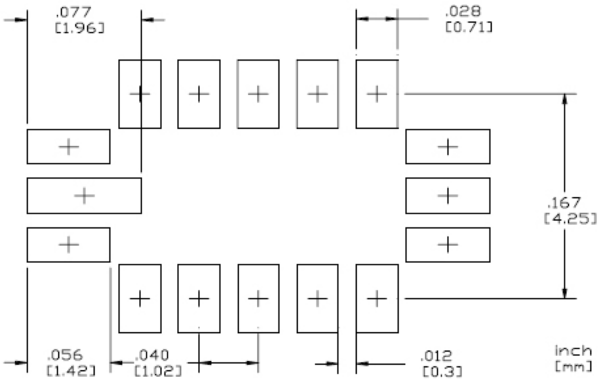

.077
[1.96]
.028
[0.71]
.167
[4.25]
.056
[1.42]
.040
[1.02]
.012
[0.3]
inch
[mm]

Figure 5. Outline Diagram

Table 7. Pin Functions		
Pad #	Symbol	Function
1	V_{DD}	Digital PLL Supply (3.3 V +/- 10% or 5.0 V +/- 10%)
2	V_{DA}	Analog PLL Supply (3.3 V +/- 10% or 5.0 V +/- 10%)
3	V_{COUT}	Control Voltage
4	Tri-state[1]	Logic Low = Output Disable / Logic High = Output Enabled
5	C1	Passive Loop Filter Node
6	FIN	Input Frequency
7	GND	Cover and Electrical Ground
8	LD[2]	Lock Detect
9	GNDB	Output Buffer Ground
10	FOUT	Output Frequency
11	VDB	Output Buffer Supply (3.3 V +/- 10% or 5.0 V +/- 10%)
12	$VCXO_{IN}$	VCXO Input
13	$VCXO_{OUT}$	VCXO Output
14	V_{DO}	VCXO Supply (3.3 V +/- 10% or 5.0 V +/- 10%)
15	N.C.	No Internal Connection Made
16	V_{CIN}	VCXO Control Voltage Input

[1] Tri-state must be driven to a logic high or a logic low, there is no internal pull up or pull down resistor (tie pin to VDD for PLL operation).

[2] LD is an open collector output requiring a 30k ohm minimum pull-up resistor to VDD. LD output is logic high under locked condition, logic low for no input at FIN, and for "out-of-lock" condition LD transitions between logic low and high at the phase detector frequency.

Tape and Reel

Table 6. Tape and Reel Information

Tape Dimensions (mm)					Reel Dimensions (mm)							
A	B	C	D	E	F	G	H	I	J	K	L	#/Reel
16	7.5	1.5	4	8	1.5	20.2	13	50	6	16.4	178	200

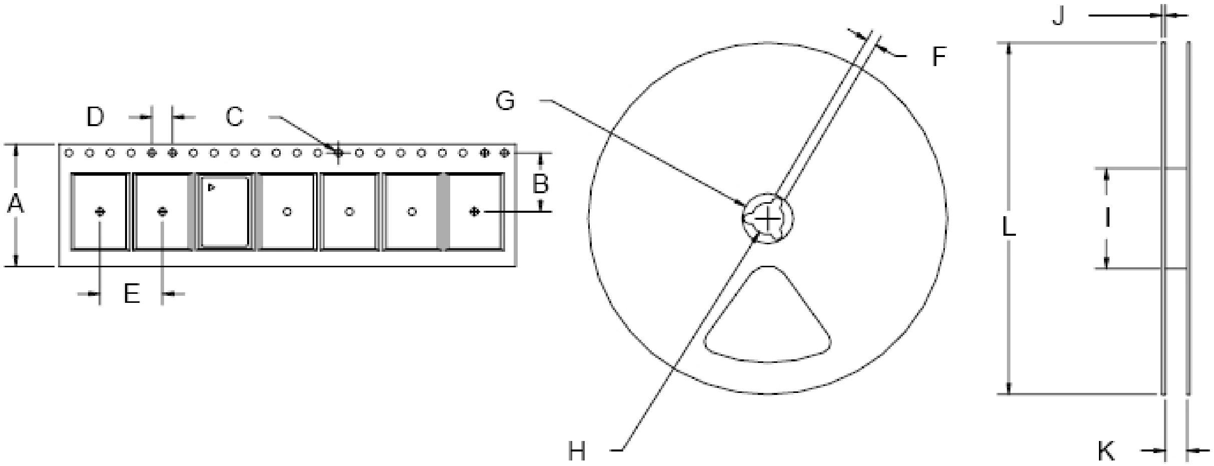


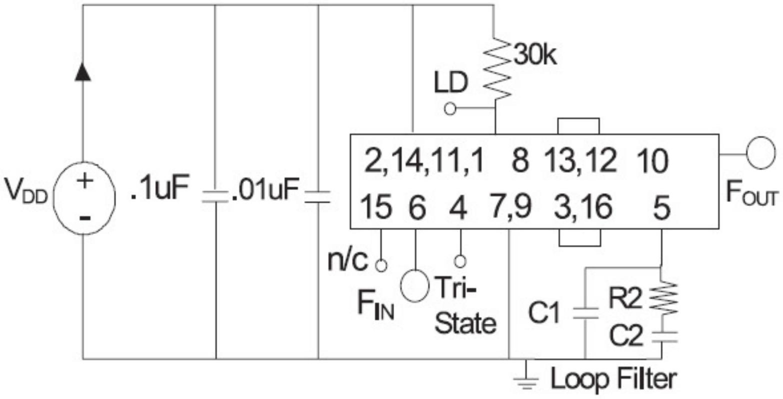
Figure 4. Tape and Reel

FX-700 Theory of Operation

The FX-700 includes an integrated phase detector, current mode charge pump, programmable frequency dividers and VCXO. The FX-700 will translate an input frequency such as 8 kHz, 1.544 MHz or 19.440 MHz to a specific output frequency which is an integer multiple (1-16384) of the input frequency and less than or equal to 77.760 MHz. For clock smoothing applications, the input frequency is typically internally divided down by a factor of 64 (2N where N = 6) by the input frequency divider and this frequency becomes an input to the phase detector. The integrated frequency dividers (factory programmed) and crystal based VCXO allows for a large range of possible frequency translations and clock smoothing applications.

The FX-700's PLL is a feedback system which forces the output frequency to lock in both phase and frequency to the input frequency. While there will be some phase error, theory states there is no frequency error. The loop filter design will dictate many key parameters such as jitter reduction, stability, lock range and acquisition time. The external second order passive loop filter is a complex impedance in parallel with the input capacitance of the VCXO. The loop filter converts the charge pump output into the VCXO's control voltage. VI's loop filter design methodology involves the calculation of the open loop gain bandwidth and corresponding phase margin to determine the optimal component values that ensure high loop stability and acceptable lock in time. As a rule of thumb, the VCXO gain is typically 100 ppm/volt and the charge pump current is typically 32 uA.

VI's Applications Engineering staff can provide the external loop filter component values required to meet specific system requirements and application.



Suggested FX-700 Circuit Configuration Drawing

Table 7. Standard Frequencies

0.00100000	A1	0.25600000	AM	3.08800000	B6	10.4142850	DV	19.6608000	DB	27.0000000	F4	41.0888870	KM	53.3300000	JU
0.00200000	AR	0.32000000	AW	3.24000000	BL	10.4582260	DU	19.6989680	DK	27.6480000	FB	41.6571440	KP	54.7460000	JL
0.00320000	AG	0.38400000	AY	3.25000000	BC	10.4872000	DN	19.7190000	DH	28.7040000	F1	41.6600000	LM	55.0000000	JX
0.00400000	A2	0.40000000	AF	3.37500000	BH	10.9490000	DG	19.9218750	ED	29.4912000	F5	41.8329130	KT	60.0000000	JR
0.00800000	A3	0.48000000	AK	3.84000000	B7	10.9500000	DJ	20.0000000	E2	29.5000000	F9	42.0000000	JB	61.3800000	KY
0.00819200	BY	0.50000000	BP	4.00000000	BN	11.1840000	DF	20.1416000	E3	30.0000000	HE	42.0101690	KV	61.4400000	J5
0.00946900	AU	0.51200000	AJ	4.09600000	B5	12.2880000	D8	20.4800000	E4	30.7200000	H1	42.5000000	JC	62.2080000	J8
0.01000000	A6	0.65545000	AE	4.19430400	CJ	12.3076860	DY	20.5444340	EF	30.8800000	HF	42.6600000	JZ	62.5000000	J9
0.01562500	AL	0.77200000	AT	5.00000000	C6	12.3520000	D1	20.7135000	E1	31.2500000	H8	44.2095440	KX	62.9145000	LE
0.01573400	AD	0.96000000	A7	5.12000000	CD	12.8000000	D2	20.8285720	EG	32.0000000	H2	44.4343000	LF	63.3600000	JJ
0.01575000	AC	1.00000000	BB	6.14400000	CG	13.0000000	D3	20.8286000	EB	32.7680000	H3	44.6218000	JW	63.8976000	JN
0.01600000	A4	1.02400000	B2	6.29140000	CC	13.5000000	DT	20.9165460	EH	33.0000000	H7	44.7360000	J3	64.0000000	JT
0.02400000	BX	1.21500000	BU	6.29145600	CF	14.8351600	DL	21.0050840	EJ	33.3330000	HC	44.9280000	JE	64.1520000	JH
0.02500000	BR	1.22880000	BK	6.31200000	C7	15.0000000	D4	22.0000000	E9	34.3680000	H6	45.1584000	JG	65.5360000	J6
0.03200000	BW	1.25000000	BG	6.48000000	C2	15.0336000	DR	22.1047720	EK	34.5600000	HB	45.8240000	JM	66.0000000	JA
0.04000000	AP	1.33330000	BF	6.75000000	CB	15.3600000	DW	22.2171000	E5	36.8640000	HG	46.0379460	LG	700000000	KB
0.04410000	AA	1.50000000	BE	7.68000000	C9	16.0000000	D9	22.5792000	E8	37.0560000	H4	46.7200000	JK	70.6560000	KC
0.04800000	AB	1.53600000	BV	7.77600000	C5	16.3840000	D5	23.5520000	EA	37.1250000	H9	46.8750000	JY	71.6100000	KF
0.04807700	AV	1.54400000	B3	8.19200000	C3	17.1840000	DE	24.0000000	EC	37.5000000	HK	48.0000000	JV	73.7280000	K8
0.05000000	BT	1.92000000	B1	9.21600000	CH	18.4320000	D7	24.5760000	E6	38.8800000	H5	49.1520000	J7	74.125000	K1
0.06400000	A5	2.00000000	B8	9.72000000	C8	18.5280000	DC	24.7040000	E7	39.0625000	HH	49.4080000	J2	74.1758000	KA
0.08000000	A9	2.04800000	B4	9.75000000	CE	18.7500000	EE	25.0000000	F7	39.3216000	HD	50.0000000	JD	74.2500000	K7
0.09600000	CN	2.30400000	BD	9.83040000	C1	19.2000000	DD	25.1658000	F8	39.8437500	HJ	50.0480000	KD	75.0000000	KH
0.10000000	AH	2.45760000	BJ	10.0000000	C4	19.3926580	DX	25.6000000	F6	40.0000000	JF	51.2000000	LL	76.8000000	K4
0.12800000	AX	2.50000000	BM	10.2300000	DP	19.4400000	D6	25.9200000	F2	40.2830630	KK	51.8400000	J4	77.760000	K2
0.24300000	A8	2.55750000	B9	10.2400000	DM	19.5312500	DZ	26.0000000	F3	40.9600000	J1	52.0000000	JP	80.000000	K9

Ordering Information

FX-700-EAE-KNKN-XX-XX

Product Family
FX: Frequency Translator

Package
700: 5.0 x 7.5 x2.0mm

Input
D: 5.0 Vdc ±10%
E: 3.3 Vdc ±10%

Output
A: CMOS

Operating Temperature
E: -40 to 85 °C
T: 0 to 70 °C

Absolute Pull Range
K: ± 50 ppm
P: ± 80 ppm
S: ± 100 ppm

Output Frequency
(See Above)

Input Frequency
(See Above)

Performance Options
N: Standard
A: Improved Phase Noise

Loop Filter BW
K: External Loop Filter

Factory Use

Note: Not all combinations will be availabe - check with the factory to determine the optimum configuration for your application

Example: FX-700-EAE-KNXN-A3-K2

* Add **_SNPB** for tin lead solder dip
Example: FX-700-EAE-KNXN-A3-K2_SNPB

Revision History

Revision Date	Approved	Description
Feb 06, 2014	TG	Updated Vectron Asia contact address
Jan 18, 2016	VN	Updated Frequency Table - Corrected typo for "A1" frequency.
Apr 18, 2017	RC	Updated Frequency Table - Include "CN" frequency
Aug 10, 2018	FB	Updated logo and contact information, added "SNPBDIP" ordering option
May 09. 2019	FB	Updated logo and contact information, added MSL1 and weight, changed SNPBDIP to SNPB

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