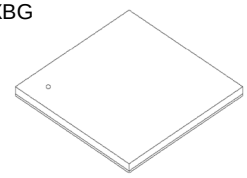
CMOS Digital Integrated Circuit Silicon Monolithic

TC9595XBG



P-VFBGA80-0707-0.65-001
Weight: 76mg (Typ.)

Overview

TC9595XBG is a bridge device that enables video streaming from a Host (application or baseband processor) over MIPI® DSI℠ or DPI℠ link to drive DisplayPort™ display panels. TC9595XBG also supports audio streaming from the host via I2S interface to the Display panels. TC9595XBG provides a low power bridge solution to efficiently translate MIPI® DSI or DPI transfers to DisplayPort™ transfers. As the DisplayPort™ uses fewer wires compared to other existing display panel standards, it simplifies the LCD connectivity. The effect of using TC9595XBG is to enable existing baseband devices supporting DSI or DPI streaming to connect to new panels supporting DisplayPort™ interface and also to connect to existing panels over longer distance using DisplayPort™ adaptors at far-end.

Features

- Translates MIPI® DSI/DPI Link video stream from Host to DisplayPort™ Link data to external display devices.
- The inputs are driven by a DSI Host with 4-Data Lanes, upto1 Gbps/lane or DPI Host with 16/18/24 bit interface upto154 MHz parallel clock.
- (Optional) Supports HDCP Digital Content Protection version 1.3 (DisplayPort™ amendment Rev1.1).
- Embeds audio information from the I2S port into the DisplayPort™ data stream.
- The output Interface consists of a DisplayPort™ Tx with a 2-lane Main Link and AUX-Ch.
- Register Configuration**:** From DSI link or I²C interface.
- Interrupt to host to inform any error status or status needing attention from Host.
- Internal test pattern (color bar) generator for DP output testing without any video (DSI/DPI) input.
- Debug/Test Port**:** I²C Slave
- **DSI Receiver**
  - ✧ MIPI® DSI**:** v1.01 / MIPI® D-PHY**:** v0.90 Compliant.
  - ✧ Up to four (4) Data Lanes with Bi-direction support on Data Lane 0.
  - ✧ Maximum speed at 1 Gbps/lane.
  - ✧ Supports Burst as well as Non-Burst Mode Video Data.
    - Video data packets are limited to one row per HSYNC period.
  - ✧ Supports video stream packets for video data transmission.
  - ✧ Supports generic long packets for accessing the chip's register set.
  - ✧ Video input data formats:
    - RGB-565, RGB-666 and RGB-888.
    - New DSI V1.02 Data Type Support**:** 16-bit YCbCr 422
  - ✧ Interlaced video mode is not supported.
- **DPI Receiver**
  - ✧ Up to 16 / 18 / 24 bit parallel data interface.
  - ✧ Maximum speed at 154 MPs (Mpixel per sec).
  - ✧ Video input data formats**:** RGB-565, RGB-666 and RGB-888.
  - ✧ Only Progressive mode supported.
- **I2S Audio Interface:** Supports one I2S port for audio streaming from the host to TC9595XBG.
  - ✧ Supports slave mode (BCLK, LRCLK & over-sampling clock input from Host).
  - ✧ Supports sampling frequencies of 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
  - ✧ Supports up to 2 audio channels.
  - ✧ Supports 16, 18, 20 or 24bits per sample.
  - ✧ Optionally inserts IEC60958 status bits and preamble bits per channel.
- **DisplayPort™ Interface:** Supports a DisplayPort™ link from TC9595XBG to display panels.
  - ✧ High speed serial bridge chip using VESA® DisplayPort™ 1.1a Standard.
  - ✧ Supports one dual-lane DisplayPort™ port for high bandwidth applications
  - ✧ Support 1.62 or 2.7 Gbps/lane data rate with voltage swings @0.4, 0.6, 0.8 or 1.2 V Support of pre-emphasis levels of 0, 3.5 and 6dB.

- ✧ Supports Audio related Secondary Data Packets.
- ✧ AUX channel supported at 1 Mbps.
- ✧ HPD support through GPIO based interrupts
- ✧ Enhanced mode supported for content protection.
- ✧ (Optional) Support HDCP encryption Version 1.3 with DisplayPort™ amendment Revision 1.1.
- ✧ Secure ASSR (Alternate Scrambler Seed Reset) support.
- ✧ Stream Policy Maker is assumed handled by the Host (software/firmware).
  - Start Link training in response to HPD & read final Link training status
  - Configure DP link for actual video streaming & start video streaming
- ✧ Link Policy maker is assumed shared between the Host and TC9595XBG chip.
  - In auto_correction = 0 mode, control link training
  - Initiate Display device capabilities read and configure TC9595XBG accordingly.
- ✧ Video timing generation as per panel requirement.
- ✧ SSCG with a 30 kHz modulation to reduce EMI.
- ✧ Built in PRBS7 Generator to test DisplayPort™ Link.

- **RGB Parallel Output Interface:**
  - ✧ RGB888 output (DisplayPort™ disabled) with only DSI input supported in this mode
  - ✧ PCLK max. = 100 MHz
  - ✧ Polarity control for PCLK, VSYNC, HSYNC & DE

- **I²C Interface:**
  - ✧ I²C slave interface for chip register set access enabled using a boot-strap option.
  - ✧ I²C compliant slave interface support for normal (100 kHz) and fast mode (400 kHz).

- **GPIO Interface:**
  - ✧ 2 bits of GPIO (shared with other digital logic).
  - ✧ Direction controllable by Host I²C accesses.

- **Clock Source:**
  - ✧ DisplayPort™ clock source is from an external clock input (13, 26, 19.2 or 38.4 MHz) or clock from DSI interface – generates all internal & output clocks to interfacing display devices.
  - ✧ Built-in PLLs generate high-speed DisplayPort™ link clock requiring no external components. These PLLs are part of the DisplayPort™ PHY.

- Clock and power management support to achieve low power states.

- **Possible modes of Operation:**
  - ✧ MODE S21**:** TC9595XBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI® DSI Host.
  - ✧ MODE P21**:** TC9595XBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI® DPI Host.
  - ✧ MODE S2P**:** TC9595XBG uses only Parallel output port and disables DisplayPort™ Tx to interface to single RGB display device. Video stream source is from MIPI® DSI Host.

- **Power supply inputs**
  - ✧ Core and MIPI® D-PHY**:** 1.2 V ± 0.06 V
  - ✧ Digital I/O**:** 1.8 V ± 0.09 V
  - ✧ DisplayPort™**:** 1.8 V ± 0.09 V
  - ✧ DisplayPort™**:** 1.2 V ± 0.06 V

- **Power Consumptions (Typical value based on estimations)**
  - ✧ Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped)**:**
    - DSI Rx**:** 0.01 mW
    - DP PHY**:** 2.34 mW
    - PLL9**:** 0.01 mW
    - Core**:** 0.96 mW
    - Rest**:** 0.01 mW
  - ✧ Normal operation (1920 × 1080 resolution with DSI-Rx in 4-lane @925 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane)**:**
    - DSI Rx**:** 21.79 mW
    - DP PHY**:** 142.70 mW
    - PLL9**:** 2.42 mW
    - Core**:** 87.64 mW
    - IOs**:** 1.68 mW

- **Package**
  - 0.65mm ball pitch, 80 balls, 7 × 7 mm BGA package

- **AEC-Q100 qualified with the following definition**
  - Grade3: -40 °C to 85 °C ambient operating temperature range

Table of contents

REFERENCES 6
1. Overview 7
2. Features 10
3. External Pins 13
3.1. TC9595XBG External Pins 13
3.2. TC9595XBG Ball Mapping 15
4. Package 16
5. Electrical Characteristics 17
5.1. Absolute Maximum Ratings 17
5.2. Operating Condition 17
5.3. DC Electrical Specification 18
5.4. Power Consumption (Typical value based on estimation) 18
6. Revision History 19
RESTRICTIONS ON PRODUCT USE 20

Table of Figures

Figure 1.1 System Overview with TC9595XBG in MODE_S21 Configuration 8
Figure 1.2 System Overview with TC9595XBG in MODE_P21 Configuration 9
Figure 1.3 System Overview with TC9595XBG in MODE_S2P Configuration 9
Figure 3.1 TC9595XBG 80-ball Layout 15
Figure 4.1 80 ball TC9595XBG package 16

List of Tables

Table 2.1 TC9595XBG operational modes summary with panel size support information 12
Table 2.2 Panel Size v/s Data link required by TC9595XBG in DSI input case 12
Table 2.3 Panel Size v/s Data link required by TC9595XBG in DPI input case 12
Table 3.1 TC9595XBG Functional Signal List for 80-ball Package 13
Table 5.1 Absolute Maximum Ratings 17
Table 5.2 Operating Condition 17
Table 5.3 DC Electrical Specification 18
Table 6.1 Revision History 19

- MIPI® is a registered trademark owned by MIPI Alliance. DSI[SM] and DPI[SM] are service marks of MIPI Alliance.
- DisplayPort is trademark owned by the Video Electronics Standards Association (VESA®) in the United States and other countries.
- All other company names, product names, and service names may be trademarks or service names of their respective companies.

NOTICE OF DISCLAIMER

The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled by any of the authors or developers of this material or MIPI®. The material contained herein is provided on an “AS IS” basis and to the maximum extent permitted by applicable law, this material is provided AS IS AND WITH ALL FAULTS, and the authors and developers of this material and MIPI® hereby disclaim all other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of negligence.

All materials contained herein are protected by copyright laws, and may not be reproduced, republished, distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express prior written permission of MIPI® Alliance. MIPI®, MIPI® Alliance and the dotted rainbow arch and all related trademarks, tradenames, and other intellectual property are the exclusive property of MIPI® Alliance and cannot be used without its express prior written permission.

ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR MIPI® BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL, CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL, WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is further notified that MIPI®: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document; and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance with the contents of this Document. The use or implementation of the contents of this Document may involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents, patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI®. MIPI® does not make any search or investigation for IPR, nor does MIPI® require or request the disclosure of any IPR or claims of IPR as respects the contents of this Document or otherwise.

Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

MIPI Alliance, Inc.
c/o IEEE-ISTO
445 Hoes Lane
Piscataway, NJ 08854
Attn: Board Secretary

This Notice of Disclaimer applies to all DSI input and processing paths related descriptions throughout this document.

REFERENCES

1. MIPI® DSI, "MIPI® Alliance Specification for DSI Version 1.01.00 - 21 February 2008"
2. MIPI® DPI, “MIPI Alliance Standard for Display Pixel Interface (DPI-2) Version 2.00 – 15 September 2005”
3. MIPI® D-PHY, “DRAFT MIPI® Alliance Specification for D-PHY Version 0.91.00 – r0.01 14-March-2008"
4. VESA® DisplayPort™ Standard (Version 1, Revision 1A January 11, 2008)
5. VESA® embedded DisplayPort™ (eDP) Standard (Version 1.1 October 23, 2009)
6. Digital Content Protection LLC, HDCP (Version 1.3 with DisplayPort™ amendment Revision 1.1, Jan. 15 2010)
7. I^2C bus specification, version 2.1, January 2000, Philips Semiconductor
8. Draft CEA-861-C, A DTV Profile for Uncompressed High Speed Digital Interfaces (Doc. Number: CEA-861rCv9.pdf (PNXXX)) Date: 05/04/2005
9. DisplayPort™ PHY DFT Strategy Specification Rev 1.3

1. Overview

The DSI/DPI to DisplayPort™ converter (TC9595XBG) is a bridge device that enables video streaming from a Host (application or baseband processor) over MIPI® DSI or DPI link to drive DisplayPort™ display panels. TC9595XBG also supports audio streaming from the host via I2S interface to the Display panels. TC9595XBG provides a low power bridge solution to efficiently translate MIPI® DSI or DPI transfers to DisplayPort™ transfers. As the DisplayPort™ uses fewer wires compared to other existing display panel standards, it simplifies the LCD connectivity. The effect of using TC9595XBG is to enable existing baseband devices supporting DSI or DPI streaming to connect to new panels supporting DisplayPort™ interface and also to connect to existing panels over longer distance using DisplayPort™ adaptors at far-end.

The chip can be configured through the DSI link by sending write/read register commands through DSI Generic Long Write packets. It can also be configured through the I^2C Slave interface.

The DSI-RX receiver supports from 1 to 4-Lane configurations at bit rate up to 1 Gbps per lane. Host can transmit video in continuous video streaming mode. Host controls video timing by sending video frame and line sync events together with video pixel data; video data transmission can be burst or non-burst. Since the chip integrates only a small video buffer, Host still has to take care of transmitting pixel data at appropriate video line time in order to avoid buffer overflow (or underflow).

The DPI-Rx receiver supports 16, 18 or 24 bits parallel interface along with the required control signals for the Pixel clock and HSYNC/VSYNC/DE.

The TC9595XBG also supports content protection using HDCP copy protection(Optional).

The DisplayPort™ transmitter supports data throughput at 1.62 Gbps or 2.7 Gbps per lane of main link.

TC9595XBG supports three configuration modes. These modes mainly differ based on the source of input stream and output interface..

- Mode_S21**:** A system configuration where TC9595XBG may typically be used is shown in Figure 1.1. In this configuration, the TC9595XBG can support displays with resolution up to WUXGA (1920×1200) at 24bit, 60 fps or WUXGA (1920×1200) at 18bit, 60 fps. Video stream source is from DSI Host.

- Mode_P21**:** A system configuration where TC9595XBG may typically be used is shown in Figure 1.2. This is similar to the Mode_S21 except that the video stream source is from DPI Host. In this configuration, the TC9595XBG can support displays with resolution up to WUXGA (1920×1200) at 24bit, 60 fps.

- Mode_S2P**:** A system configuration where TC9595XBG may typically be used is shown in Figure 1.3. In this mode, DisplayPort™ output is not used and the chip rather behaves as a DSI to RGB convertor. In this system, TC9595XBG could be connected to a single display. In this configuration, the TC9595XBG can support displays with resolution up to WXGA (1280x800 or 1366x768). Maximum output PCLK is 100MHz. Video stream source is from DSI Host.

The chip supports power management to conserve power when its functions are not in use. Host manages the chip's power consumption modes by using ULPS messages over DSI link during DPI input mode.

The following figures show all these modes, where TC9595XBG, display panels and a Host are connected in target Reference system for mobile large display panel applications.

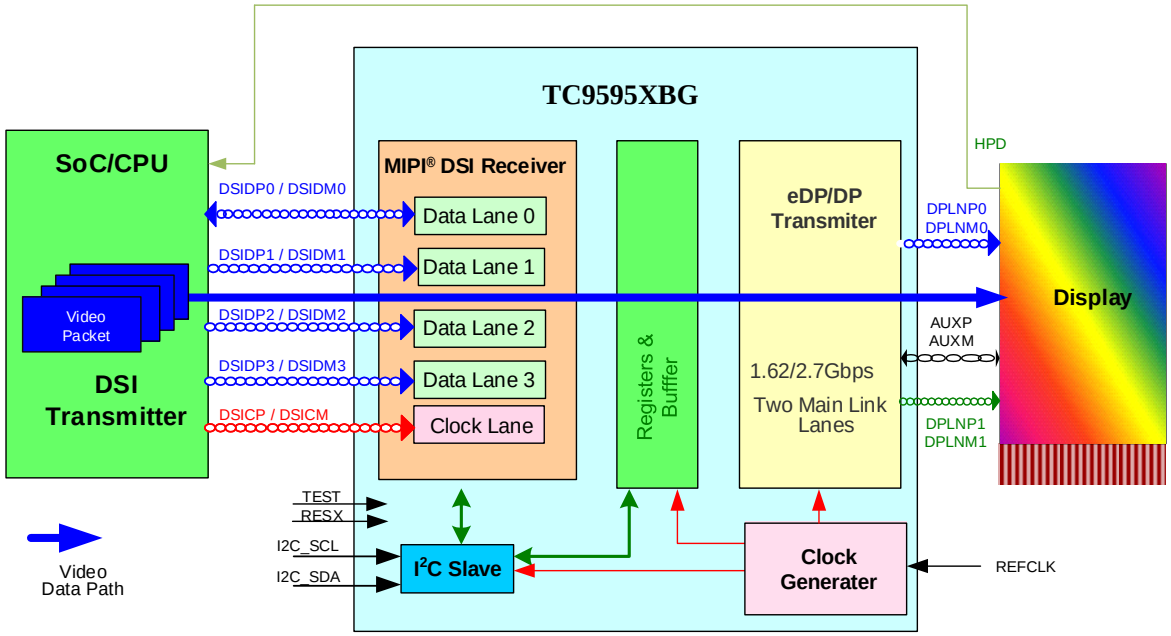


Figure 1.1 System Overview with TC9595XBG in MODE_S21 Configuration

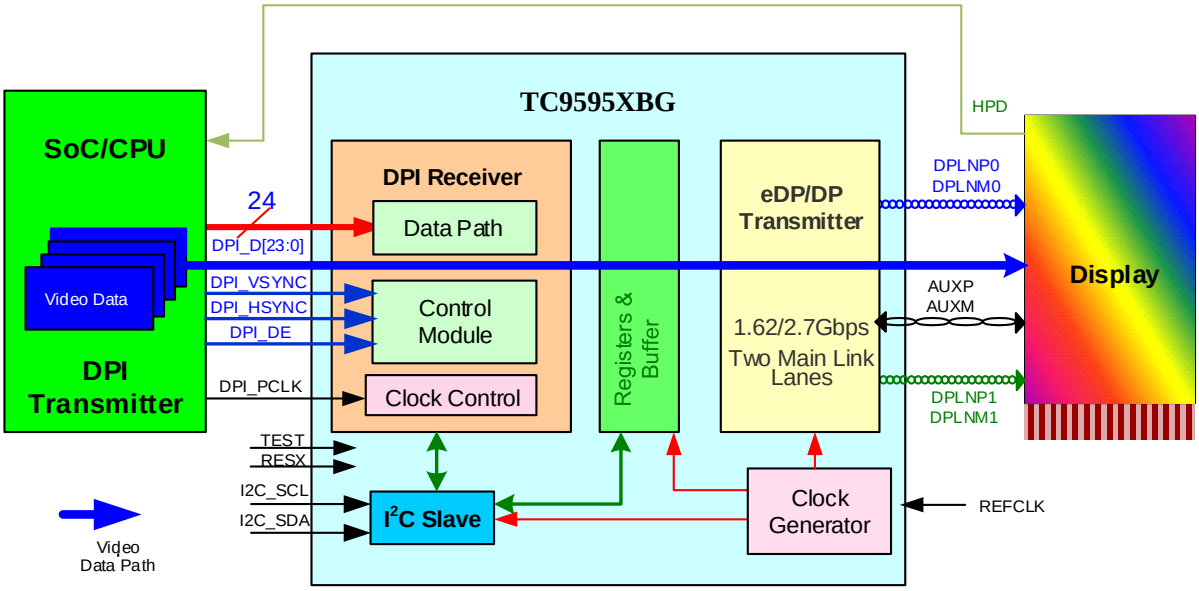


Figure 1.2 System Overview with TC9595XBG in MODE_P21 Configuration

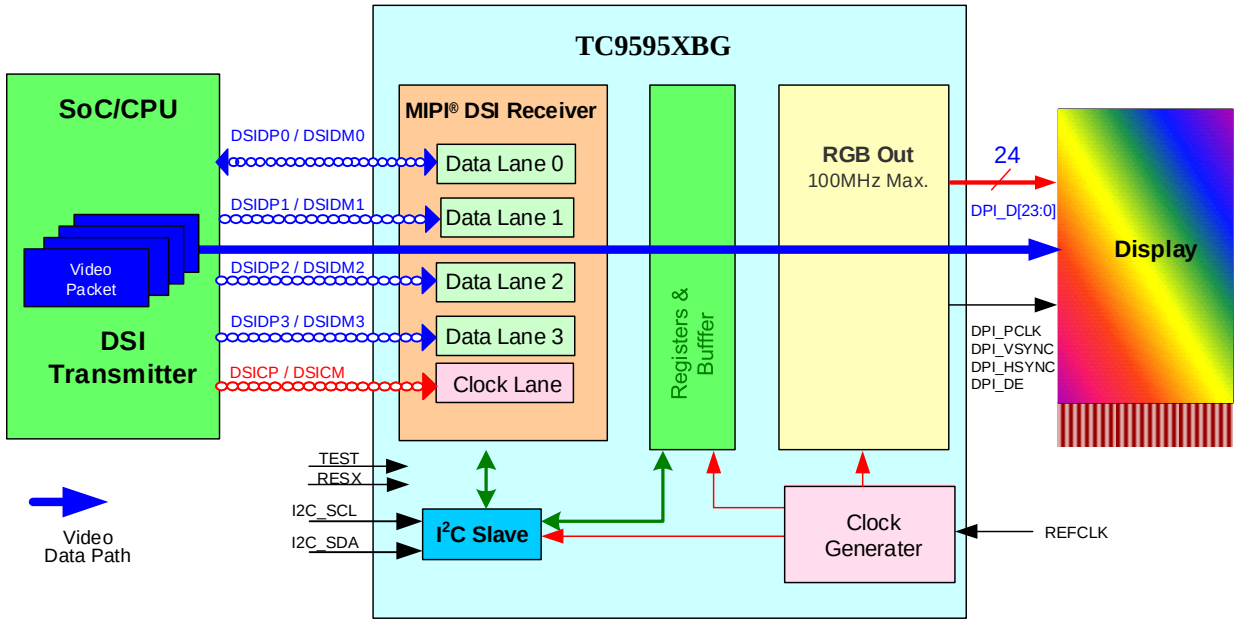


Figure 1.3 System Overview with TC9595XBG in MODE_S2P Configuration

2. Features

Below are the main features supported by TC9595XBG.

- Translates MIPI® DSI/DPI Link video stream from Host to DisplayPort™ Link data to external display devices.
- The inputs are driven by a DSI Host with 4-Data Lanes, upto1 Gbps/lane or DPI Host with 16/18/24 bit interface upto154 MHz parallel clock.
- (Optional) Supports HDCP Digital Content Protection version 1.3 (DisplayPort™ amendment Rev1.1).
- Embeds audio information from the I2S port into the DisplayPort™ data stream.
- The output Interface consists of a DisplayPort™ Tx with a 2-lane Main Link and AUX-Ch.
- Register Configuration**:** From DSI link or I^2C interface.
- Interrupt to host to inform any error status or status needing attention from Host.
- Internal test pattern (color bar) generator for DP output testing without any video (DSI/DPI) input.
- Debug/Test Port**:** I^2C Slave
- **DSI Receiver**
  - ✧ MIPI® DSI**:** v1.01 / MIPI® D-PHY**:** v0.90 Compliant.
  - ✧ Up to four (4) Data Lanes with Bi-direction support on Data Lane 0.
  - ✧ Maximum speed at 1 Gbps/lane.
  - ✧ Supports Burst as well as Non-Burst Mode Video Data.
    - Video data packets are limited to one row per HSYNC period.
  - ✧ Supports video stream packets for video data transmission.
  - ✧ Supports generic long packets for accessing the chip's register set.
  - ✧ Video input data formats**:**
    - RGB-565, RGB-666 and RGB-888.
    - New DSI V1.02 Data Type Support**:** 16-bit YCbCr 422
  - ✧ Interlaced video mode is not supported.
- **DPI Receiver**
  - ✧ Up to 16 / 18 / 24 bit parallel data interface.
  - ✧ Maximum speed at 154 MPs (MPixel per sec).
  - ✧ Video input data formats**:** RGB-565, RGB-666 and RGB-888.
  - ✧ Only Progressive mode supported.
- **I2S Audio Interface:** Supports one I2S port for audio streaming from the host to TC9595XBG.
  - ✧ Supports slave mode (BCLK, LRCLK & over-sampling clock input from Host).
  - ✧ Supports sampling frequencies of 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
  - ✧ Supports up to 2 audio channels.
  - ✧ Supports 16, 18, 20 or 24 bits per sample.
  - ✧ Optionally inserts IEC60958 status bits and preamble bits per channel.
- **DisplayPort™ Interface:** Supports a DisplayPort™ link from TC9595XBG to display panels.
  - ✧ High speed serial bridge chip using VESA® DisplayPort™ 1.1a Standard.
  - ✧ Supports one dual-lane DisplayPort™ port for high bandwidth applications.
  - ✧ Support 1.62 or 2.7 Gbps/lane data rate with voltage swings @0.4, 0.6, 0.8 or 1.2 V.
  - ✧ Support of pre-emphasis levels of 0, 3.5 and 6 dB.
  - ✧ Supports Audio related Secondary Data Packets.
  - ✧ AUX channel supported at 1 Mbps.
  - ✧ HPD support through GPIO based interrupts
  - ✧ Enhanced mode supported for content protection.
  - ✧ (Optional) Supports HDCP encryption Version 1.3 with DisplayPort™ amendment Revision 1.1.
  - ✧ Secure ASSR (Alternate Scrambler Seed Reset) support for embedded DisplayPort™ panels
  - ✧ Stream Policy Maker is assumed to be handled by the Host (software/firmware).
    - Start Link training in response to HPD & read final Link training status
    - Configure DP link for actual video streaming & start video streaming
  - ✧ Link Policy maker is assumed shared between the Host and TC9595XBG chip.
    - In auto_correction = 0 mode, control link training
    - Initiate Display device capabilities read and configure TC9595XBG accordingly.

- ✧ Video timing generation as per panel requirement.
- ✧ SSCG with a 30 kHz modulation to reduce EMI.
- ✧ Built in PRBS7 Generator to test DisplayPort™ Link.

- **RGB Parallel Output Interface:**
  - ✧ RGB888 output (DisplayPort™ disabled) with only DSI input supported in this mode
  - ✧ PCLK max. = 100 MHz
  - ✧ Polarity control for PCLK, VSYNC, HSYNC & DE
- **I²C Interface:**
  - ✧ I²C slave interface for chip register set access enabled using a boot-strap option.
  - ✧ I²C compliant slave interface support for normal (100 kHz) and fast mode (400 kHz).
- **GPIO Interface:**
  - ✧ 2 bits of GPIO (shared with other digital logic).
  - ✧ Direction controllable by Host I²C accesses.
- **Clock Source:**
  - ✧ DisplayPort™ clock source is from an external clock input (13, 26, 19.2 or 38.4 MHz) or clock from DSI interface – generates all internal & output clocks to interfacing display devices.
  - ✧ Built-in PLLs generate high-speed DisplayPort™ link clock requiring no external components. These PLLs are part of the DisplayPort™ PHY.
- Clock and power management support to achieve low power states.
- **Possible modes of Operation:**
  - ✧ MODE S21**:** TC9595XBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI® DSI Host.
  - ✧ MODE P21**:** TC9595XBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI® DPI Host.
  - ✧ MODE S2P**:** TC9595XBG uses only Parallel output port and disables DisplayPort™ Tx to interface to single RGB display device. Video stream source is from MIPI® DSI Host.
- **Power supply inputs**
  - ✧ Core and MIPI® D-PHY**:** 1.2 V ± 0.06 V
  - ✧ Digital I/O**:** 1.8 V ± 0.09 V
  - ✧ DisplayPort™**:** 1.8 V ± 0.09 V
  - ✧ DisplayPort™**:** 1.2 V ± 0.06 V
- **Power Consumptions (Typical value based on estimations)**
  - ✧ Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped)**:**
    - DSI Rx**:** 0.01 mW
    - DP PHY**:** 2.34 mW
    - PLL9**:** 0.01 mW
    - Core**:** 0.96 mW
    - Rest**:** 0.01 mW
  - ✧ Normal operation (1920×1080 resolution with DSI-Rx in 4-lane @925 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane)**:**
    - DSI Rx**:** 21.79 mW
    - DP PHY**:** 142.70 mW
    - PLL9**:** 2.42 mW
    - Core**:** 87.64 mW
    - IOs**:** 1.68 mW
- **Package**
  - 0.65mm ball pitch, 80 balls, 7 × 7 mm BGA package
- **AEC-Q100 Qualified with the following definition**
  - Grade3: -40°C to 85°C ambient operating temperature range

Table 2.1 TC9595XBG operational modes summary with panel size support information

Mode	Input Configuration		Register Access Method	Max Panel size example
	DSI input	DPI input		
S21	Active	-	DSI or I^2C	WUXGA 18bpp @ 60fps WUXGA 24bpp @ 60fps
P21	-	Active	I^2C	WUXGA 24bpp @ 60fps

Tables below provide an idea of different panel sizes that can be supported by using different data link lane configurations.

Table 2.2 Panel Size v/s Data link required by TC9595XBG in DSI input case

Frame Size			FPS	Pixel Clock (MHz)	RGB666				RGB888			
		With Overhead			Bit Rate (Gbps)	# DSI Data lanes	# DP Main links		Bit Rate (Gbps)	# DSI Data lanes	# DP Main links	
							1.62G	2.7G			1.62G	2.7G
XGA	1024×768	1184×790	60	56	1.01	2	1	1	1.34	2	2	1
WXGA+ / WSXGA	1440×900	1600×926	60	89	1.60	2	2	1	2.13	3	2	1
SXGA+	1400×1050	1560×1080	60	89	1.82	2	2	1	2.43	3	2	2
WSXGA+	1680×1050	1840×1080	60	119	2.15	3	2	1	2.86	3	–	2
UXGA	1600×1200	1760×1235	60	130	2.35	3	2	2	3.13	4	–	2
WUXGA	1920×1200	2080×1235	60	154	2.77	3	–	2	3.70	4	–	2

Table 2.3 Panel Size v/s Data link required by TC9595XBG in DPI input case

Frame Size			FPS	Pixel Clock (MHz)	DPI Support 154 MHz PCLK	RGB666			RGB888		
		With Overhead				Bit Rate (Gbps)	# DP Main links		Bit Rate (Gbps)	# DP Main links	
							1.62G	2.7G		1.62G	2.7G
XGA	1024×768	1184×790	60	56	Yes	1.01	1	1	1.34	2	1
WXGA+ / WSXGA	1440×900	1600×926	60	89	Yes	1.60	2	1	2.13	2	1
SXGA+	1400×1050	1560×1080	60	89	Yes	1.82	2	1	2.43	2	2
WSXGA+	1680×1050	1840×1080	60	119	Yes	2.15	2	1	2.86	–	2
UXGA	1600×1200	1760×1235	60	130	Yes	2.35	2	2	3.13	–	2
WUXGA	1920×1200	2080×1235	60	154	Yes	2.77	–	2	3.70	–	2

Note: These are the formats commonly used by displays. Support for other sizes is possible as long as they satisfy the maximum data rate constraints on the DSI and DisplayPort™ link interfaces.

Note: Throughout the rest of the document, "DP" is used to denote "DisplayPort™". Both these words have been used interchangeably and refer to the VESA® DisplayPort™ specification as mentioned in the references.

3. External Pins

3.1. TC9595XBG External Pins

TC9595XBG uses an 80ball package. Following table gives the signals of TC9595XBG and their function.

Table 3.1 TC9595XBG Functional Signal List for 80-ball Package

Group	Pin Name	I/O	Type	Function	Note
System: Reset, Clock, Mode select, Test (9)	RESX	I	Sch	System Reset – active Low 0: Reset 1: Normal operation	—
	REFCLK	I	Sch	13, 26, 19.2 or 38.4 MHz 50ps phase jitter p2p/ WC duty cycle 40-60%	—
	INT	O	N	Interrupt to Host – active High 0: No interrupt is generated 1: Interrupt is generated	4mA
	DISABLE_ASSR	I	N	ASSR control 0: Enable ASSR 1: Disable ASSR	—
	MODE[1:0]	I	N	Mode Selection pins MODE_0: 0: REFCLK is source of internal DP PLL 1: When REFCLK="0", DSI clock is source of internal DP PLL. When REFCLK="1", DPI PCLK is source of internal DP PLL. MODE_1: When MODE_0="1" & REFCLK="0" this pin will be effective. 0: DSI clock/2/7 is source of internal DP PLL. 1: DSI clock/2/9 is source of internal DP PLL.	—
	TEST	I	N	Test Pin - active high 0: Normal operation 1: Test mode	—
	TEST3	O	N	Test Pin, Open	—
	VPGM0	NA	—	eFUSE programming voltage. Connect to GND	—
DSI Rx (10)	DSICP	I	MIPI®-PHY	MIPI®-DSI Rx Clock Lane Pos.	—
	DSICM	I	MIPI®-PHY	MIPI®-DSI Rx Clock Lane Neg.	—
	DSIDP0	I/O	MIPI®-PHY	MIPI®-DSI Rx Data Lane Pos.	—
	DSIDM0	I/O	MIPI®-PHY	MIPI®-DSI Rx Data Lane Neg.	—
	DSIDP[3:1]	I	MIPI®-PHY	MIPI®-DSI Rx Data Lane Pos.	—
	DSIDM[3:1]	I	MIPI®-PHY	MIPI®-DSI Rx Data Lane Neg.	—
DP Out (8)	DPLNP[1:0]	O	DP-PHY	embedded DisplayPort™ Output Main Link Pos.	—
	DPLNM[1:0]	O	DP-PHY	embedded DisplayPort™ Output Main Link Neg.	—
	DPAUXP	I/O	DP-PHY	embedded DisplayPort™ Output AUX Channel Pos	—
	DPAUXM	I/O	DP-PHY	embedded DisplayPort™ Output AUX Channel Neg	—
	PREC_RES[1:0]	I	DP-PHY	Precision Resistance (3kΩ @ 1%) connection	—
DPI Tx/Rx (28)	DPI_PCLK	I/O	N	DPI Pixel Clock (max 154 MHz) (default: Input)	4mA
	DPI_VSYNC	I/O	N	DPI Vertical Sync (default: Input)	4mA
	DPI_HSYNC	I/O	N	DPI Horizontal Sync (default: Input)	4mA
	DPI_DE	I/O	N	DPI Data Enable (default: Input)	4mA
	DPI_D [23:0]	I/O	N	DPI Parallel Data (default: Input)	4mA
I^2C (3)	I2C_SCL	OD	Sch	I^2C Clock	—
	I2C_SDA	OD	Sch	I^2C Data	4mA

	I2C_ADR_SEL	I	N	I²C Slave Address Select 0: Slave address=7'b1101_000 1: Slave address=7'b0001_111	—
I2S (4)	SD/I2S_OSCLK	I	N	I2S Over Sampling Clock	—
	I2S_BCLK	I	N	I2S Bit Clock (max 12.5 MHz)	—
	I2S_LRCLK	I	N	I2S sample clock (max 192 kHz)	—
	I2S_DATA	I	N	I2S Data	—
GPIO (2)	GPIO[1:0]	OD	5T-OD	GPIO or Test Control *Note1 GPIO[1:0] can be used for HPD support	4mA
POWER (10)	VDDC (1.2V)	NA	—	VDD for Internal Core (2)	—
	VDDS (1.8V)	NA	—	VDDS for IO Ring power supply (1)	—
	VDD_PLL18 (1.8V)	NA	—	VDD for DP PHY PLLs (1)	—
	VDD_DP18 (1.8V)	NA	—	VDD for DP PHY Main Channels (2)	—
	VDD_PLL912 (1.2V)	NA	—	VDD for PLL9 (1)	—
	VDD_DP12 (1.2V)	NA	—	VDD for DP PHY (2)	—
	VDD_DSI12 (1.2V)	NA	—	VDD for the MIPI® DSI PHY (1)	—
GROUND (6)	VSS	NA	—	Ground (Core, DSI, I/O) (3)	—
	VSS_DP	NA	—	Ground (DP) (3)	—

Note 1: Pins with multiplexed Functional mode functions.

N: Normal IO
PHY: Either DP analog front end or MIPI® D-PHY
Sch: Schmitt trigger input
OD: Open drain
5T-OD: 5 V tolerant bi-direction buffer with Open drain

3.2. TC9595XBG Ball Mapping

The mapping of TC9595XBG signals to the external pins is given in the following figure. (BGA array)

Top View

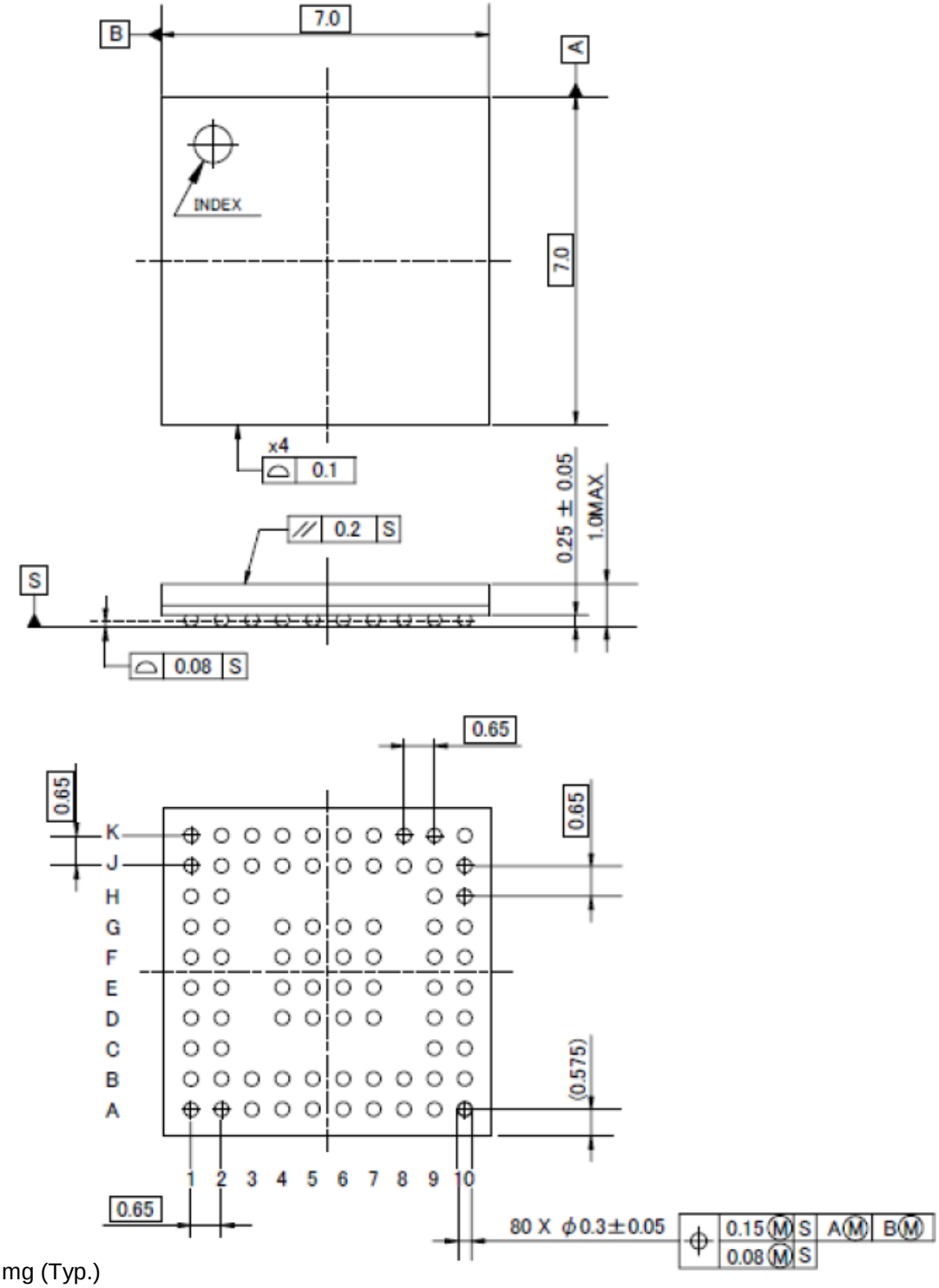
	1	2	3	4	5	6	7	8	9	10
A	INT	GPIO0	DPI_VSYNC	DPI_D0	VDDC	VDDC	DPI_D3	VDDS	I2C_SDA	I2C_SCL
B	DSIDM0	DSIDP0	DPI_DE	DPI_HSYNC	DPI_D1	DPI_D2	DPI_D4	DPI_D7	DPI_D5	DPI_D6
C	DSIDM1	DSIDP1							DPI_D9	DPI_D8
D	DSICM	DSICP		I2S_LRCLK	I2S_BCLK	SD/ I2S_OSCLK	I2S_DATA		DPI_D13	DPI_D14
E	VDD_DSI12	I2C_ADR_SEL		VSS	TEST3	VPGM0	DPI_D10		DPI_D16	DPI_D15
F	DSIDM2	DSIDP2		VSS	VSS	TEST	DPI_D11		DPI_D17	DPI_D18
G	DSIDM3	DSIDP3		VSS_DP	VSS_DP	VSS_DP	DPI_D12		DPI_D19	DPI_PCLK
H	PREC_RES0	DISABLE_ASSR							DPI_D20	DPI_D21
J	PREC_RES1	MODE1	DPLNP0	VDD_DP12	MODE0	DPLNP1	GPIO1	DPAUXP	RESX	DPI_D23
K	REFCLK	VDD_DP18	DPLNM0	VDD_DP12	VDD_PLL18	DPLNM1	VDD_DP18	DPAUXM	VDD_PLL912	DPI_D22

Figure 3.1 TC9595XBG 80-ball Layout

4. Package

The package for TC9595XBG is described in the figure below.

Unit: mm



Weight: 76 mg (Typ.)

Figure 4.1 80 ball TC9595XBG package

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS/VSS_DP= 0 V reference

Table 5.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (VDD_PLL18, VDD_DP18)	VDD18	-0.3 to +3.5	V
Supply voltage (VDDC, VDD_PLL12, VDD_PLL912, VDD_DP12, VDD_DSI12)	VDD12	-0.3 to +2.0	V
Supply voltage (VDDS)	VDD18S	-0.3 to +3.5	V
Input voltage	VIN	-0.3 to VDDS+0.3	V
Output voltage	VOUT	-0.3 to VDDS+0.3	V
Storage temperature	Tstg	-40 to +125	°C

5.2. Operating Condition

VSS/VSS_DP = 0 V reference

Table 5.2 Operating Condition

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (VDD_PLL18, VDD_DP18)	VDD18	1.71	1.8	1.89	V
Supply voltage (VDDC, VDD_PLL12, VDD_PLL912, VDD_DP12, VDD_DSI12)	VDD12	1.14	1.2	1.26	V
Supply voltage (VDDS)	VDD18S	1.71	1.8	1.89	V
Operating frequency (internal)	Fopr	—	—	200	MHz
Operating temperature	Ta	-40	—	+85	°C

5.3. DC Electrical Specification

VSS/VSS_DP = 0V reference

Table 5.3 DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage High level CMOS input Note1	VIH	0.7 VDDS	—	VDDS	V
Input voltage Low level CMOS input Note1	VIL	0	—	0.3 VDDS	V
Input voltage High level CMOS Schmitt Trigger Note1	VIHS	0.7 VDDS	—	VDDS	V
Input voltage Low level CMOS Schmitt Trigger Note1	VILS	0	—	0.3 VDDS	V
Output voltage High level Note1, Note2	VOH	0.8 VDDS	—	VDDS	V
Output voltage Low level Note1, Note2	VOL	0	—	0.2 VDDS	V
Input leak current High level	IIH1 (Note3)	-10	—	10	µA
Input leak current Low level	IIL1 (Note4)	-10	—	10	µA
	IIL2 (Note5)	-200	—	-10	µA

Note1: VDD18S within operating condition.

Note2: Output current value is according to each IO buffer specification. Output voltage changes with output current value.

Note3: Normal pin, or Pull-up I/O pin applied VDD18S supply voltage to input pin

Note4: Normal pin applied VSS (0 V) to input pin

Note5: Pull-up I/O pin applied VSS (0 V) to input pin

5.4. Power Consumption (Typical value based on estimation)

Typical power consumption as measured for the power-down modes and for normal operation are provided below:

- Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped):
  - ✧ DSI Rx: 0.01 mW
  - ✧ DP PHY: 2.34 mW
  - ✧ PLL9: 0.01 mW
  - ✧ Core: 0.96 mW
  - ✧ Rest: 0.01 mW

- Normal operation (1920×1080 resolution with DSI-Rx in 4-lane @925 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane):
  - ✧ DSI Rx: 21.79 mW
  - ✧ DP PHY: 142.70 mW
  - ✧ PLL9: 2.42 mW
  - ✧ Core: 87.64 mW
  - ✧ IOs: 1.68 mW

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
0.1	2020-05-19	Newly released
1.1	2021-06-23	Add “AEC-Q100 Qualified” to Features Modified Table 5.1 and Table 5.2
1.2	2022-08-23	Corrected Typos in Features

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, and lifesaving and/or life supporting medical equipment. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**