Click here for production status of specific part numbers.

MAX20056B

Integrated, 6-Channel High-Brightness LED Driver with Very Wide PWM Dimming Ratio and Phase Shifting for Automotive Displays

General Description

The MAX20056B is a 6-channel LED driver that integrates a DC-DC switching boost/SEPIC controller and six 120mA current sinks. A current-mode switching DC-DC controller provides the necessary voltage to the strings of HB LEDs.

An internal current-mode switching DC-DC controller supports boost, SEPIC, or coupled-inductor buck-boost topologies and operates in a programmable frequency range between 400kHz and 2.2MHz. Current-mode control provides fast response and simplifies loop compensation. An adaptive output-voltage-adjustment scheme minimizes power dissipation in the LED current sinks.

An external resistor sets the channel currents to the same value in the range of 20mA to 120mA. The device features logic-controlled pulse-width modulation (PWM) dimming with minimum pulse widths as low as 500ns, and either phase-shifted LED strings or standard dimming control. When phase shifting is enabled, each string is turned on at a different time, reducing the input and output ripple as well as audible noise. With phase shifting disabled, each current sink is turned on at the same time and allows parallel connection of current sinks for > 120mA per string.

Applications

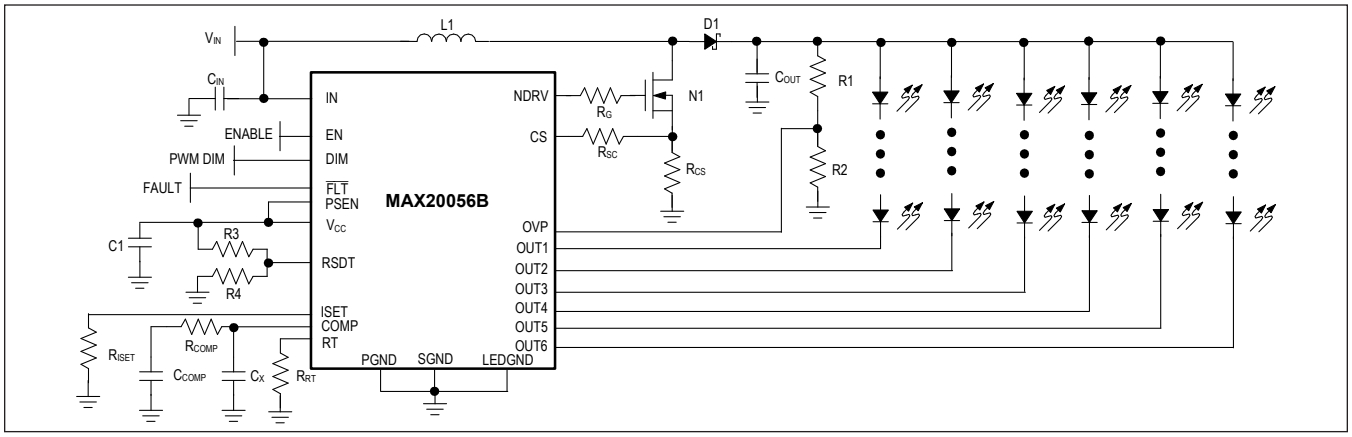
- Automotive Dashboards
- Automotive Central Information Displays
- Automotive Head-Up Displays
- Automotive Navigation Systems

Benefits and Features

- Robust with Respect to EMC and Automotive Battery Transients
  - Wide 4.5V to 42V Input Operating Range Powers HB LEDs for Medium-to-Large-Sized LCD Displays in Automotive and Display Backlight Applications
  - Withstands Automotive Load-Dump Events Up to 52V
  - Integrated Spread Spectrum
- Spread-Spectrum Mode Reduces Emission at the Switching Frequency and its Harmonics
  - EMI Reduction Features Include Spread-Spectrum Modulation (±6% of the Switching Frequency Set by a Resistor Connected Between RT and SGND)
- Phase-Shift Dimming of LED Strings
  - Reduced Input and Output Ripple/Audible Noise
- Wide Contrast Ratio Ideal for High-Quality TFT and Head-Up Displays
  - PWM Dimming Ratio of 10,000:1 at 200Hz
- Robust with Respect to Temperature and Fault Conditions
  - LED-Open/Short Detection
  - Overtemperature Protection
  - Low Shutdown Current (< 15µA) through Enable Pin
  - Thermally Enhanced 24-Pin TSSOP Package
  - -40°C to +125°C AEC-Q100 compliance

***Ordering Information* appears at end of data sheet.**

Simplified Schematic



Absolute Maximum Ratings

IN, EN, OUT_, OVP to SGND .....-0.3V to +52V
V_{CC} to SGND .....-0.3V to the lower of (IN + 0.3V) and +6V
$\overline{FLT}$, DIM, RSDT, PSEN to SGND .....-0.3V to +6V
CS, NDRV, COMP, ISET, RT to SGND .... -0.3V to (V_{CC} + 0.3V)
PGND, LEDGND to SGND .....-0.3V to +0.3V
LEDGND to PGND .....-0.3V to +0.3V
NDRV Peak Current (< 100ns) .....±5A
NDRV Continuous Current .....±100mA
OUT_ Continuous Current.....±150mA
V_{CC} Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate 30.27mW/°C above +70°C) 2421.3mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ...+33.04°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....+2.34°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = V_{EN} = 12V, R_{RT} = 20kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{IN}		4.5		42	V
Input Voltage Range	V_{IN}	V_{IN} = V_{CC}	4.5		5.5	V
Quiescent Supply Current	I_Q	V_{DIM} = 5V, V_{OVP} = 1.3V, OUT1–OUT6 unconnected		6	10	mA
Standby Supply Current	I_{SH}	V_{IN} = 12V, V_{EN} = 0V		8	15	µA
Undervoltage Lockout		V_{IN} rising	3.8	4.15	4.5	V
Undervoltage Lockout		V_{IN} falling	3.3		4	V
V_{CC} REGULATOR						
Output Voltage	V_{CC}	5.75V < V_{IN} < 42V, I_{VCC} = 1mA to 10mA, C_{VCC} = 2.2µF	4.8	5	5.2	V
Dropout Voltage	VCC_{DROP}	V_{IN} = 4.5V, I_{VCC} = 10mA		0.1	0.3	V
V_{CC} Undervoltage Lockout		V_{CC} rising	4.1	4.2	4.3	V
V_{CC} Undervoltage Lockout		V_{CC} falling	3.6		3.95	V
Short-Circuit Current Limit	$IVCC_{SC}$	V_{CC} shorted to SGND		65		mA

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 20kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BOOST/SEPIC CONTROLLER						
Switching Frequency	f_{SW}	R_{RT} = 20kΩ, frequency dithering disabled	360	400	440	kHz
		R_{RT} = 52.3kΩ, frequency dithering disabled	630	700	770	kHz
		R_{RT} = 76.8kΩ, frequency dithering disabled	900	1000	1100	kHz
		R_{RT} = 113kΩ, frequency dithering disabled	1170	1300	1430	kHz
		R_{RT} = 158kΩ, frequency dithering disabled	1440	1600	1760	kHz
		R_{RT} = 210kΩ, frequency dithering disabled	1710	1900	2090	kHz
		R_{RT} = 301kΩ, frequency dithering disabled	1980	2200	2420	kHz
RT Input Current	I_{RT}	V_{RT} = 0V	4.65	5	5.35	µA
Minimum Off-Time	t_{OFF_MIN}	R_{RT} = 20kΩ	100	150	200	ns
		R_{RT} = 301kΩ		40	70	ns
Frequency Dither				±6		%
SLOPE COMPENSATION						
Peak Slope-Compensation Current-Ramp Magnitude	I_{SLOPE}	Current ramp added to CS input	42.5	50	57.5	µA
CS LIMIT COMPARATOR						
CS Threshold Voltage	V_{CS_MAX}	(Note 3)	400	420	440	mV
CS Limit Comparator-to-NDRV Propagation Delay	$t_{CS\text{-}TO\text{-}NDRV}$	Including leading-edge blanking time		100		ns
ERROR AMPLIFIER						
OUT_ Window-Comparator Threshold	V_{OUT_UP}	$V_{OUT\_}$ rising	1.05	1.12	1.2	V
	V_{OUT_DOWN}	$V_{OUT\_}$ falling	0.75	0.82	0.9	V
Transconductance	gs_M		440	680	880	µS
COMP Sink Current	$I_{COMPSINK}$	V_{COMP} = 2V	160	400	800	µA
COMP Source Current	$I_{COMPSOURCE}$	V_{COMP} = 1V	160	400	800	µA
MOSFET DRIVER						
NDRV On-Resistance	R_{NDRV}	I_{SINK} = 30mA		0.8	1.6	Ω
		I_{SOURCE} = 30mA		1.5	3	Ω
Rise Time	t_{NDRVR}	C_{LOAD} = 1nF		8		ns
Fall Time	t_{NDRVF}	C_{LOAD} = 1nF		8		ns

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 20kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED CURRENT SINK						
ISET Resistance Range	$R_{ISETRANGE}$		12.5		75	kΩ
Full-Scale OUT_ Output Current	$I_{OUT\_}$	R_{ISET} = 12.5kΩ	115	120	124	mA
		R_{ISET} = 15kΩ	95	100	104	mA
		R_{ISET} = 30kΩ	47	50	52	mA
		R_{ISET} = 75kΩ	17.5	20	22.5	mA
ISET Output Voltage	V_{ISET}		1.225	1.25	1.275	V
Current Regulation Between Strings	I_{OUT_MATCH}	$I_{OUT\_}$ = 120mA	-1.9		+1.9	%
		$I_{OUT\_}$ = 50mA	-3		+3	%
OUT_ Leakage Current	I_{OUT_LEAK}	$V_{OUT\_}$ =48V, V_{DIM} = 0V, OUT1–OUT6 shorted together			3	µA
$I_{OUT\_}$ Rise Time	t_{IOUT_R}	10% to 90% $I_{OUT\_}$		150		ns
$I_{OUT\_}$ Fall Time	t_{IOUT_F}	90% to 10% $I_{OUT\_}$		50		ns
LOGIC INPUTS AND OUTPUTS						
DIM Input High Level	V_{THDIMH}		2.1			V
DIM Input Low Level	V_{THDIML}				0.8	V
DIM Pullup Current	I_{DIMPU}			5		µA
EN Input Logic-High	V_{THENH}		2.1			V
EN Input Logic-Low	V_{THENL}				0.8	V
EN Input Current	I_{ENIN}		-1		+1	µA
PSEN Input Logic-High	$V_{THPSENH}$		2.1			V
PSEN Input Logic-Low	$V_{THPSENL}$				0.8	V
PSEN Input Current	I_{PSENIN}		-1		+1	µA
$\overline{FLT}$ Output Low Voltage	$V_{\overline{FLT}L}$	I_{SINK} = 5mA			0.4	V
$\overline{FLT}$ Output Leakage Current	$I_{\overline{FLT}LEAK}$	$V_{\overline{FLT}}$ = 5.5V			1	uA
LED FAULT DETECTION						
LED Short-Detection Threshold	V_{THRSDT}	V_{RSDT} = 2V	7.2	8	8.8	V
LED Disable-Short Threshold	$V_{THRSDTDIS}$		2.65	2.8	2.9	V
Short-Detection Comparator Delay	t_{RSDT}			9		µs
RSDT Leakage Current	$I_{RSDTLEAK}$	V_{RSDT} = 2.25V	-600		+600	nA
OUT_ Check LED Source Current			48	60	72	µA
OUT_ Short-to-GND Detection Threshold		(Note 4)	250	300	350	mV
OUT_ Unused Detection Threshold			1.15	1.25	1.35	V

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, R_{RT} = 20kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

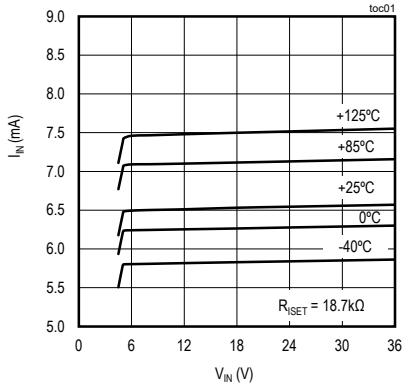
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OVERVOLTAGE PROTECTION						
Overvoltage-Trip Threshold	V_{THOVP}	V_{OVP} rising	1.2	1.23	1.26	V
Overvoltage Hysteresis	V_{OVPHYS}			70		mV
OVP Input Bias Current	I_{OVPIN}	0 < V_{OVP} < 1.3V	-500		+500	nA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	$T_{SHUTDOWN}$			165		°C
Thermal-Shutdown Hysteresis	T_{HYS}			15		°C

Note 2: 100% tested at T_A = +25°C. All limits over temperature are guaranteed by design, not production tested.
Note 3: CS threshold includes slope-compensation ramp magnitude.
Note 4: The OUT_ short-to-ground threshold is also used in normal mode as the open-string-detection threshold.

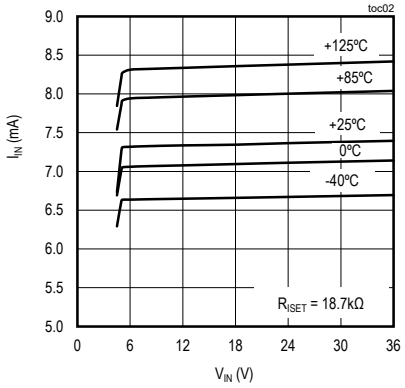
Typical Operating Characteristics

(V_{IN} = V_{EN} = 12V, T_A = +25°C, unless otherwise noted.)

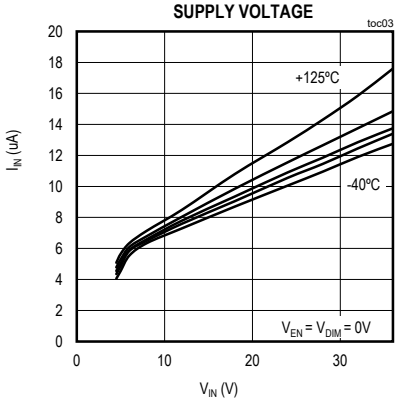
SUPPLY CURRENT vs. SUPPLY VOLTAGE (400kHz SWITCHING FREQUENCY)



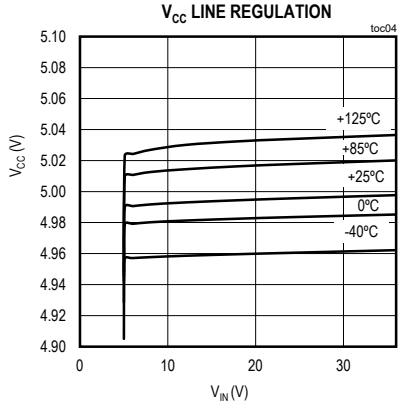
SUPPLY CURRENT vs. SUPPLY VOLTAGE (2.2MHz SWITCHING FREQUENCY)



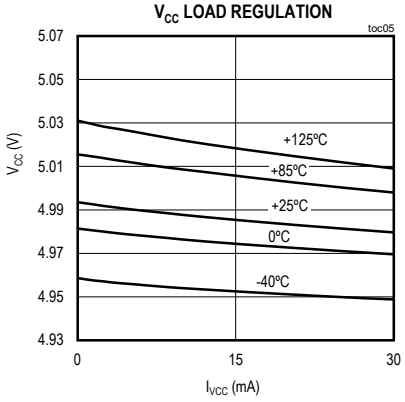
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



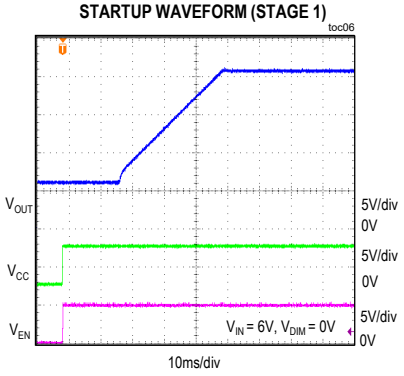
V_{CC} LINE REGULATION



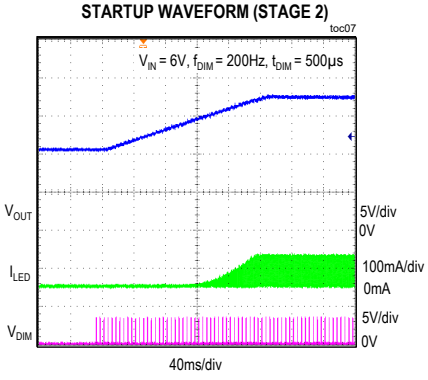
V_{CC} LOAD REGULATION



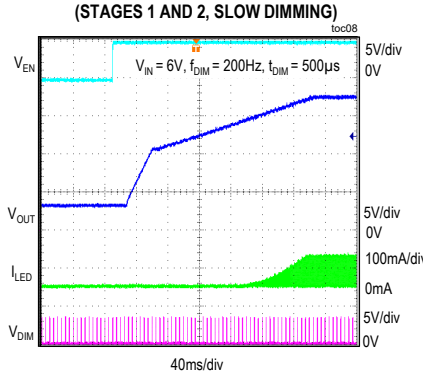
STARTUP WAVEFORM (STAGE 1)



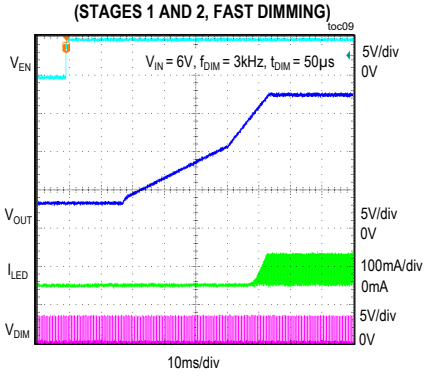
STARTUP WAVEFORM (STAGE 2)



STARTUP WAVEFORM (STAGES 1 AND 2, SLOW DIMMING)



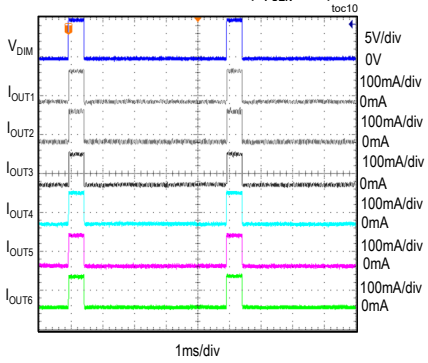
STARTUP WAVEFORM (STAGES 1 AND 2, FAST DIMMING)



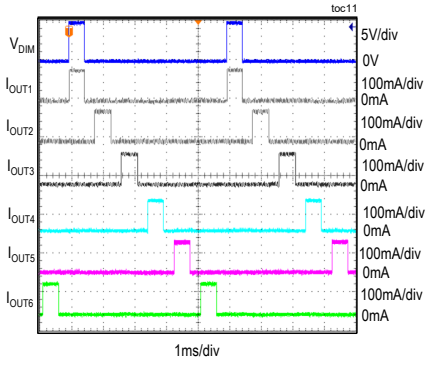
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 12V, T_A = +25°C, unless otherwise noted.)

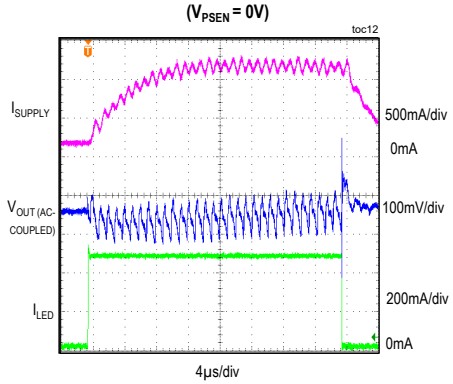
DIMMING WAVEFORM (V_{PSEN} = 0V)



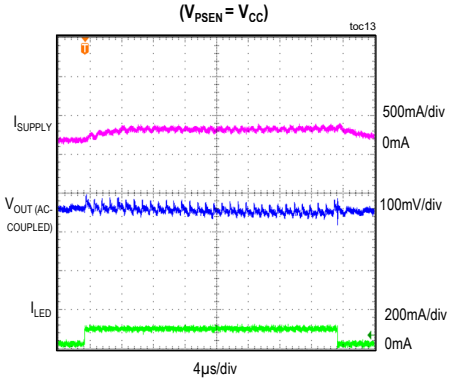
DIMMING WAVEFORM (V_{PSEN} = V_{CC})



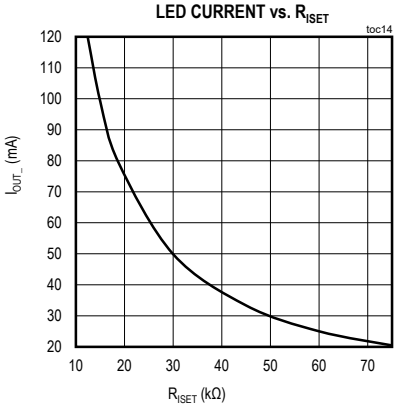
OUTPUT RIPPLE (V_{PSEN} = 0V)



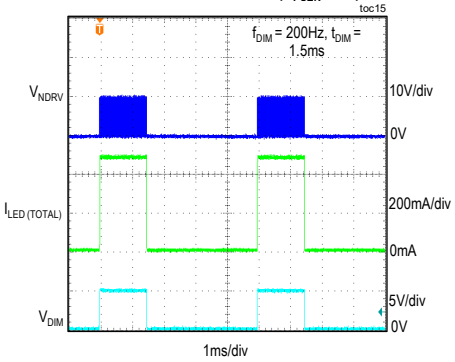
OUTPUT RIPPLE (V_{PSEN} = V_{CC})



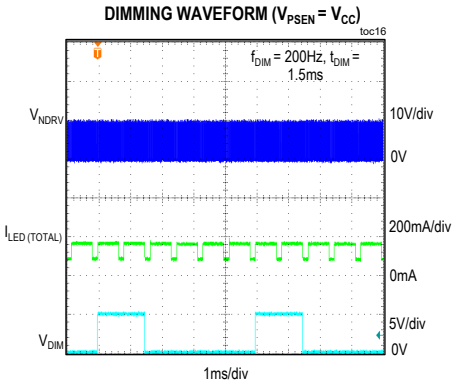
LED CURRENT vs. R_{ISET}



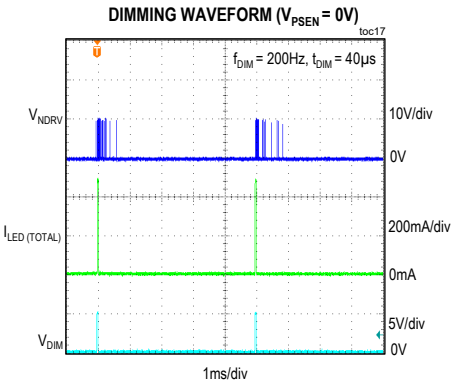
DIMMING WAVEFORM (V_{PSEN} = 0V)



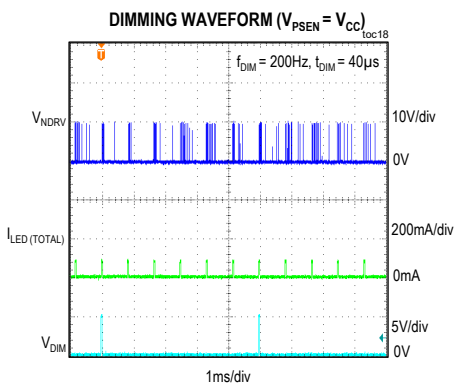
DIMMING WAVEFORM (V_{PSEN} = V_{CC})



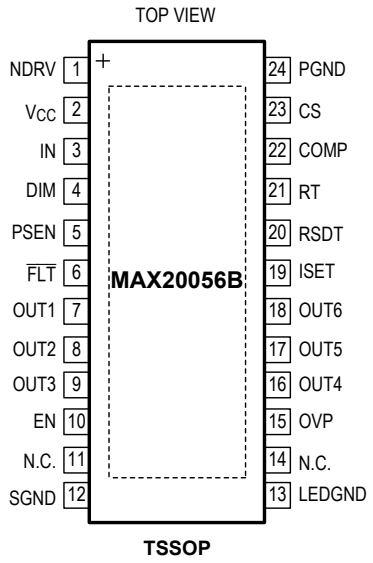
DIMMING WAVEFORM (V_{PSEN} = 0V)



DIMMING WAVEFORM (V_{PSEN} = V_{CC})



Pin Configuration



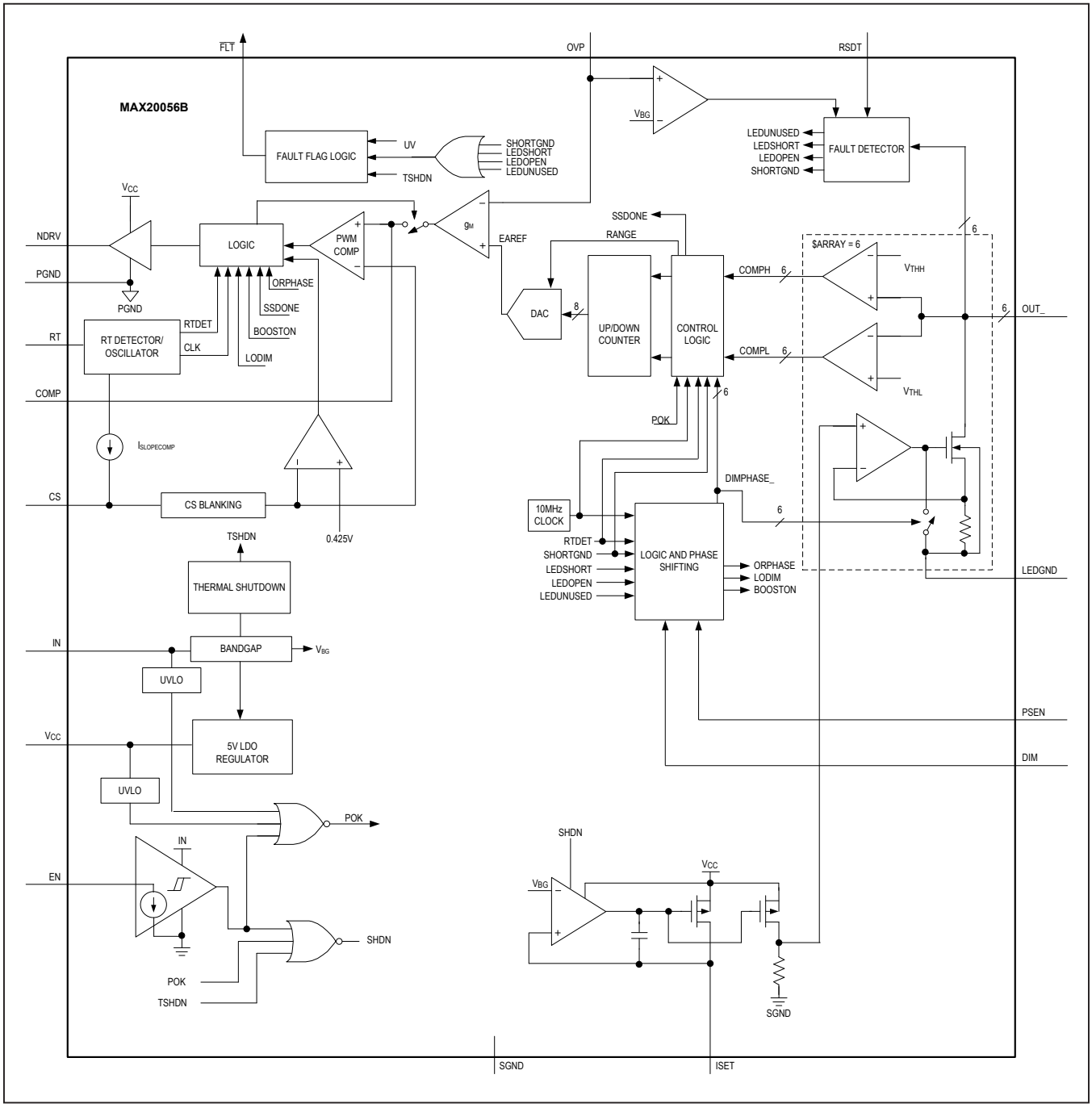
Pin Description

PIN	NAME	FUNCTION
1	NDRV	Switching nMOSFET Gate-Driver Output. Connect NDRV to the gate of the external switching power MOSFET. Typically, a small resistor (1Ω to 22Ω) is inserted between the NDRV output and nMOSFET gate to decrease the slew rate of the gate driver and reduce the switching noise.
2	V_{CC}	5V Regulator Output. Bypass V_{CC} to SGND with a minimum 2.2µF ceramic capacitor as close as possible to the device.
3	IN	Bias Supply Input. Connect a 4.5V to 42V supply to IN. Bypass IN to SGND with a ceramic capacitor.
4	DIM	Digital PWM Dimming Input. Apply a PWM signal to DIM for LED dimming control. Connect DIM to V_{CC} if dimming control is not used.
5	PSEN	Phase-Shift Enable Input. Connect to V_{CC} to enable phase shifting of the LED strings. Connect to SGND to disable phase shifting. The phase shifting is latched during power-on of the IC and cannot be changed unless power is cycled to the device, or EN is cycled.
6	$\overline{FLT}$	Open-Drain Fault Output. $\overline{FLT}$ asserts low when an open-LED, short-LED, or thermal shutdown is detected. Connect a pullup resistor from $\overline{FLT}$ to V_{CC}.
7	OUT1	LED-String Cathode Connection 1. OUT1 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT1. OUT1 sinks up to 120mA. If unused, connect OUT1 to LEDGND through a 12kΩ resistor.
8	OUT2	LED-String Cathode Connection 2. OUT2 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT2. OUT2 sinks up to 120mA. If unused, connect OUT2 to LEDGND through a 12kΩ resistor.

Pin Description (continued)

PIN	NAME	FUNCTION
9	OUT3	LED-String Cathode Connection 3. OUT3 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT3. OUT3 sinks up to 120mA. If unused, connect OUT3 to LEDGND through a 12kΩ resistor.
10	EN	Enable Input. Connect EN to logic-low to shut down the device. Connect EN to logic-high or IN for normal operation.
11, 14	N.C.	No Connection. Not internally connected.
12	SGND	Signal Ground. SGND is the current return-path connection for the low-noise analog signals. Connect SGND, LEDGND, and PGND at a single point.
13	LEDGND	LED Ground. LEDGND is the return-path connection for the linear current sinks. Connect SGND, LEDGND, and PGND at a single point.
15	OVP	Overvoltage Threshold-Adjust Input. Connect a resistor-divider from the switching converter output to OVP and SGND. The OVP comparator reference is internally set to 1.23V.
16	OUT4	LED-String Cathode Connection 4. OUT4 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT4. OUT4 sinks up to 120mA. If unused, connect OUT4 to LEDGND through a 12kΩ resistor.
17	OUT5	LED-String Cathode Connection 5. OUT5 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT5. OUT5 sinks up to 120mA. If unused, connect OUT2 to LEDGND through a 12kΩ resistor.
18	OUT6	LED-String Cathode Connection 6. OUT6 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT6. OUT6 sinks up to 120mA. If unused, connect OUT6 to LEDGND through a 12kΩ resistor.
19	ISET	LED Current-Adjust Input. Connect a resistor (R_{ISET}) from ISET to SGND to set the current through each LED string (I_{LED}) according to the formula $I_{LED} = 1500/R_{ISET}$.
20	RSDT	LED Short-Detection Threshold-Adjust Input. Connect a resistive divider from V_{CC} to RSDT and SGND to program the LED short-detection threshold. Connect RSDT directly to V_{CC} to disable LED short detection.
21	RT	Oscillator Timing Resistor Connection. Connect a timing resistor (R_{RT}) from RT to SGND to program the switching frequency according to Table 1.
22	COMP	Switching Converter Compensation Input. Connect the compensation network from COMP to SGND for current-mode control (see the *Feedback Compensation* section).
23	CS	Current-Sense Input. CS is the current-sense input for the switching regulator. A sense resistor connected from the source of the external power MOSFET to PGND sets the switching current limit. A resistor connected between the source of the power MOSFET and CS sets the slope compensation ramp rate (see the *Slope Compensation* section).
24	PGND	Power Ground. PGND is the switching current return-path connection. Connect SGND, LEDGND, and PGND at a single point.
—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the main IC ground connection. EP must be connected to SGND.

Block Diagram



Detailed Description

The MAX20056B high-efficiency HB LED driver integrates all the necessary features to implement a high-performance backlight driver to power LEDs in medium-to-large-sized displays for automotive as well as general applications. The device provides load-dump voltage protection up to 52V in automotive applications. The device incorporates two major blocks: a DC-DC controller with peak current-mode control to implement a boost or a SEPIC-type switched-mode power supply and a 6-channel LED driver with 20mA to 120mA constant-current-sink capability per channel.

The device features a constant-frequency, peak current-mode control with programmable slope compensation to control the duty cycle of the PWM controller. The DC-DC converter implemented using the controller generates the required supply voltage for the LED strings from a wide input-supply range. Connect LED strings from the DC-DC converter output to the 6-channel constant-current-sink drivers that control the current through the LED strings. A single resistor connected from the ISET input to ground adjusts the forward current through all six LED strings.

The device features adaptive voltage control that adjusts the converter output voltage depending on the forward voltage of the LED strings. This feature minimizes the voltage drop across the constant-current-sink drivers and reduces power dissipation in the device. The device includes an internal 5V LDO capable of powering additional external circuitry (up to 30mA). A logic input (EN) shuts down the device when pulled low. When the EN pin is pulled below 0.8V, the quiescent input current to the device is less than 8µA (typ).

The device provides a very wide (10,000:1) PWM dimming range where a dimming pulse as narrow as 500ns is possible at a 200Hz dimming frequency. When using the internal oscillator for the boost, the oscillator is synchronized to the PWM signal or to the phase-shift dimming logic derived from the PWM signal (phase-shifted dimming). This provides better dimming performance by guaranteeing that the gate drive for the boost goes high at the same instant that the PWM pulse goes high.

The device features phase shifting of the LED strings and frequency dithering of the switching converter.

Other advanced features include detection and string disconnect for open-LED strings, partially or fully shorted strings, and unused strings. Overvoltage protection clamps the converter output voltage to the programmed OVP threshold in the event of an open-LED condition.

Shorted-LED-string detection and overvoltage-protection thresholds are programmable using the RSDT and OVP inputs, respectively. An open-drain $\overline{FLT}$ signal asserts to indicate open-LED, shorted-LED, and overtemperature conditions. Disable individual current-sink channels by connecting the corresponding OUT_ to LEDGND through a 12kΩ resistor. In this case, $\overline{FLT}$ does not assert indicating an open-LED condition for the disabled channel. The device also features an overtemperature protection that shuts down the controller if the die temperature exceeds +165°C.

Current-Mode DC-DC Controller

The MAX20056B is a constant-frequency, current-mode controller designed to drive the LEDs in a boost, SEPIC, or a coupled-inductor buck-boost configuration. The device features multiloop control to regulate the peak current in the inductor, as well as the voltage across the LED current sinks to minimize power dissipation.

The switching frequency can be programmed over the 400kHz to 2.2MHz range using a resistor connected from RT to GND (see Table 1). Programmable slope compensation is available to compensate for subharmonic oscillations that occur at above 50% duty cycles in continuous-conduction mode.

The external nMOSFET is turned on at the beginning of every switching cycle. The inductor current ramps up linearly until turned off at the peak current level set by the feedback loop. The peak inductor current is sensed from the voltage across the current-sense resistor (R_{CS}) connected from the source of the external nMOSFET to PGND.

The device features leading-edge blanking to suppress the external nMOSFET switching noise. A PWM comparator compares the current-sense voltage plus the slope-compensation signal with the output of the transconductance error amplifier. The controller turns off the external nMOSFET when the voltage at CS exceeds the error amplifier's output voltage. This process repeats every switching cycle to achieve peak current-mode control.

In addition to the peak current-mode-control loop, the device has two other feedback loops for control. The converter output voltage is sensed through the OVP input, which goes to the inverting input of the error amplifier.

The OVP gain (A_{OVP}) is defined as V_{OUT}/V_{OVP}, or (R1 + R2)/R2.

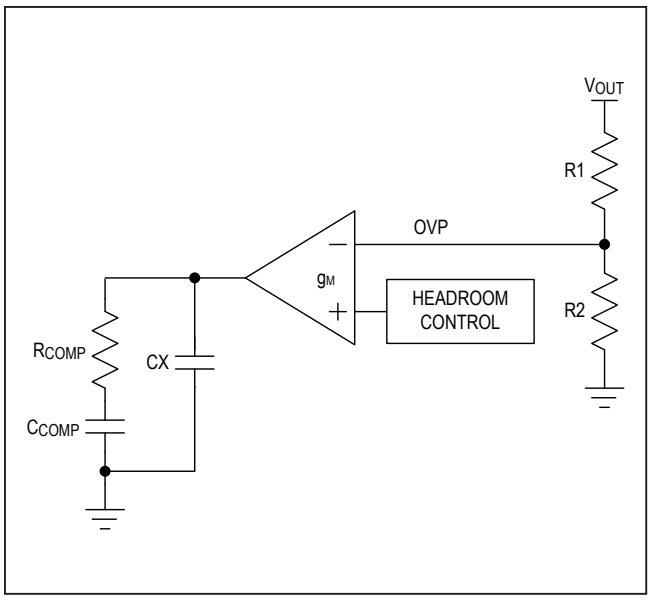


Figure 1. V_{OUT} Feedback Loop

The other feedback comes from the OUT_ current sinks. This loop controls the headroom of the current sinks to minimize total power dissipation, while still ensuring accurate LED current matching. Each current sink has a window comparator with a low threshold of 0.82V and a high threshold of 1.12V. These comparators drive some logic, which controls an up/down counter. The up/down counter is updated on every falling edge of the DIM input and drives an 8-bit digital-to-analog converter (DAC) that sets the reference to the error amplifier.

8-Bit DAC

The error amplifier's reference input is controlled with an 8-bit DAC. The DAC output is ramped up slowly during startup to implement a soft-start function (see the *Startup Sequence* section). During normal operation, the DAC output range is limited from 0.6V to 1.25V. The DAC LSB determines the minimum output-voltage step according to the following equation:

$$V_{STEP\_MIN} = V_{DAC\_LSB} \times A_{OVP}$$

where V_{STEP_MIN} is the minimum output-voltage step, V_{DAC_LSB} is 2.5mV, and A_{OVP} is the OVP resistor-divider gain.

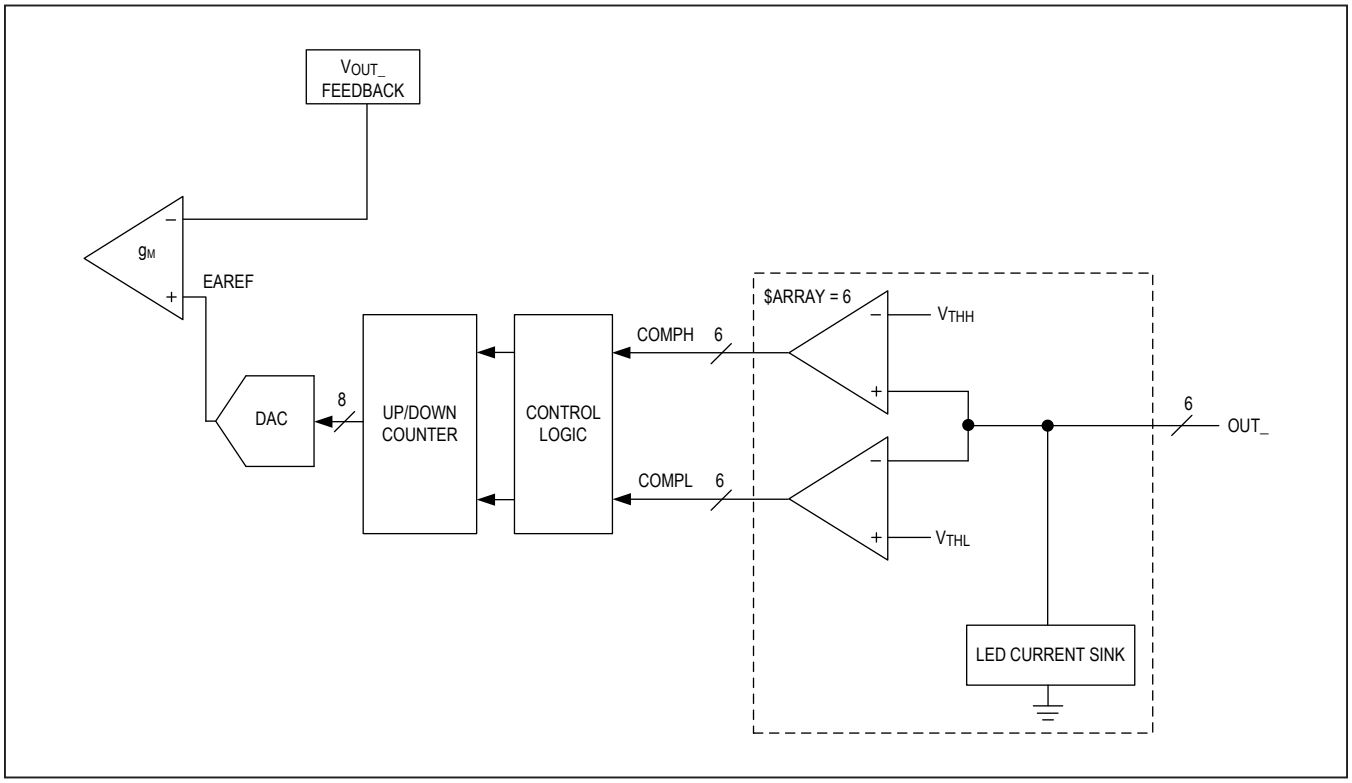


Figure 2. Headroom Control Loop

PWM Dimming

The DIM input accepts a pulse-width modulation (PWM) signal to control the luminous intensity of the LEDs and modulate the pulse width of the LED current. This allows for changing the brightness of the LEDs without the color temperature shift that sometimes occurs with analog dimming. The DIM input detects the dimming frequency based on the first two pulses applied to the DIM input after EN goes high. The dimming frequency cannot be changed during normal operation. The DIM input is sampled with an internal 10MHz clock and the sampled pulse width takes effect at the OUT_ pins on the following dimming period.

If a change of dimming frequency is desired, set the EN input low, change the DIM frequency, and then the EN signal can be set high again. The DIM signal can be applied before or after the device is enabled, but needs to power on smoothly (no high-frequency pulses). If the DIM signal turn-on is inconsistent, the DIM signal should be applied first; once the DIM signal is stable, the EN signal can be applied. In normal dim mode, if at least one of the LED current sinks is turned on, the boost converter switches. If none of the current sinks are on (each current sink dim signal is low), the boost converter stops switching, and the COMP node is disconnected from the error amplifier until one of the LED current sinks is turned on.

Low-Dim Mode

The MAX20056B operation changes at very narrow dimming pulses to ensure a consistent dimming response of the LEDs. The device checks the pulse width of the signal being applied to the DIM input. If the dimming on-time is lower than 50µs (typ) for f_{SW} between 400kHz and 1MHz or 25µs (typ) for f_{SW} between 1.3MHz and 2.2MHz, the device enters low-dim mode. In this state, the converter switches continuously and the LED short detection is disabled. When the DIM input is greater than 51µs (typ) for f_{SW} between 400kHz and 1MHz or 26µs (typ) for f_{SW} between 1.3MHz and 2.2MHz, the device goes back into normal dim mode, enabling the short-LED detection and switching the power FET only when the DIM signal is high.

Phase Shifting

The MAX20056B offers phase shifting of the LED strings. The DIM signal is sampled by a 10MHz clock. When phase shifting is enabled, the sampled DIM input is used to generate separate dimming signals for each LED string that are shifted in phase. The resolution with which the DIM signal is captured degrades at higher DIM input frequencies; therefore, dimming frequencies between 100Hz and 3kHz are recommended, although higher dimming frequencies are technically possible. The phase shift between strings is determined by the following equation:

$$\theta = 360/n$$

where n is the total number of strings being used and θ is the phase shift in degrees. The order of the sequence is fixed, with OUT1 as the first in the sequence and OUT6 as the last. See Figure 3 for a timing diagram example with phase shifting enabled.

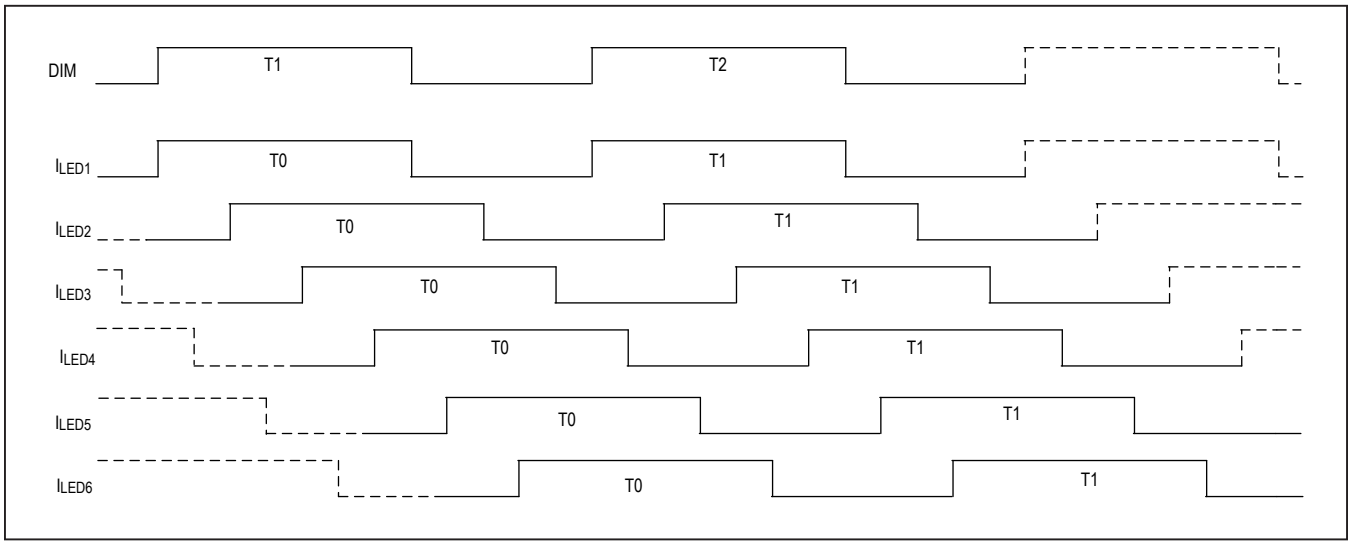


Figure 3. Timing Diagram with Phase Shifting Enabled

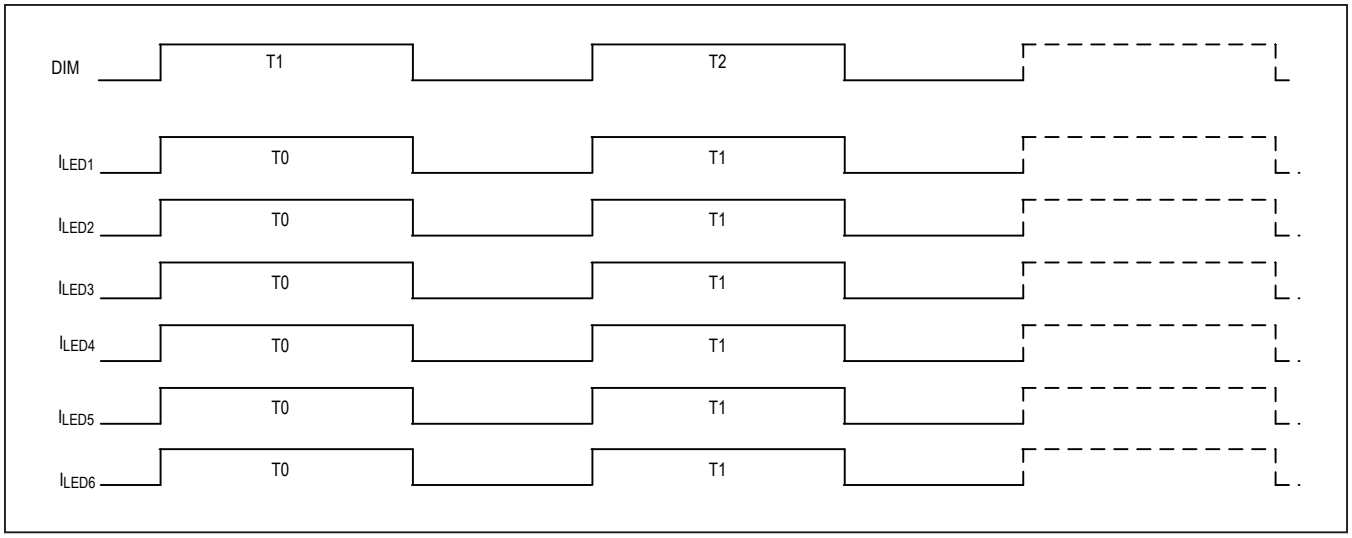


Figure 4. Timing Diagram with Phase Shifting Disabled

The phase-shifting feature is enabled or disabled with the PSEN input. The PSEN input status is latched at power-up. Connect PSEN to V_{CC} to enable phase shifting of the LED strings. When phase shifting is disabled, all strings turn on/turn off at the same time and are controlled with the DIM input (Figure 4). If multiple current sinks are being connected in parallel to achieve greater than 120mA per string, phase shifting should be disabled.

If a fault is detected, resulting in a string being disabled during normal operation, the phase shifting does not adjust. For example, if there are six strings, each string is 60° out-of-phase. If the 4th string is disabled due to a fault, there will still be 60° phase difference between each string, except for the 3rd and 5th strings, which will be 120° out-of-phase.

The PWM dimming frequency should not change during normal operation. To change the PWM dimming frequency, the device must be disabled and reenabled. When disabling unused strings, disable the higher-numbered OUT_ current sinks first.

Undervoltage Lockout (UVLO)

The device features two UVLOs that monitor the input voltage at IN and the output of the internal LDO regulator at V_{CC}. The device turns on after both IN and V_{CC} exceed their respective UVLO thresholds. Both UVLO thresholds are at 4.15V rising and 3.95V falling.

Enable (EN)

The device is enabled using the EN logic input pin. The EN input is sequence-free, meaning it can tolerate voltages up to +52V, regardless of the voltage on IN. To shut down the device, drive the EN pin with a logic-low, which reduces the current consumption to 8µA (typ) at V_{IN} = 12V. Connect the EN pin to IN if not used.

Startup Sequence

The startup behavior of the MAX20056B is based on the IN, EN, and DIM inputs, all of which are sequence-free inputs. The startup sequence of the device begins when the EN input rises above its threshold. The startup sequence occurs in two stages, as described in the *Stage 1* and *Stage 2* sections.

Stage 1

Assuming the IN input is above its UVLO, the V_{CC} regulator will begin to charge up. Once the V_{CC} regulator output rises above the V_{CC} UVLO threshold, the device goes through its power-up checks, including unused string detection and OUT_ short-to-ground detection. Any current sinks detected as unused are disabled to prevent a false fault-flag assertion during normal operation. After these checks have been performed the converter begins to operate and the output voltage begins to ramp up. The DAC reference to the error amplifier is stepped up 1 bit at a time until the output reaches 50% of the OVP set point (or 1.1V in the case of MAX20056BAUGB). This stage duration is fixed at approximately 50ms (or 25ms in the case of MAX20056BAUGB). See Figure 5, Figure 7, and Figure 8.

Stage 2

The second stage begins once the first stage is complete and the DIM input goes high. During the second stage, the output of the converter is ramped up or down until the minimum OUT_ voltage falls within the window comparator limits of 0.82V (typ) and 1.12V (typ). The output ramp is again controlled by the DAC, which provides the reference for the error amplifier. The DAC output is updated on each rising edge of the DIM input. If the DIM input is a 100% duty cycle (DIM = high), then the DAC output is updated once every 10ms. See Figure 6, Figure 7, and Figure 8.

Figure 7 and Figure 8 show typical startup waveforms for MAX20056BAUGA with Stage 1 and Stage 2 of the soft-start, one after the other. They also show the dependency of the total soft-start time on the dimming frequency. The total soft-start time can be calculated using the following equations:

For MAX20056BAUGA

$$t_{SS} = 50ms + \frac{V_{LED} + 0.97V - (0.6V \times A_{OVP})}{f_{DIM} \times 0.01V \times A_{OVP}}$$

For MAX20056BAUGB

$$t_{SS} = 25ms + \frac{1.1V \times A_{OVP} - (V_{LED} + 0.97V)}{f_{DIM} \times 0.01V \times A_{OVP}}$$

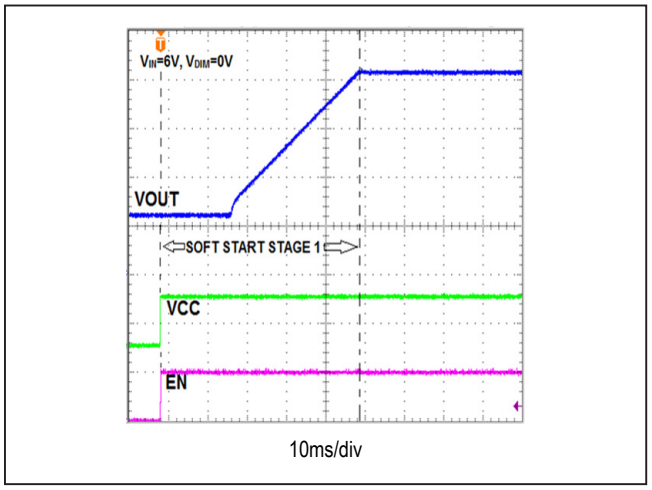


Figure 5. Stage 1 of Soft-Start

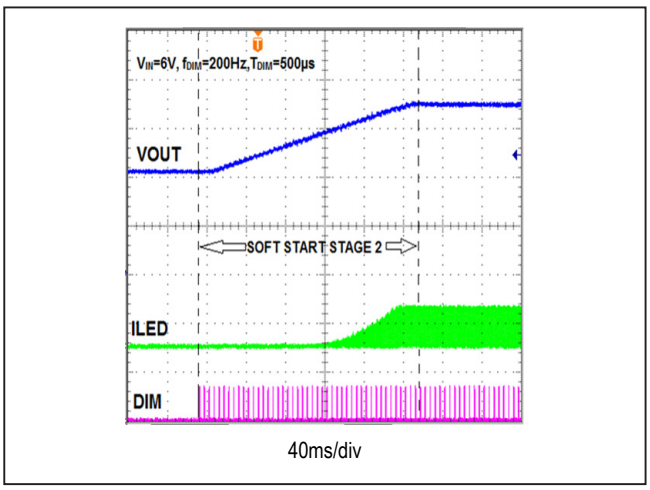


Figure 6. Stage 2 of Soft-Start

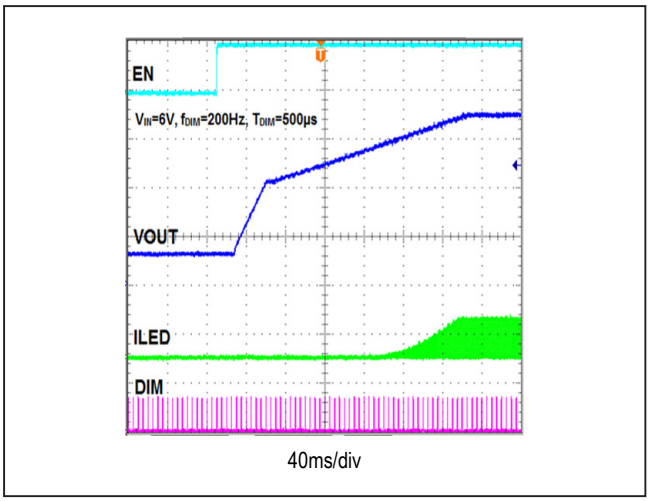


Figure 7. Stage 1 and Stage 2 of Soft-Start with 200Hz Dimming (Total Soft-Start Time is Approximately 250ms)

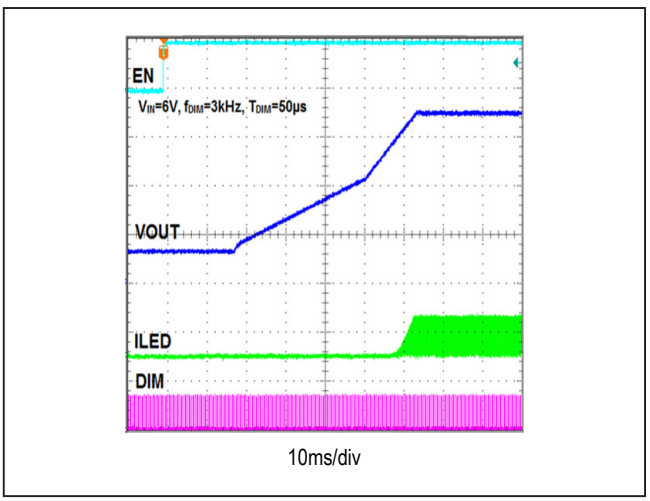


Figure 8. Stage 1 and Stage 2 of Soft-Start with 3kHz Dimming (Total Soft-Start Time is Approximately 60ms)

where t_{SS} is the total soft-start time, 50ms is the fixed Stage 1 duration, V_{LED} is the total forward voltage of the LED strings, 0.97V is midpoint of the window comparator, A_{OVP} is the gain of the OVP resistor-divider, f_{DIM} is the dimming frequency (use 100Hz if the DIM input duty cycle is 100%), and 0.01V is the maximum voltage step per clock cycle of the DAC. A fast soft-start option is also available.

Oscillator Frequency

The internal oscillator frequency is programmable between 400kHz and 2.2MHz using a resistor (R_{RT}) connected from the RT input to SGND. A current is sourced through RT and the voltage is compared to different thresholds. Table 1 shows the switching-frequency options and corresponding recommended resistor values.

Spread-Spectrum Mode

The MAX20056B includes a unique spread-spectrum mode (SSM) that reduces emission (EMI) at the switching frequency and its harmonics.

The spread spectrum uses a pseudorandom dithering technique where the switching frequency is varied in the range of 94% of the programmed switching frequency to 106% of the programmed switching frequency when enabled.

Instead of a large amount of spectral energy present at multiples of the switching frequency, the total energy at the fundamental and each harmonic is spread over a wider bandwidth, reducing the energy peak.

5V LDO Regulator (V_{CC})

The internal LDO regulator converts the input voltage at IN to a 5V output voltage at V_{CC}. The V_{CC} regulator supplies current to the internal control circuitry and the gate driver. The V_{CC} regulator is also capable of supplying up to 30mA of current to external circuits.

Table 1. Switching Frequency vs. R_{RT}

f_{SW} (kHz)	R_{RT} RECOMMENDED (kΩ, 1%)
400	20
700	52.3
1000	76.8
1300	113kΩ
1600	158kΩ
1900	210kΩ
2200	301kΩ

Bypass V_{CC} to SGND with a minimum of 1µF ceramic capacitor placed as close as possible to the device. If the input supply to the LED driver is a regulated 5V supply, it is possible to externally connect IN to V_{CC} to maximize the gate-drive voltage. When connecting IN and V_{CC} together externally, ensure that enough bypass capacitance is used to keep the input stable over all operating conditions.

PWM MOSFET Driver

The NDRV output is a push-pull output with a pMOSFET on-resistance of 1.5Ω (typ) and an nMOSFET on-resistance of 0.8Ω (typ). NDRV swings from PGND to V_{CC} to drive an external nMOSFET. The driver typically sources 2.0A and sinks 2.0A allowing for fast turn-on/turn-off of high gate-charge MOSFETs. The power dissipation in the device is mainly a function of the average current sourced to drive the external MOSFET (I_{VCC}) if there are no additional loads on V_{CC}. I_{VCC} depends on the total gate charge (Q_G) and operating frequency of the converter.

LED Current Control

The MAX20056B features six identical constant-current sources used to drive multiple HB LED strings. The current through each one of the six channels is adjustable between 20mA and 120mA using an external resistor (R_{ISET}) connected between ISET and SGND. Select R_{ISET} using the following formula:

$$R_{ISET} = \frac{1500}{I_{OUT\_}}$$

where $I_{OUT\_}$ is the desired output current for each of the six channels. If more than 120mA is required in an LED string, use two or more of the current-source outputs (OUT_) connected together to drive the string. Phase shifting cannot be used in applications where multiple current sinks are connected in parallel; therefore, PSEN should be connected to ground for standard dimming control.

Disabling LED Strings

To disable an unused LED string, connect the unused OUT_ to ground through a 12kΩ resistor. During startup, the device sources 60µA (typ) current through the OUT_ pins and measures the corresponding voltage. For the string to be properly disabled, the OUT_ voltage should measure between 350mV and 1.15V during this check. 350mV is the maximum threshold for the OUT_ short-to-

ground check and 1.15V is the minimum unused string-detection threshold.

Note: When disabling unused strings, it is necessary to start by disabling the highest-numbered current sinks first. For example, if only four strings are required, OUT1–OUT4 must be used and OUT5 and OUT6 must be disabled.

Fault Protections

Fault protections in the device include cycle-by-cycle current limiting using the PWM controller, DC-DC converter output overvoltage protection, open-LED detection, short-LED detection and protection, and overtemperature shutdown. An open-drain fault-flag output ($\overline{FLT}$) goes low when an open-LED string is detected, a shorted-LED string is detected, or during thermal shutdown. A fault flag resulting from thermal shutdown or shorted LEDs is cleared as soon as the fault condition is removed. $\overline{FLT}$ is latched low for an open LED and can be reset by cycling power or toggling the EN pin. The thermal-shutdown threshold is +165°C with +15°C hysteresis.

Open-LED Management and Overvoltage Protection

On power-up, the device detects and disconnects any unused current-sink channels before entering the DC-DC converter soft-start. Disable the unused current-sink channels by connecting the corresponding OUT_ to LEDGND through a 12kΩ resistor. This avoids asserting the $\overline{FLT}$ output for the unused channels. After soft-start, the device detects open LED and disconnects any strings with an open LED from the internal minimum OUT_ voltage detector. This keeps the DC-DC converter output voltage within safe limits and maintains high efficiency. During normal operation, the DC-DC converter output regulates the minimum OUT_ voltage to fall within the 0.82V and 1.12V window comparator limits. If any LED string is open, the voltage at the opened OUT_ goes to V_{LEDGND}. The DC-DC converter output voltage then increases to the overvoltage-protection threshold set by the voltage-divider network connected between the converter output, OVP input, and SGND. Select V_{OUT_OVP} according to the following equation:

$$1.1 \times (V_{LED\_MAX} + 1.25V) < V_{OUT\_OVP} < 2 \times (V_{LED\_MIN} + 0.7V)$$

where V_{LED_MAX} is the maximum expected LED string voltage and V_{LED_MIN} is the minimum expected LED string voltage. V_{OUT_OVP} should also be chosen such that the voltage at OUT_ does not exceed the absolute maximum rating.

The overvoltage-protection threshold at the DC-DC converter output (V_{OUT_OVP}) is determined using the following formula:

$$V_{OUT\_OVP} = 1.23V \times \left(1 + \frac{R1}{R2}\right)$$ (see Figure 12)

where 1.23V (typ) is the OVP threshold.

As soon as the DC-DC converter output reaches the overvoltage-protection threshold, the PWM controller is switched off, setting NDRV low. Any current-sink output with $V_{OUT\_}$ < 300mV (typ) is disconnected from the minimum-voltage detector.

The OVP voltage threshold should be set less than twice the minimum LED voltage to ensure proper operation. The OVP minimum regulation point is 600mV (typ).

Connect a 12kΩ resistor between OUT_ and LEDGND for each unused channel to avoid OVP triggering at startup. When an open-LED overvoltage condition occurs, $\overline{FLT}$ is latched low.

For boost-circuit applications, the OVP resistor-divider is always dissipating power from the battery, through the inductor and switching diode (See Figure 9). If ultra-low shutdown current is needed, a general-purpose MOSFET can be added between the bottom OVP resistor and ground, with the EN of the device controlling the gate of the MOSFET (See Figure 10). This additional MOSFET disconnects the OVP resistor-divider path when the device is disabled.

Short-LED Detection

The device checks for shorted LEDs at each rising edge of DIM. An LED short is detected at OUT_ if the following condition is met:

$$V_{OUT\_} > 4 \times V_{RSDT}$$

where $V_{OUT\_}$ is the voltage at OUT_, and V_{RSDT} is the programmable LED short-detection threshold set at the RSDT input. Adjust V_{RSDT} using a voltage-divider resistive network connected at the V_{CC} output, RSDT input, and SGND. Once a short is detected on any of the strings, the LED strings with the short are disconnected and the $\overline{FLT}$ output flag asserts until the device detects that the shorts are removed on any of the following rising edges of DIM. Connect RSDT directly to V_{CC} to always disable LED short detection. Short-LED detection is disabled in low-dimming mode. If the DIM input is connected high, short-LED detection is performed continuously.

Short-LED detection is also disabled in the case where all active OUT_ channels rise above 2.8V. This can occur in a boost-converter application when the input voltage

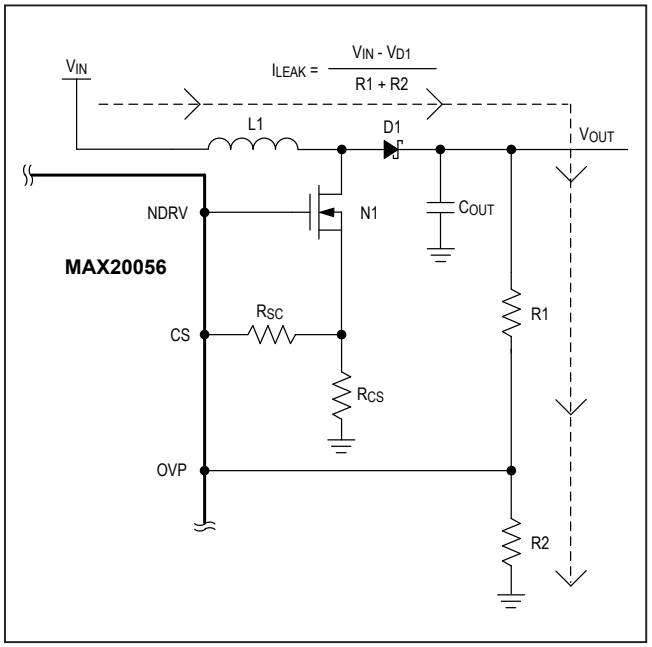


Figure 9. Battery Leakage through the OVP Resistor-Divider

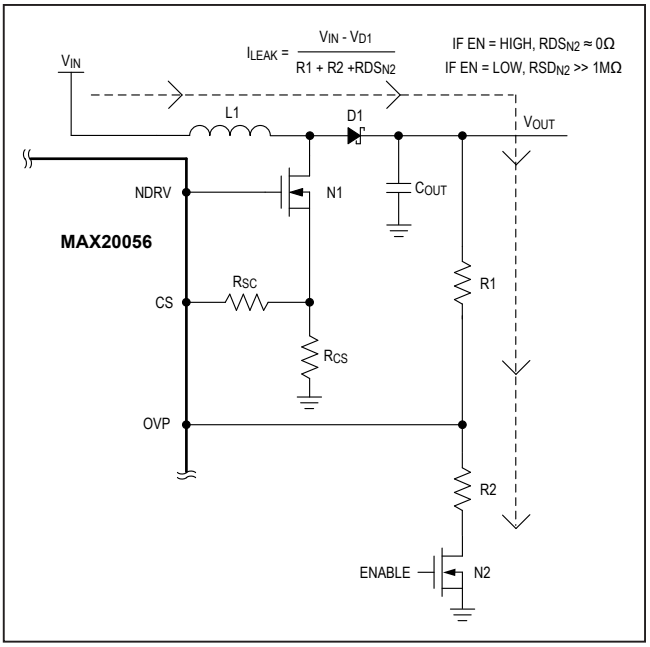


Figure 10. N2 Disconnects the OVP Resistor-Divider During Shutdown to Greatly Reduce the Leakage Current

becomes higher than the total LED string voltage drop, such as during a battery load dump. If a short-LED fault occurs during a load dump, the fault flag will not assert until the load dump is over and the minimum OUT_ voltage has fallen below 2.8V. If a load dump occurs after a short LED is detected, the fault flag deasserts until the load dump is over and the minimum OUT_ voltage has fallen below 2.8V, at which point, the fault flag reasserts.

Applications Information

DC-DC Converter

Three different converter topologies are possible with the DC-DC controller in the MAX20056B, which has the ground-referenced outputs necessary to use the constant-current-sink drivers. If the LED string forward voltage is always more than the input-supply voltage range, use the boost-converter topology. If the LED string forward voltage falls within the supply voltage range, use the SEPIC or coupled-inductor buck-boost converter topology. The latter is basically a flyback converter with 1:1 turns ratio. 1:1 coupled inductors are available with tight coupling suitable for this application.

The boost-converter topology provides the highest efficiency among the above-mentioned topologies. The coupled-inductor topology has the advantage of not using a coupling capacitor over the SEPIC configuration. Also, the feedback-loop compensation for SEPIC becomes complex if the coupling capacitor is not large enough. A coupled inductor is not suitable for cases where the coupled-inductor windings are not tightly coupled. Considerable leakage inductance requires additional snubber components and degrades the efficiency.

Power-Circuit Design

First select a converter topology based on the above factors. Determine the required input supply voltage range, the maximum voltage needed to drive the LED strings including the minimum voltage across the constant LED current sink (V_{LED}), and the total output current needed to drive the LED strings (I_{LED}) as follows:

$$I_{LED} = I_{STRING} \times N_{STRING}$$

where I_{STRING} is the LED current per string in amperes and N_{STRING} is the number of strings used.

Calculate the maximum duty cycle (D_{MAX}) using the following equations:

For boost configuration:

$$D_{MAX} = \frac{(V_{LED} + V_{D1} - V_{IN\_MIN})}{(V_{LED} + V_{D1} - V_{DS} - 0.3V)}$$

For SEPIC and coupled-inductor buck-boost-configurations:

$$D_{MAX} = \frac{(V_{LED} + V_{D1})}{(V_{IN\_MIN} - V_{DS} - 0.3V + V_{LED} + V_{D1})}$$

where V_{D1} is the forward drop of the rectifier diode in volts (approximately 0.6V), V_{IN_MIN} is the minimum input supply voltage in volts, and V_{DS} is the drain-to-source voltage of the external MOSFET in volts when it is on, and 0.3V is the peak current-sense voltage. Initially, use an approximate value of 0.2V for V_{DS} to calculate D_{MAX}. Calculate a more accurate value of D_{MAX} after the power MOSFET is selected based on the maximum inductor current. Select the switching frequency (f_{SW}) depending on the space, noise, and efficiency constraints.

Boost and Coupled-Inductor Configurations

In all three converter configurations, the average inductor current varies with the line voltage and the maximum average current occurs at the lowest line voltage. For the boost converter, the average inductor current is equal to the input current. Select the maximum peak-to-peak ripple on the inductor current (ΔIL). The recommended peak-to-peak ripple is 60% of the average inductor current, but other values are acceptable too.

Use the following equations to calculate the maximum average inductor current (IL_{AVG}) and peak inductor current (IL_P) in amperes:

$$IL_{AVG} = \frac{I_{LED}}{1 - D_{MAX}}$$

Allowing the peak-to-peak inductor ripple ΔIL to be +30% of the average inductor current:

$$\Delta IL = IL_{AVG} \times 0.3 \times 2$$

and:

$$IL_P = IL_{AVG} + \frac{\Delta IL}{2}$$

Calculate the minimum inductance value (L_{MIN}) in henries with the inductor current ripple set to the maximum value:

$$L_{MIN} = \frac{\left(V_{IN\_MIN} - V_{DS} - 0.3V\right) \times D_{MAX}}{f_{SW} \times \Delta IL}$$

where 0.3V is the peak current-sense voltage. Choose an inductor that has a minimum inductance greater than the calculated L_{MIN} and current rating greater than IL_P. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current for boost configuration. For the coupled inductor, the saturation limit of the inductor with only one winding conducting should be 10% higher than IL_P.

SEPIC Configuration

Power-circuit design for the SEPIC configuration is very similar to a conventional design, with the output voltage referenced to the input supply voltage. For SEPIC, the output is referenced to ground and the inductor is split into two parts (see Figure 13 for the SEPIC configuration). One of the inductors (L2) takes LED current as the average current and the other (L1) takes input current as the average current.

Use the following equations to calculate the average inductor currents ($IL1_{AVG}$, $IL2_{AVG}$) and peak inductor currents ($IL1_P$, $IL2_P$) in amperes:

$$IL1_{AVG} = \frac{I_{LED} \times D_{MAX} \times 1.1}{1 - D_{MAX}}$$

The factor 1.1 provides a 10% margin to account for the converter losses:

$$IL2_{AVG} = I_{LED}$$

Assuming the peak-to-peak inductor ripple ΔIL is ±30% of the average inductor current:

$$\Delta IL1 = IL1_{AVG} \times 0.3 \times 2$$

and:

$$IL1_P = IL1_{AVG} + \frac{\Delta IL1}{2}$$

$$\Delta IL2 = IL2_{AVG} \times 0.3 \times 2$$

and:

$$IL2_P = IL2_{AVG} + \frac{\Delta IL2}{2}$$

Calculate the minimum inductance values ($L1_{MIN}$ and $L2_{MIN}$) in henries with the inductor current ripples set to the maximum value as follows:

$$L1_{MIN} = \frac{\left(V_{IN\_MIN} - V_{DS} - 0.3V\right) \times D_{MAX}}{f_{SW} \times \Delta IL1}$$

$$L2_{MIN} = \frac{\left(V_{IN\_MIN} - V_{DS} - 0.3V\right) \times D_{MAX}}{f_{SW} \times \Delta IL2}$$

where 0.3V is the peak current-sense voltage. Choose inductors that have a minimum inductance greater than the calculated $L1_{MIN}$ and $L2_{MIN}$ and current rating greater than $IL1_P$ and $IL2_P$, respectively. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current.

For simplifying further calculations, consider L1 and L2 as a single inductor with L1 and L2 connected in parallel. The combined inductance value and current is calculated as follows:

$$L_{MIN} = \frac{L1_{MIN} \times L2_{MIN}}{L1_{MIN} + L2_{MIN}}$$

and:

$$IL_{AVG} = IL1_{AVG} + IL2_{AVG}$$

where IL_{AVG} represents the total average current through both the inductors together for SEPIC configuration. Use these values in the calculations for SEPIC configuration in the following sections.

Select coupling-capacitor C_S so that the peak-to-peak ripple on it is less than 2% of the minimum input supply voltage. This ensures that the second-order effects created by the series-resonant circuit comprising L1, C_S, and L2 do not affect the normal operation of the converter. Use the following equation to calculate the minimum value of C_S:

$$C_S \geq \frac{I_{LED} \times D_{MAX}}{V_{IN\_MIN} \times 0.02 \times f_{SW}}$$

where C_S is the minimum value of the coupling capacitor in farads, I_{LED} is the LED current in amperes, the factor 0.02 accounts for 2% ripple, and f_{SW} is in hertz.

Slope Compensation

The MAX20056B generates a current ramp for slope compensation. This ramp current is in sync with the switching frequency and starts from zero at the beginning of every clock cycle and rises linearly to reach 50µA at the end of the clock cycle. The slope-compensating resistor (R_{SC}) is connected between the CS input and the source of the external MOSFET. This adds a programmable ramp voltage to the CS input voltage to provide slope compensation.

Use the following equation to calculate the value of slope-compensation resistance (R_{SC}):

For boost configuration:

$$R_{SC} = \frac{\left(V_{LED} - 2V_{IN\_MIN}\right) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

For SEPIC and coupled-inductor configurations:

$$R_{SC} = \frac{\left(V_{LED} - V_{IN\_MIN}\right) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

where V_{LED} and V_{IN_MIN} are in volts, R_{SC} and R_{CS} are in ohms, L_{MIN} is in henries and f_{SW} is in hertz. The value of the switch current-sense resistor (R_{CS}) can be calculated as follows:

For boost configuration:

$$0.4 \times 0.9 = I_{LP} \times R_{CS} + \frac{(D_{MAX} \times \left(V_{LED} - 2V_{IN\_MIN}\right) \times R_{CS} \times 3)}{4 \times L_{MIN} \times f_{SW}}$$

For SEPIC and coupled-inductor configurations:

$$0.4 \times 0.9 = I_{LP} \times R_{CS} + \frac{(D_{MAX} \times \left(V_{LED} - V_{IN\_MIN}\right) \times R_{CS} \times 3)}{4 \times L_{MIN} \times f_{SW}}$$

where 0.4 is the minimum value of the peak current-sense threshold. The current-sense threshold also includes the slope-compensation component. The minimum current-sense threshold of 0.4 is multiplied by 0.9 to take tolerances into account.

Output Capacitor Selection

For all three converter topologies, the output capacitor supplies the load current when the main switch is on. The function of the output capacitor is to reduce the converter output ripple to acceptable levels. The entire output-voltage ripple appears across constant-current-sink outputs because the LED string voltages are stable due to the constant current. For the MAX20056B, limit the peak-to-peak output-voltage ripple to 200mV to get stable output current.

The ESR, ESL, and the bulk capacitance of the output capacitor contribute to the output ripple. In most of the applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects. To reduce the ESR and ESL effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise during PWM dimming, the amount of ceramic capacitance on the output is usually minimized. In this case, an additional electrolytic or aluminum organic polymer capacitor provides most of the bulk capacitance.

External Switching-MOSFET Selection

The external switching MOSFET should have a voltage rating sufficient to withstand the maximum output voltage, together with the rectifier diode drop and any possible overshoot due to ringing caused by parasitic inductances

and capacitances. The recommended MOSFET V_{DS} voltage rating is 30% higher than the sum of the maximum output voltage and the rectifier diode drop.

The recommended continuous drain-current rating of the MOSFET (ID), when the case temperature is at +70°C, is greater than that calculated below:

$$ID_{RMS} = 1.3 \times \sqrt{IL_{AVG}^2 \times D_{MAX}}$$

The MOSFET dissipates power due to both switching losses and conduction losses.

Use the following equation to estimate the conduction losses in the MOSFET:

$$P_{COND} = IL_{AVG}^2 \times D_{MAX} \times R_{DS(ON)}$$

where $R_{DS(ON)}$ is the on-state drain-to-source resistance of the MOSFET. Use the following equation to estimate the switching losses in the MOSFET:

$$P_{SW} = \frac{IL_{AVG} \times V_{LED} \times V_{GS} \times C_{GD} \times f_{SW}}{2} \times \left(\frac{1}{I_{GON}} + \frac{1}{I_{GOFF}} \right)$$

where I_{GON} and I_{GOFF} are the gate currents of the MOSFET in amperes, with V_{GS} as the threshold voltage in volts, when it is turned on and turned off, respectively. C_{GD} is the gate-to-drain MOSFET capacitance in farads.

The MOSFET power-dissipation equations provide first-order estimates only. The actual MOSFET power dissipation may vary depending on the parasitic components introduced by the PCB layout, as well as any EMI mitigation components such as gate resistors or snubber circuits.

Rectifier-Diode Selection

Using a Schottky rectifier diode produces less forward drop and puts the least burden on the MOSFET during reverse recovery. A diode with considerable reverse-recovery time increases the MOSFET switching loss. Select a Schottky diode with a voltage rating 20% higher than the maximum boost-converter output voltage and current rating greater than that calculated in the following equation:

$$I_D = IL_{AVG} \times (1 - D_{MAX})$$

Feedback Compensation

During normal operation, the feedback control loop regulates the minimum OUT_ voltage to fall within the window comparator limits of 0.8V and 1.1V when LED string currents are enabled during PWM dimming. When LED currents are off during PWM dimming, the control loop turns off the converter and stores the steady-state condition in the form of capacitor voltages, mainly the output filter-capacitor voltage and the compensation-capacitor voltage.

The switching converter small-signal-transfer function has a right-half plane (RHP) zero for boost configuration if the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90° phase lag, which is difficult to compensate.

The worst-case RHP zero frequency (f_{ZRHP}) is calculated as follows:

For boost configuration:

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2\pi \times L \times I_{LED}}$$

For SEPIC and coupled-inductor buck-boost configurations:

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2\pi \times L \times I_{LED} \times D_{MAX}}$$

where f_{ZRHP} is in hertz, V_{LED} is in volts, L is the inductance value of L1 in henries, and I_{LED} is in amperes. A simple way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency, with a -20dB/decade slope.

The switching converter small-signal-transfer function also has an output pole. The effective output impedance, together with the output-filter capacitance, determines the output pole frequency (f_{P1}) that is calculated as follows:

For boost configuration:

$$f_{P1} = \frac{I_{LED}}{2\pi \times V_{LED} \times C_{OUT}}$$

For SEPIC and coupled-inductor buck-boost configurations:

$$f_{P1} = \frac{I_{LED} \times D_{MAX}}{2\pi \times V_{LED} \times C_{OUT\_}}$$

where f_{P1} is in hertz, V_{LED} is in volts, I_{LED} is in amperes, and $C_{OUT\_}$ is in farads. Compensation components (R_{COMP} and C_{COMP}) perform two functions: C_{COMP} introduces a low-frequency pole that presents a -20dB/decade slope to the loop gain and R_{COMP} flattens the gain of the error amplifier for frequencies above the zero formed by R_{COMP} and C_{COMP}. For compensation, this

zero is placed at the output pole frequency (f_{P1}) so that it provides a -20dB/decade slope for frequencies above f_{P1} to the combined modulator and compensator response.

The value of R_{COMP} needed to fix the total loop gain at f_{P1} so the total loop gain crosses 0dB with -20dB/decade slope at 1/5 the RHP zero frequency is calculated as follows:

For boost configuration:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times A_{OVP}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1 - D_{MAX})}$$

For SEPIC and coupled-inductor buck-boost configurations:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times D_{MAX} \times A_{OVP}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1 - D_{MAX})}$$

where R_{COMP} is the compensation resistor in ohms, f_{ZRHP} and f_{P1} are in hertz, A_{OVP} is the OVP resistor-divider gain, R_{CS} is the switch current-sense resistor in ohms, and GM_{COMP} is the transconductance of the error amplifier (680µS).

The value of C_{COMP} is calculated as follows:

$$C_{COMP} = \frac{1}{2\pi \times R_{COMP} \times f_{Z1}}$$

where f_{Z1} is the compensation zero placed at 1/5 of the crossover frequency that is, in turn, set at 1/5 of the f_{ZRHP}. If the output capacitors do not have low ESR, the ESR zero frequency may fall within the 0dB crossover frequency. An additional pole may be required to cancel out this pole placed at the same frequency. This is usually implemented by connecting a capacitor in parallel with C_{COMP} and R_{COMP}.

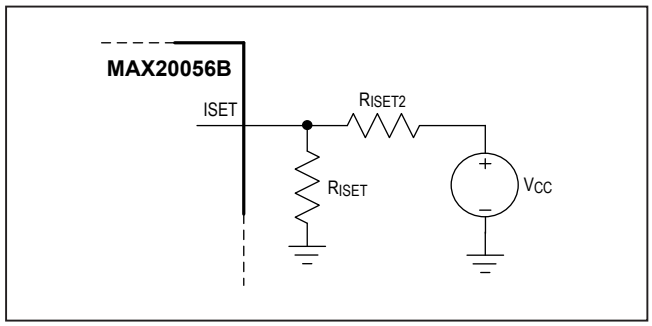


Figure 11. Analog Dimming with External Control Voltage

V_{OUT} to OUT_ Bleed Resistors

The OUT_ pins have a leakage specification of 3µA (max) in the case where all the OUT_ pins are shorted to 48V (see $I_{OUTLEAK}$ in the *Electrical Characteristics* table). This leakage current is dependent on the OUT_ voltage and is higher at higher voltages. Therefore, in cases where large numbers of LEDs are connected in series, a 100kΩ (or larger) bleed resistor can be placed in parallel with the LED string to prevent the OUT_ leakage current from very dimly turning on the LEDs even when the DIM signal is low. See resistors R_{B1}–R_{B6} in Figure 12.

Analog Dimming Using External Control Voltage

Connect a resistor R_{ISET2} to the ISET input (see Figure 11) for controlling the LED string current using an external control voltage. The device applies a fixed 1.23V bandgap reference voltage at ISET and measures the current through ISET. This measured current, multiplied by a factor of 1220, is the current through each one of the six constant-current-sink channels. Adjust the current through ISET to get analog dimming functionality by connecting the external control voltage to ISET through the R_{ISET2} resistor. The resulting change in the LED current with the control voltage is linear and inversely proportional. The LED current control range remains between 20mA to 120mA.

Use the following equation to calculate the LED current set by the control voltage applied:

$$I_{OUT\_} = \frac{1500}{R_{ISET}} + \frac{(1.23 - V_C)}{R_{ISET2}} \times 1220$$

PCB Layout Considerations

LED driver circuits based on the MAX20056B use a high-frequency switching converter to generate the voltage for LED strings. Take proper care while laying out the circuit to ensure proper operation. The switching-converter part of the circuit has nodes with very fast voltage changes that could lead to undesirable effects on the sensitive parts of the circuit. Follow the guidelines below to reduce noise as much as possible:

1) Connect the bypass capacitor on V_{CC} as close as possible to the device and connect the capacitor ground to the signal ground plane using vias close to the capacitor terminal. Connect SGND of the device to the signal ground plane using a via close to SGND. Lay the signal ground plane on the inner layer, preferably next to the top layer. Use the signal ground

plane to cover the entire area under critical signal components for the power converter.

2) Have a power ground plane for the switching-converter power circuit under the power components (input filter capacitor, output filter capacitor, inductor, MOSFET, rectifier diode, and current-sense resistor). Connect PGND to the power ground plane as close to PGND as possible. Connect all other ground connections to the power ground plane using vias close to the terminals.

3) There are two loops in the power circuit that carry high-frequency switching currents: One loop is when the MOSFET is on (from the input filter-capacitor positive terminal, through the inductor, the internal MOSFET, and the current-sense resistor, to the input capacitor negative terminal). The other loop is when the MOSFET is off (from the input capacitor positive terminal, through the inductor, the rectifier diode, output filter capacitor, to the input capacitor negative terminal). Analyze these two loops and make the loop areas as small as possible. Wherever possible, have a return path on the power ground plane for the switching currents on the top-layer copper traces, or through power components. This reduces the loop area considerably and provides a low-inductance path for the switching currents. Reducing the loop area also reduces radiation during switching.

4) Connect the power ground plane for the constant-current LED driver part of the circuit to LEDGND as close as possible to the device. Connect SGND to PGND at the same point.

5) Add a small bypass capacitor (22pF to 47pF) to the OVP input. Place the capacitor as close as possible to the pin to suppress high-frequency noise.

6) The trace from the LED connector to the output capacitors should start directly at the output capacitors, rather than at the boost-diode cathode.

7) Use wide traces and multiple vias to connect all input and output capacitors directly to the ground plane beneath them.

8) Refer to the MAX20056B evaluation kit for an example layout.

Typical Operating Circuits

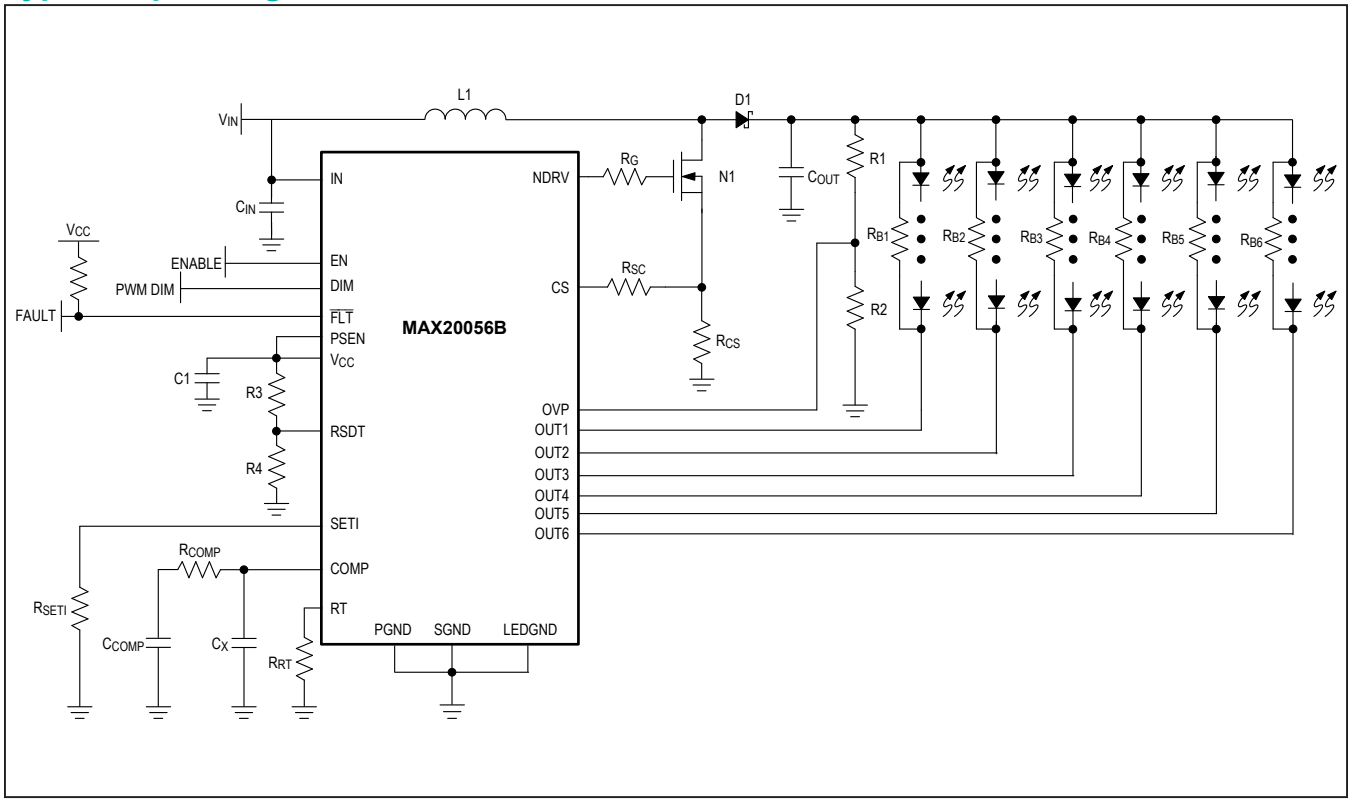


Figure 12. Boost Topology

Typical Operating Circuits (continued)

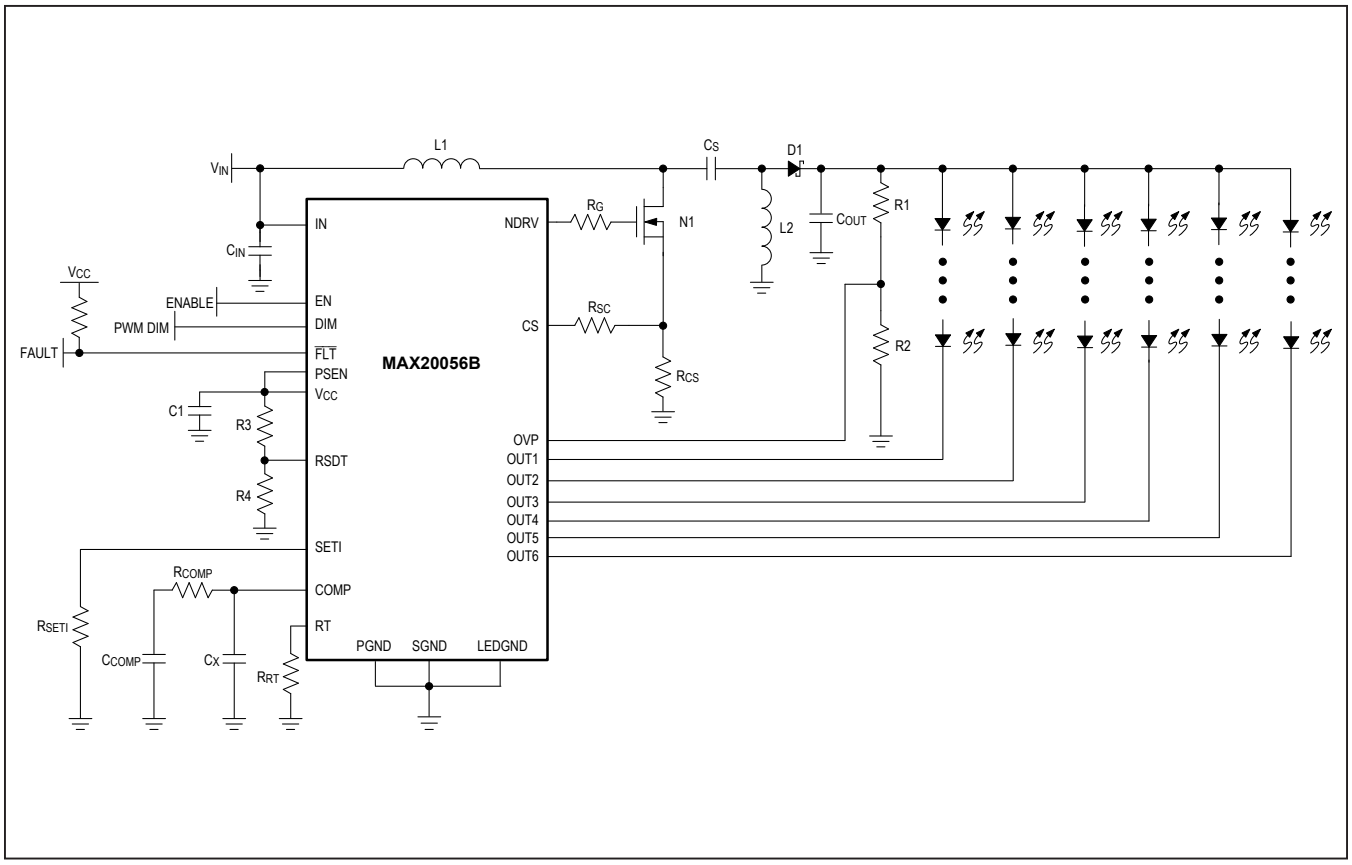


Figure 13. SEPIC Topology

Typical Operating Circuits (continued)

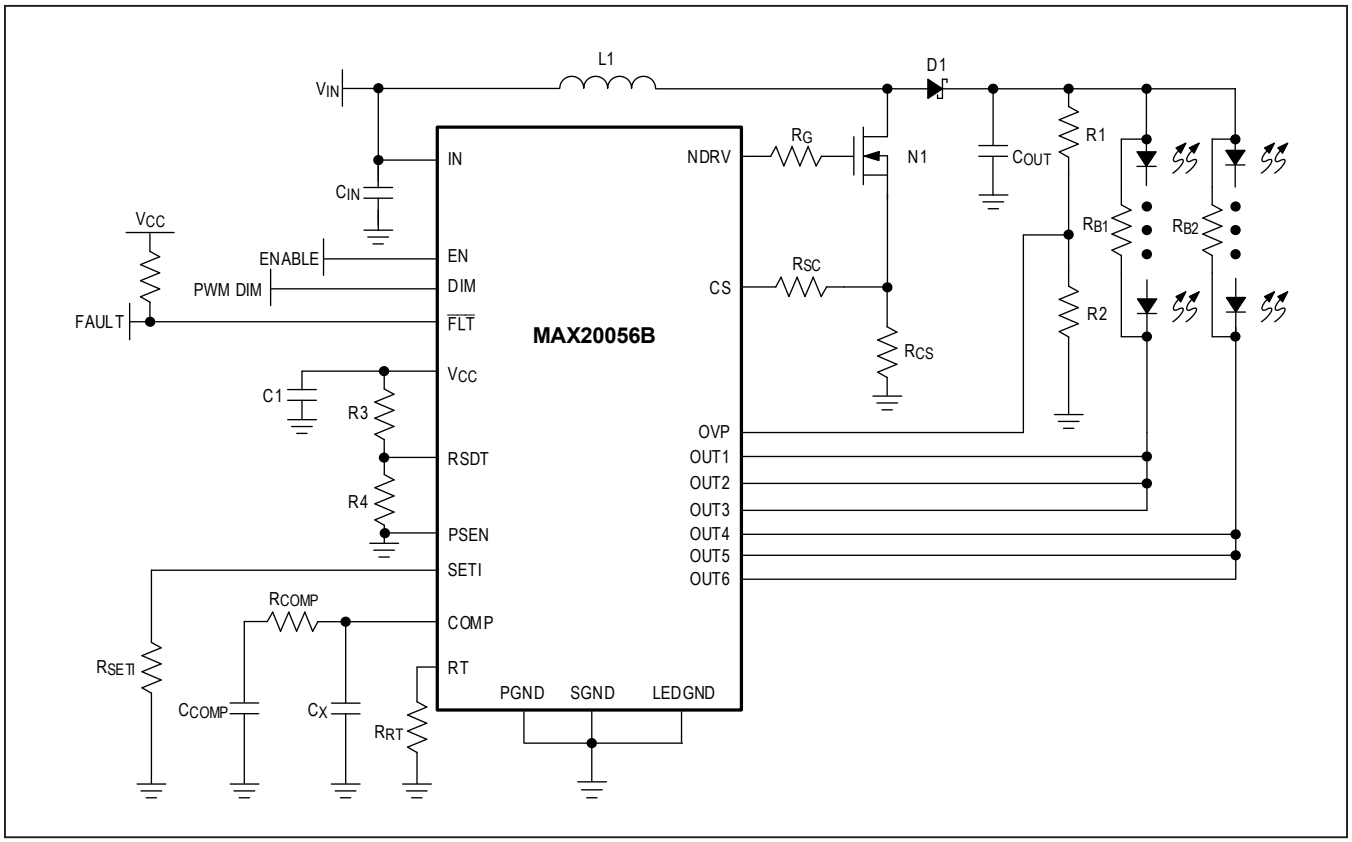


Figure 14. Boost Topology with Multiple Current Sinks Connected in Parallel for > 120mA per LED String (Phase Shifting Disabled Only)

Ordering Information

PART	TEMPERATURE RANGE	PIN-PACKAGE	START-UP
MAX20056BAUGA/V+	-40°C to +125°C	24 TSSOP-EP	Standard
MAX20056BAUGB/V+	-40°C to +125°C	24 TSSOP-EP	Fast

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TSSOP-EP	U24E+2C	21-0772	90-0468

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/18	Initial release	—
1	11/18	Added future-part designation to MAX20056BAUGB/V+ in *Ordering Information*	25
2	1/19	Removed future-part designation from MAX20056BAUGB/V+ in *Ordering Information*	25
3	3/19	Updated IL_{AVG} equation for SEPIC configuration in *Applications Information*	20
4	9/19	Updated *Absolute Maximum Ratings* and *Package Thermal Characteristics*	2