# MAX22505

# ±40V High-Speed USB Port Protector

## General Description

The MAX22505 is designed to protect a USB port on commercial and industrial equipment against damage due to faulty or incorrectly wired power supplies. The USB port is protected against connection to typical $24V_{DC}$ or $24V_{AC}$ systems with a max data line protection of ±40.7V and power/ground line protection up to ±50V.

$V_{BUS}$, ground and connector shield connections can be configured for any level of ESD, burst, and surge protection by choosing external components. USB data D+ and D- are protected by external diode clamps to $V_{BUS}$ and GND, allowing for the lowest possible insertion loss while providing high ESD and Burst protection.

The MAX22505 is housed in a 24-pin, 4mm x 4mm TQFN package with exposed pad and is specified for operation over the -40°C to +105°C temperature range.

## Applications

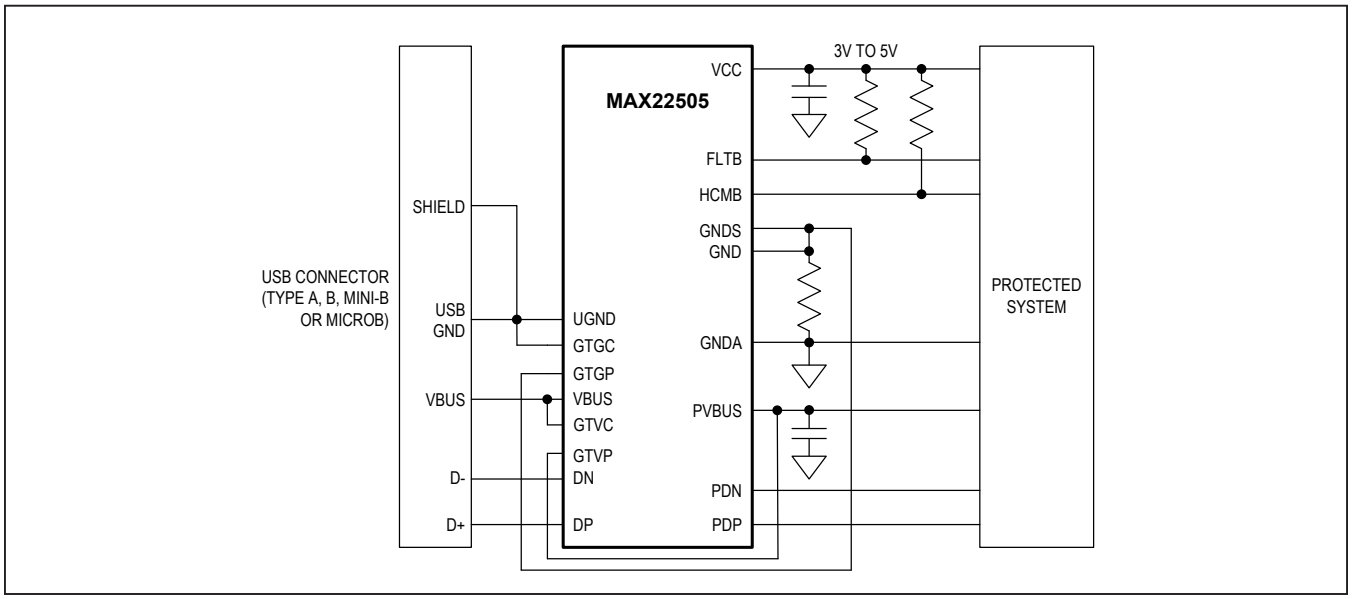
- Industrial PC
- Programmable Logic Controller (PLC)
- Diagnostic USB port

## Benefits and Features

- Robust Communications
  - Integrated ±50V dc Protection for $V_{BUS}$/GND
  - Integrated ±40.7V dc Protection for D+/D-
  - Thermal Shutdown Protected
  - -40°C to +105°C Operating Temperature
- High Performance
  - High (480Mb), Full (12Mb), and Low (1.5Mb) Speed Capable
  - 3.0V to 5.5V Supply Voltage
  - 4Ω (typ) $V_{BUS}$/D+/D- channel resistance
  - 1Ω (max) GND Channel Resistance
  - High-Speed USB Disable Mode Allowing Operation with High Common Mode Voltages
- Flexibility
  - Transparent to USB Operation Speeds
  - Configurationless USB Host or Device Protection
  - Optional External MOSFET driver for $V_{BUS}$ and GND Paths
- Supports USB OTG
- Simpler Than USB Isolation

***Ordering Information* appears at end of data sheet.**

## Application Block Diagram



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## Absolute Maximum Ratings

(Voltages referenced to GND.)

$V_{CC}$, FLTB, HCMB ..... -0.3V to +6.0V
DN to PDN, DP to PDP ..... -40.7V to +40.7V
$V_{BUS}$ to PVBUS, UGND to GNDS ..... -50.0V to +50.0V
GTGC to UGND ..... -0.3 to +6.0V
GTGP to GNDS ..... -0.3 to +6.0V
GTVC to $V_{BUS}$ ..... -0.3 to +6.0V
GTVP to PVBUS ..... -0.3 to +6.0V
PVBUS ..... -0.3V to +6.0V
GNDS ..... -0.6V to +0.6V
PDN, PDP ..... -0.3V to +6.0V

Continuous Current
GTGC, GTGP, GTVC, GTVP ..... 10mA
$V_{BUS}$ to PVBUS, UGND to GNDS ..... 280mA
Any other pin ..... 50mA
Continuous Power Dissipation ($T_A$ = +70°C)
T2444-2C TQFN (Multi Layer)
(derate by 25.6mW/°C above +70°C) ..... 2051mW
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Thermal Characteristics (Note 1)

TDFN (Multi-Layer PCB)
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .....39°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$) .....6°C/W

TDFN (Single-Layer PCB)
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .....56°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$) .....6°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{CC}$ = +3.0V to +5.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$ = 5.0V, $T_A$ = +25°C.) Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Supply Voltage Range | $V_{CC}$ | | 3.0 | | 5.5 | V |
| Supply Voltage Range | $V_{CC}$ | External MOSFETs present | 4.75 | | 5.5 | V |
| Supply Current | $I_{CC}$ | | | 3.8 | 5.9 | mA |
| Power-On Reset Voltage | $V_{POR}$ | Measured at $V_{CC}$ | | 2.75 | | V |
| Power-On Reset Delay | $t_{POR}$ | | | 10 | | ms |
| GTGC Voltage | $V_{GTGC}$ | $V_{GTGC}$ - $V_{UGND}$, $V_{CC}$ ≥ 4.75V, $I_{GTGC}$ = 0.5µA | 4.5 | 5.1 | 5.7 | V |
| GTGP Voltage | $V_{GTGP}$ | $V_{GTGP}$ - $V_{GND}$, $V_{CC}$ ≥ 4.75V, $I_{GTGP}$ = 0.5µA | 4.5 | 5.1 | 5.7 | V |
| GTVC Voltage | $V_{GTVC}$ | $V_{GTVC}$ - $V_{VBUS}$, $V_{CC}$ ≥ 4.75V, $I_{GTVC}$ = 0.5µA | 4.5 | 5.1 | 5.7 | V |
| GTVP Voltage | $V_{GTVP}$ | $V_{GTVP}$ - $V_{PVBUS}$, $V_{CC}$ ≥ 4.75V, $I_{GTVP}$ = 0.5µA | 4.5 | 5.1 | 5.7 | V |
| **GND CHANNEL** | | | | | | |
| On Resistance | $R_{ONGND}$ | | | 0.5 | 1.0 | Ω |
| On Resistance Flatness | $R_{ONGND\ FLAT}$ | -0.3V ≤ $V_{UGND}$ ≤ +0.3V | | | 0.1 | Ω |
| GND Resistor | $R_{GND}$ | UGND to GND | | 50 | | kΩ |

## Electrical Characteristics (continued)

($V_{CC}$ = +3.0V to +5.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$ = 5.0V, $T_A$ = +25°C.) Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **$V_{BUS}$ CHANNEL** | | | | | | |
| On Resistance | $R_{ONVB}$ | | | 4 | 5.6 | Ω |
| On Resistance Flatness | $R_{ONVBFLAT}$ | 0V ≤ $V_{BUS}$ ≤ +5.0V | | | 0.5 | Ω |
| Off Leakage Current | $I_{PVBUSOFFL}$ | Measured at PVBUS, $V_{BUS}$ = +50V or -50V, $V_{PVBUS}$ = 0V or 5V | | 150 | | µA |
| $V_{BUS}$ Resistance | $R_{VBUS}$ | VBUS to GND | | 50 | | kΩ |
| **D+ AND D- CHANNEL** | | | | | | |
| On Resistance | $R_{OND}$ | 0V ≤ $V_D$ ≤ +3.6V, PVBUS = 5V | | 4 | 6.2 | Ω |
| On Resistance Flatness | $R_{ONDFLAT}$ | 0V ≤ $V_D$ ≤ +3.6V, PVBUS=5V | | | 0.1 | Ω |
| Off Leakage Current | $I_{DOFFL}$ | $V_{DP}$ or $V_{DN}$ = +40.7V or - 40.7V, $V_{PDN}$ or $V_{PDP}$ = 0V | | 500 | | µA |
| On Leakage Current | $I_{DONL}$ | $V_{DP}$ or $V_{DN}$ = +0.4V or +3.3V | | 3 | | µA |
| **DIGITAL IO** | | | | | | |
| HCMB Input Logic-High | $V_{IH}$ | Sampled at POR | 1.4 | | | V |
| HCMB Input Logic-Low | $V_{IL}$ | Sampled at POR | | | 0.4 | V |
| Open-Drain Logic-Low | $V_{OL}$ | $I_{OD}$ = 5mA | | | 0.3 | V |
| Open-Drain Leakage | $I_{ODL}$ | $V_{OD}$ = 5.0V | | 1 | | µA |
| **FAULT DETECTION CHARACTERISTICS** | | | | | | |
| Fault Negative Threshold Low | $V_{N\_L}$ | Falling Edge | -0.22 | -0.21 | -0.20 | V |
| Fault Negative Threshold High | $V_{N\_H}$ | Falling Edge | -0.9 | -0.85 | -0.8 | V |
| Fault Positive Threshold Low | $V_{P\_L}$ | Rising Edge | 0.20 | 0.21 | 0.22 | V |
| Fault Comparator Hysteresis | | | | 1 | | % |
| $V_{BUS}$ Fault Detection Threshold | $V_{B\_H}$ | Rising Edge | 5.8 | 6.1 | 6.4 | V |
| $V_{BUS}$ Fault Detection Hysteresis | | | | 1 | | % |
| Data Fault Detection Threshold | $V_{D\_H}$ | Rising Edge | 4.0 | 4.2 | 4.4 | V |
| Data Fault Detection Hysteresis | | | | 1 | | % |
| $V_{BUS}$ Detect Threshold | $V_{BDET}$ | Measured at PVBUS to GND Rising Edge | 3.8 | 4 | 4.2 | V |

## Electrical Characteristics (continued)

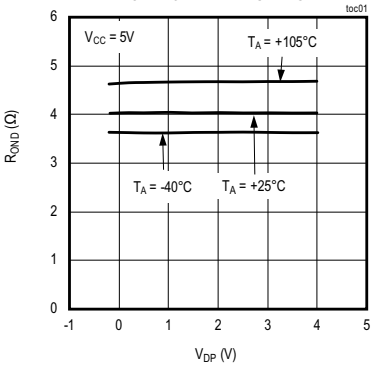
($V_{CC}$ = +3.0V to +5.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$ = 5.0V, $T_A$ = +25°C.) Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Differential $V_{BUS}$ Detect Threshold | $V_{BDETD}$ | Measured at $V_{BUS}$ to UGND on PVBUS Rising Edge | 3.7 | 4 | 4.3 | V |
| $V_{BUS}$ Detect Hysteresis | | | | 0.5 | | V |
| GNDS Positive Threshold | $V_{GSTHP}$ | Rising Edge | 45 | 50 | 55 | mV |
| GNDS Negative Threshold | $V_{GSTHN}$ | Falling Edge | -55 | -50 | -45 | mV |
| GNDS Threshold Hysteresis | | | | 1 | | % |
| UGND and $V_{BUS}$ Path Soft-Start Time | $t_{SS}$ | | | 10 | | ms |
| Fault Response Time | $t_{FAULT}$ | From any positive fault value + 0.5V or negative fault value – 0.5V till switch off | | 0.5 | 0.9 | µs |
| Fault Recovery Time | $t_{RECOVER}$ | Fault voltage removed till switches close | | 30 | | ms |
| $V_{BUS}$ Detect Debounce Time | $t_{VBDB}$ | | | 30 | | ms |
| GND Debounce Time | $t_{GDB}$ | | | 30 | | ms |
| **USB PERFORMANCE** | | | | | | |
| Crosstalk | $V_{CT}$ | Between DN and DP channels $V_{DP}$, $V_{DN}$ = 0dBm, $R_L$ = $R_S$ = 50Ω, f = 240MHz | | -40 | | dB |
| On Capacitance | $C_{ON}$ | DN and DP channels, f = 240MHz | | 10 | | pF |
| **PROTECTION** | | | | | | |
| ESD | | All pins - HBM | | 2 | | kV |
| Thermal Shutdown Threshold | $T_{SHDN}$ | Temperature rising, until switches open | | +150 | | °C |
| Thermal Shutdown Hysteresis | $T_{SHDN\_HYS}$ | | | 20 | | °C |

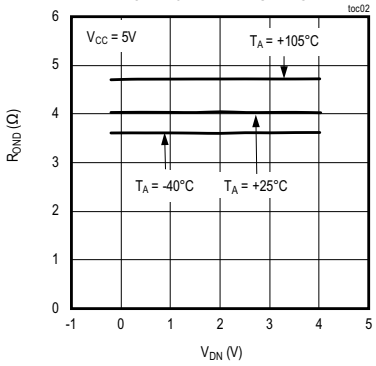
## Typical Operating Characteristics

$V_{CC}$ = 5.0V, $T_A$ = +25°C unless otherwise noted

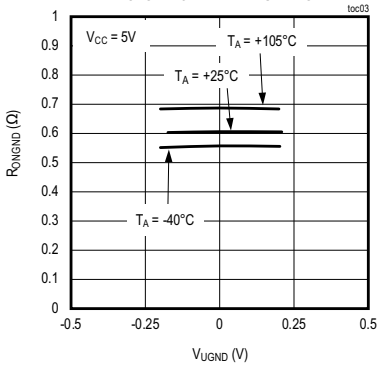
ON RESISTANCE vs. DP CHANNEL VOLTAGE



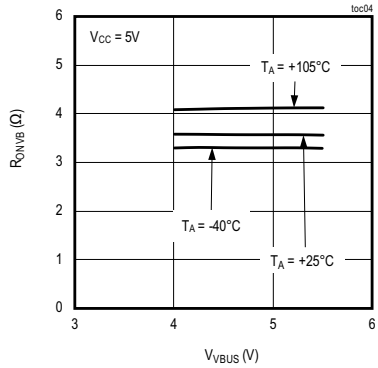

ON RESISTANCE vs. DN CHANNEL VOLTAGE



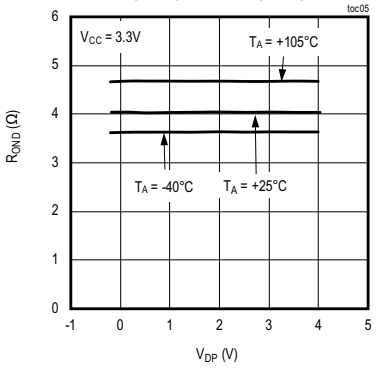

ON RESISTANCE vs. GND CHANNEL VOLTAGE



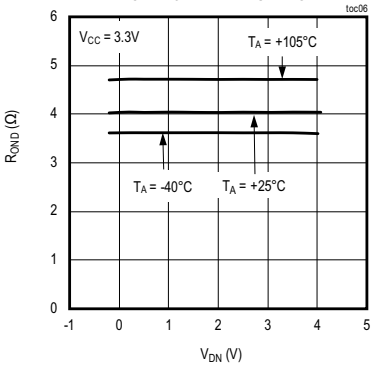

ON RESISTANCE vs. VBUS CHANNEL VOLTAGE



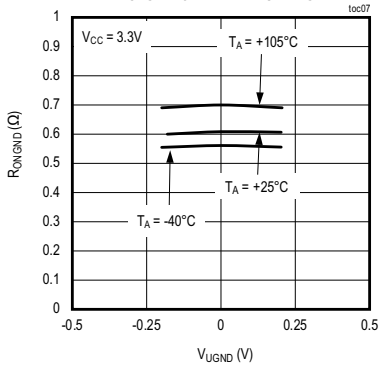

ON RESISTANCE vs. DP CHANNEL VOLTAGE



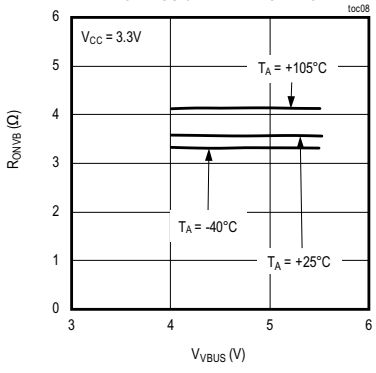

ON RESISTANCE vs. DN CHANNEL VOLTAGE



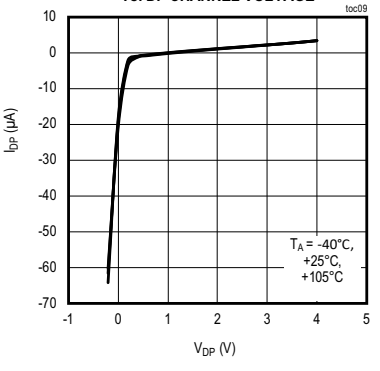

ON RESISTANCE vs. GND CHANNEL VOLTAGE




ON RESISTANCE vs. VBUS CHANNEL VOLTAGE



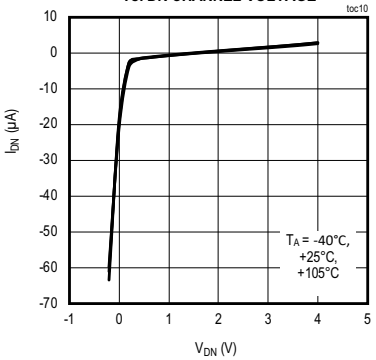

ON LEAKAGE vs. DP CHANNEL VOLTAGE



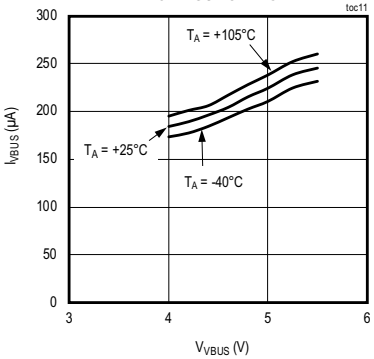
## Typical Operating Characteristics (continued)

$V_{CC}$ = 5.0V, $T_A$ = +25°C unless otherwise noted

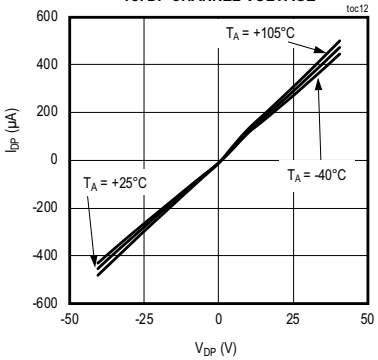
ON LEAKAGE vs. DN CHANNEL VOLTAGE



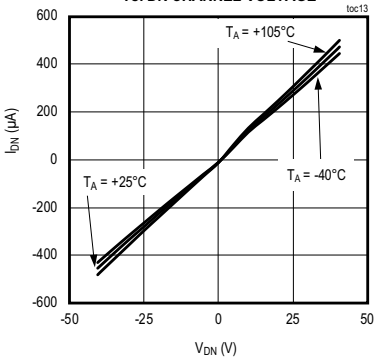

ON LEAKAGE vs. VBUS VOLTAGE



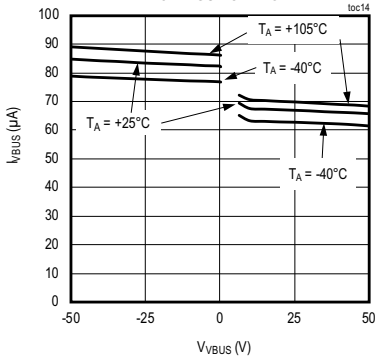

OFF LEAKAGE vs. DP CHANNEL VOLTAGE



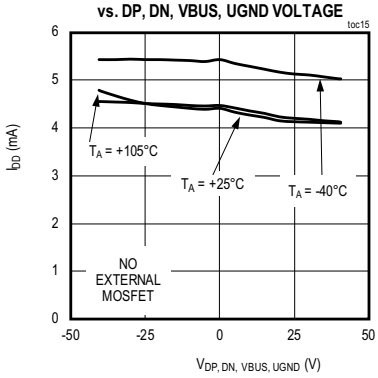

OFF LEAKAGE vs. DN CHANNEL VOLTAGE



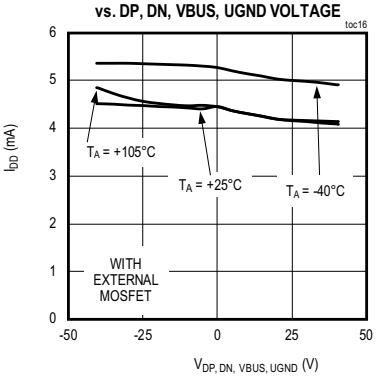

OFF LEAKAGE vs. VBUS VOLTAGE



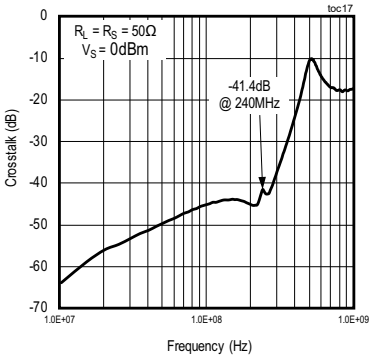

SUPPLY CURRENT vs. DP, DN, VBUS, UGND VOLTAGE



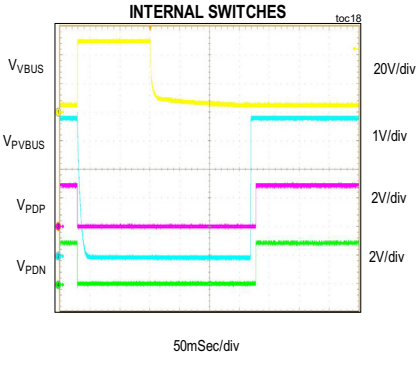

SUPPLY CURRENT vs. DP, DN, VBUS, UGND VOLTAGE




DP/DN CROSSTALK vs. FREQUENCY



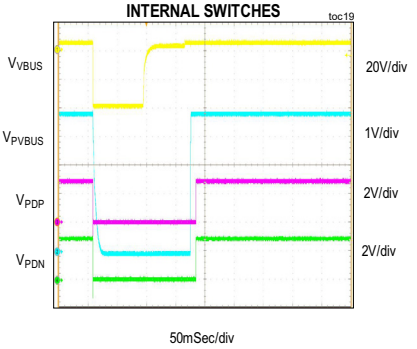

PROTECTION AND RECOVERY POSITIVE VBUS FAULT INTERNAL SWITCHES



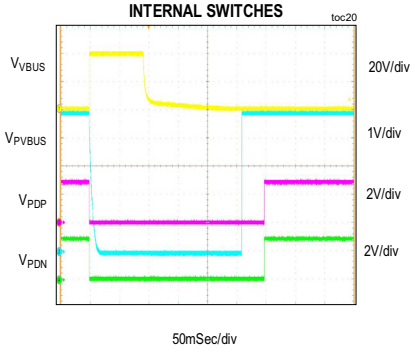
## Typical Operating Characteristics (continued)

$V_{CC}$ = 5.0V, $T_A$ = +25°C unless otherwise noted

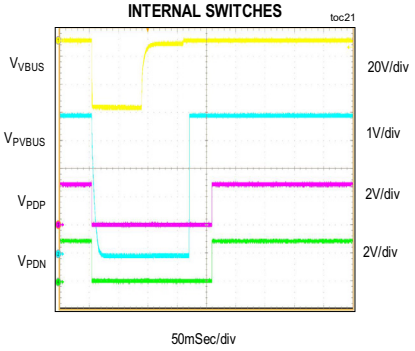
PROTECTION AND RECOVERY
NEGATIVE VBUS FAULT
INTERNAL SWITCHES



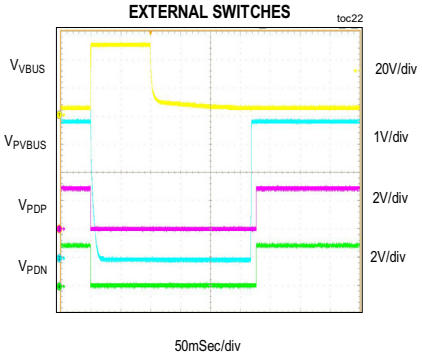

PROTECTION AND RECOVERY
POSITIVE UGND FAULT
INTERNAL SWITCHES



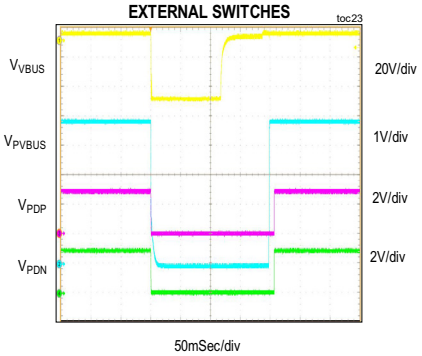

PROTECTION AND RECOVERY
NEGATIVE UGND FAULT
INTERNAL SWITCHES



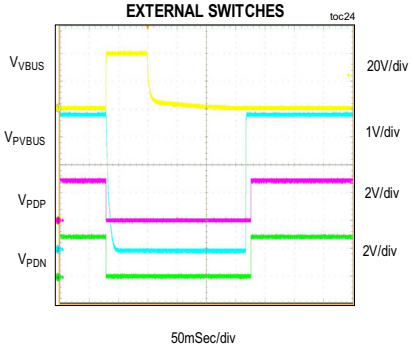

PROTECTION AND RECOVERY
POSITIVE VBUS FAULT
EXTERNAL SWITCHES



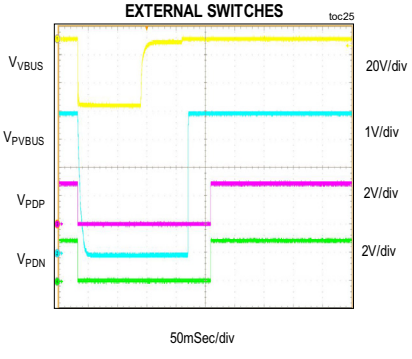

PROTECTION AND RECOVERY
NEGATIVE VBUS FAULT
EXTERNAL SWITCHES



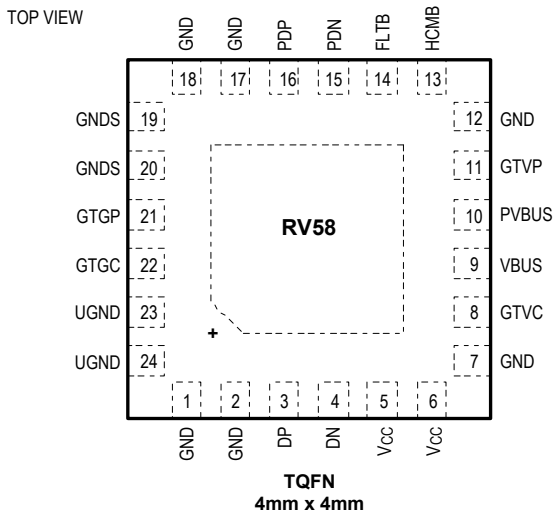

PROTECTION AND RECOVERY
POSITIVE UGND FAULT
EXTERNAL SWITCHES




PROTECTION AND RECOVERY
NEGATIVE UGND FAULT
EXTERNAL SWITCHES



## Pin Configuration




**TQFN**
**4mm x 4mm**

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 2, 7, 12, 18 | GND | Ground. GND is the ground for the MAX22505. Connect all GND pins and the exposed pad together. Connect GND to GNDS for applications with no external MOSFETs. Connect GND to GNDA for all other applications. |
| 3 | DP | USB Connector D+ Data Line Connection. Use 90Ω differential pair transmission line routing with the D- data line to the USB connector. Connect DP to an external diode bridge clamp for high ESD and Burst protection. See applications section for details. |
| 4 | DN | USB Connector D- Data Line Connection. Use 90Ω differential pair transmission line routing with the D+ data line to the USB connector. Connect DN to an external diode bridge clamp for high ESD and Burst protection. See applications section for details. |
| 5, 6 | $V_{CC}$ | Power Supply. bypass to ground with a minimum 1µF ceramic capacitor as close to the device as possible. Connect all VCC pins together. These two pins may share one external bypass capacitor. |
| 8 | GTVC | Optional Gate Drive for External MOSFET with Source Connected to USB Connector VBUS Pin. Use external MOSFETs to reduce VBUS path on resistance for high current applications. Connect back-to-back N-Channel MOSFETs as shown in Figures 3 and 4. Keep PCB trace as short as possible. In applications with no external MOSFETs, short GTVC to VBUS. |
| 9 | VBUS | USB Connector $V_{BUS}$ Connection. Bypass $V_{BUS}$ to GND with a snubber circuit for ESD protection. Bypass $V_{BUS}$ to UGND with a capacitor for USB host applications. See *Applications Information* for details. |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 10 | PVBUS | Protected $V_{BUS}$ Output. Bypass to ground with a minimum 1µF ceramic capacitor as close to the device as possible. PVBUS must have a total of ≥4.7 µF of distributed capacitance. Add an external TVS diode to absorb peak current if system has no other clamp. See applications section for details. |
| 11 | GTVP | Optional Gate Drive for External MOSFET with Source Connected to the PVBUS Pin. Use external MOSFETs to reduce $V_{BUS}$ path on resistance for high current applications. Connect back-to-back N-Channel MOSFETs, as shown in Figure 3 and Figure 4. Keep PCB trace as short as possible. In applications with no external MOSFETs, short GTVP to PVBUS. |
| 13 | HCMB | High Common Mode Voltage Indication Open-Drain Output, and Full-Speed Force Disable Input. The voltage value on HCMB is sampled at power up to determine if Full-Speed Fallback mode is enabled or disabled. Tie an external pullup to this pin to enable Full-Speed Fallback. After initial power-up, HCMB indicates if a high common mode voltage is present, causing the MAX22505 to force traffic to full speed data rates. HCMB drives active low when the common mode voltage detected at UGND exceeds the VN_L or VP_L thresholds. High impedance indicates normal operation. See Figure 1 for more details. |
| 14 | FLTB | Fault Indication Open Drain output. Connect an external pullup resistor to this pin if used. FLTB drives active low if MAX22505 detects any abnormal voltages at $V_{BUS}$, UGND, DP, or DN. High-impedance indicates normal operation. |
| 15 | PDN | Protected D- Data Line Connection. Use 90Ω differential pair transmission line routing with D+ data line to the system USB transceiver. Add external series 18nH to 22nH inductor. See applications section for details. |
| 16 | PDP | Protected D+ data line connection. Use 90Ω differential pair transmission line routing with D- data line to the system USB transceiver. Add external series 18nH to 22nH inductor. See *Applications Information* for details. |
| 17 | GNDA | Analog Ground. |
| 19, 20 | GNDS | Ground Sense. Output from internal GND path switch and sense point for external UGND to GND MOSFETs. REQUIRED - Connect a current sense resistor, as shown in Figure 2, Figure 3, and Figure 4. Connect all GNDS pins together. |
| 21 | GTGP | Optional Gate Drive for External MOSFET with Source Connected to Protected System Ground. Use external MOSFETs to reduce GND path on resistance for high current applications. Connect back-to-back N-Channel MOSFETs as shown in Figure 3 and Figure 4. Keep PCB trace as short as possible. In applications with no external MOSFETs, short GTGP to GNDS. |
| 22 | GTGC | Optional Gate Drive for External MOSFET with Source Connected to USB Connector Ground Pin. Use external MOSFETs to reduce GND path on resistance for high current applications. Connect back-to-back N-Channel MOSFETs as shown in Figure 3 and Figure 4. Keep PCB trace as short as possible. In applications with no external MOSFETs, short GTGC to to UGND |
| 23, 24 | UGND | USB Connector Ground Connection. Bypass UGND to GND with a snubber circuit for ESD protection. See *Applications Information* for details. USB connector shield may be connected to UGND. Connect all UGND pins together. |
| — | EP | Exposed Pad. Connect EP to GND. Exposed pad must not be left unconnected. |

## Detailed Description

The MAX22505 is designed to protect a USB port on commercial and industrial equipment against damage due to faulty or incorrectly wired power supplies. The USB port is protected against connection to typical $24V_{DC}$ or $24V_{AC}$ systems with a max data line protection of ±40.7V and power/ground line protection of ±50V.

$V_{BUS}$, ground and connector shield connections can be configured for any level of ESD, burst and surge protection by choosing external TVS devices. USB data D+ and D- are protected by external diode clamps to $V_{BUS}$ and GND allowing for the lowest possible insertion loss while providing high ESD and Burst protection.

### Internal Protection Switches

The MAX22505 contains 4 switch paths used to protect a typical USB bus connection. When all inputs to the potentially unsafe side (UGND, $V_{BUS}$, DP, DN) exhibit normal operation voltage, the MAX22505 connects these to the corresponding protected side inputs (GNDS, PVBUS, PDP, PDN).

The ground power path protects the USB connector GND. The ground protection path features a 1.0Ω max on resistance to minimize power loss and maintain signal integrity for USB data signals. The $V_{BUS}$ path protects the USB connector 5V power rail and features a 4Ω typical on resistance. The USB data line path features low shunt capacitance (10pF, typ) and 4Ω typ on resistance to maintain good USB signal integrity. When an out of limit voltage appears at any of the potentially unsafe inputs (UGND, $V_{BUS}$, DN or DP), all of the switches automatically open. The ground connection also features current detection implemented by an external sense resistor connected between GNDS and the system GND. When the voltage at GNDS is above +50mV or below -50mV, all switches are opened. The MAX22505 will automatically return to the idle state.

All switch paths default to open if the $V_{CC}$ supply is not present.

### Operation

The MAX22505 will enter into protection mode when any of the potentially unsafe inputs exceed normal operation voltages. Except for overvoltage or undervoltage faults on $V_{BUS}$ alone, the MAX22505 will remain in protection mode, for at least 30ms. In the case of overvoltage or undervoltage faults on $V_{BUS}$ alone, the MAX22505 auto-restarts after 30ms.

Voltage drops on the cable can cause operation issues with high speed USB due to common mode shifts in the USB data. The MAX22505 can detect a high common mode condition using comparators on UGND. The comparator threshold (-0.21V to +0.21V) determines if high-speed USB operation is allowed. If at initial power up (voltage applied to $V_{CC}$), a pullup is attached to HCMB, the automatic USB full-speed fallback circuit is enabled. If no pullup is attached or a pullup is attached after $V_{CC}$ is applied, the automatic USB full-speed fallback circuit is disabled.

When the MAX22505 indicates a fault, it disconnects the potentially unsafe side from the protected side. A fault occurs when the voltages on $V_{BUS}$, DP, or DN fall outside their respective window thresholds. A fault also occurs upon detection of an overcurrent on UGND.

When the automatic full-speed fallback circuit is enabled, a window comparator on UGND determines if and when to fall back from USB High-Speed to Full/Low Speed. To use this feature, the current sense resistor value on GNDS must be set such that an overcurrent condition would trigger at a higher window threshold than the comparators triggering the fall back. An incorrect sense resistor value would cause the MAX22505 to disconnect the potentially unsafe side from the protected side before fall back could occur.

### Full-Speed Fallback Mode

The MAX22505 has the ability to automatically restrict the USB bus speed to low and full (1.5Mbps and 12Mbps) speed if large common mode voltages are detected. This feature allows the USB bus to remain operational in cases where the common mode voltage exceeds the USB high speed receiver capability but could still operate at low and full speed. Table 1 details full-speed fallback mode settings.

**Table 1. Full Speed Fallback Mode Settings**

| VOLTAGE AT HCMB AT POR | HIGH COMMON MODE DETECTED | USB BUS SPEED |
|---|---|---|
| Low | Ignored | No Limit |
| High | No | No Limit |
| High | Yes | Limited to Full-Speed |

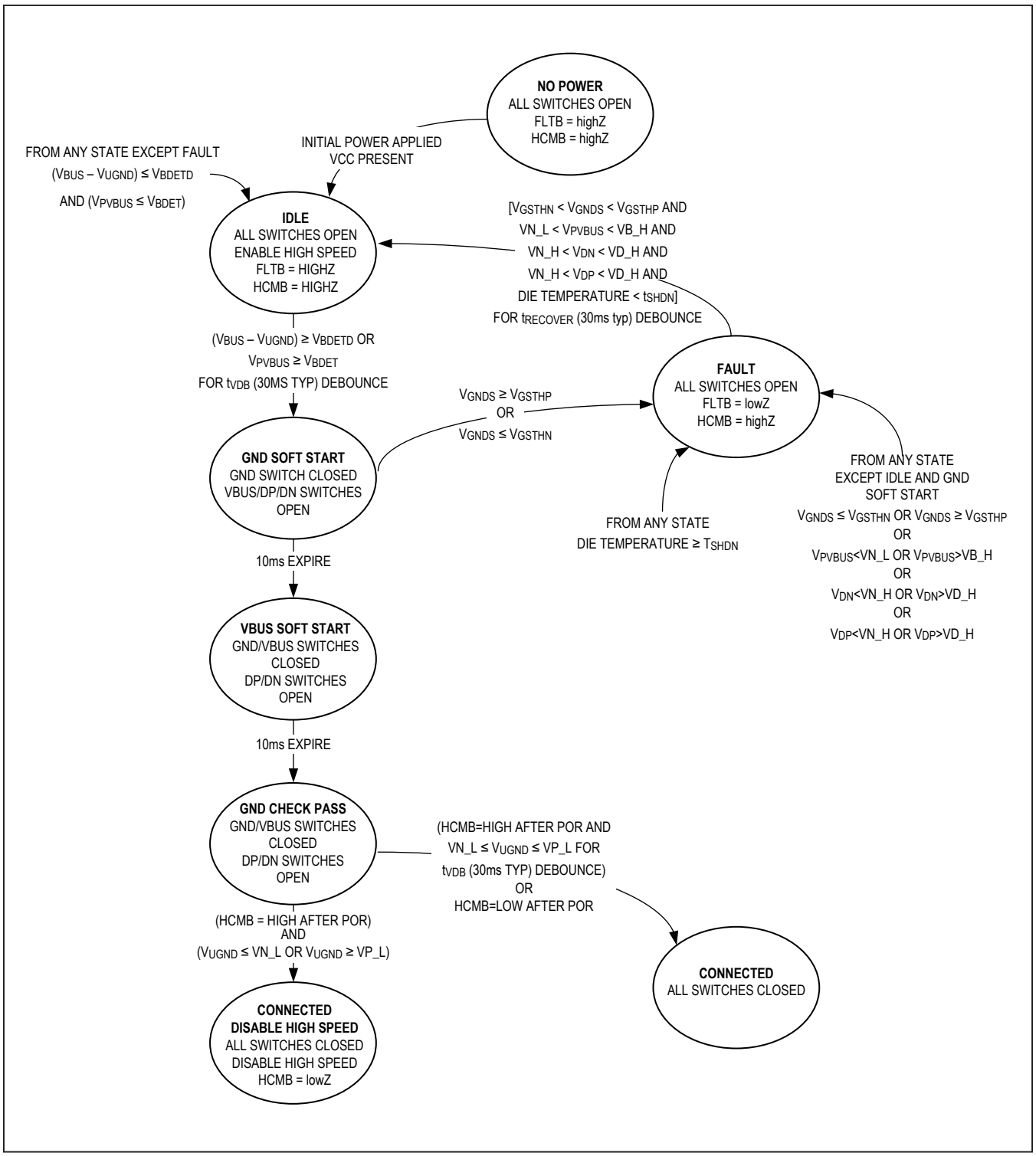



*Figure 1. Operation State Diagram*

### Thermal Shutdown Protection

The MAX22505 is protected against high thermal dissipation with internal thermal shutdown detection. If the die temperature exceeds 150°C typ, all switch paths will open. The switch paths will remain open until the die cools by 20°C which will cause the MAX22505 to automatically close the switch paths if the voltages at the inputs are in normal operating range.

## Applications Information

### ESD/Burst Protection

Figure 2, Figure 3 and Figure 4 describe the external protection required to protect up to ±15kV airgap and ±8kV contact discharge as per IEC61000-4-2, and clamp inductive surges due to external cable inductance during hot-plug and protection shutdown events. A 100nF capacitor must bypass VBUS to system ground, and a TVS diode

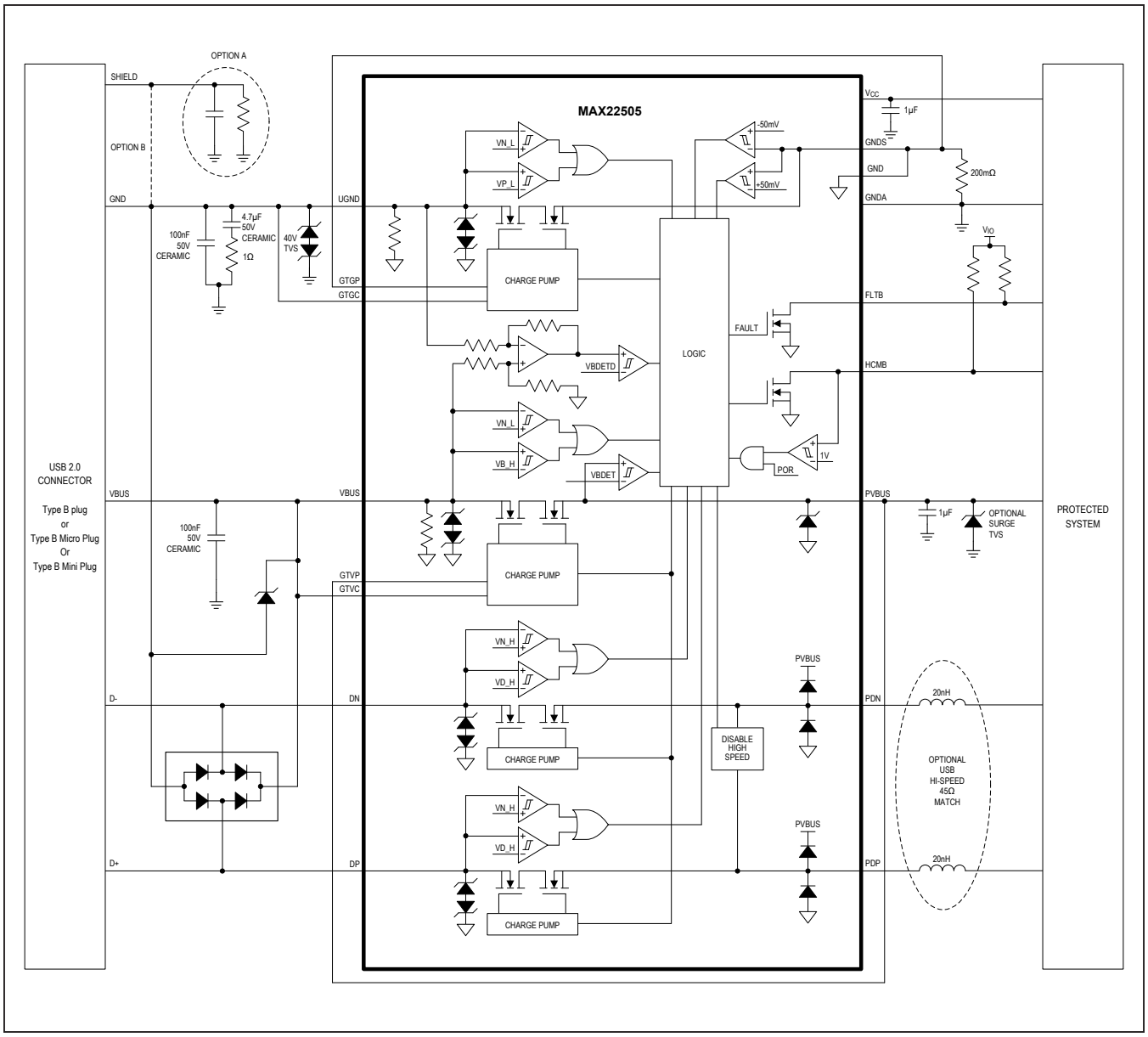



*Figure 2. USB Self-Powered Peripheral Application*

must connect between VBUS and UGND. A 40V TVS diode and a series RC snubber (4.7µF ceramic and 1Ω) bypassed with 100nF ceramic must connect UGND to system ground. The snubber is required to limit the voltage rise time caused by the MAX22505 turn-off with an inductive load (cable inductance). A diode bridge clamps D+ and D- to VBUS and to UGND, to absorb energy during a protection event. It is critical that the clamp diodes have extremely low junction capacitance with a reverse bias of 400mV (operation voltage range of High Speed USB). It is required to connect the 100nF VBUS and UGND bypass capacitors with the shortest possible PCB traces to the diode bridge and the ground plane so that the parasitic inductance on the ESD current path is minimized.

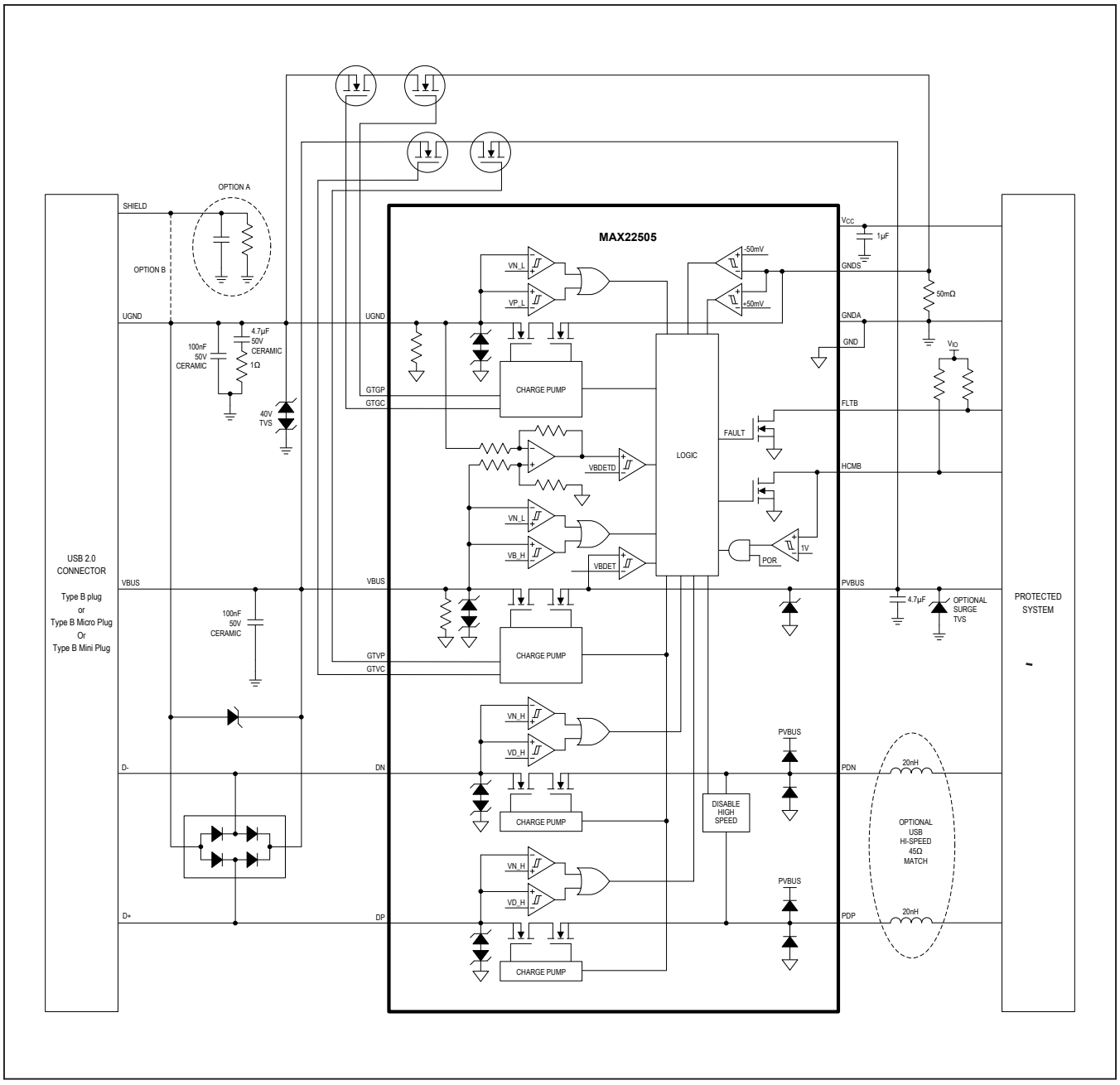



*Figure 3. USB Bus-Powered Peripheral Application*

## USB Self-Powered Peripheral Application

When the MAX22505 protects a system configured as a USB self-powered peripheral, the system draws little or no current from the USB bus. In this case, configure the MAX22505 as shown in Figure 2. Note that GND and GNDS are connected together. It is recommended to choose the resistor between GNDS and GNDA to set the current limit between 100mA and 250mA. The largest allowed current limit in this configuration is 250mA (200mΩ resistor). Using a larger current limit decreases the maximum voltage withstand capability, and could damage the MAX22505 during a fault condition.

## USB Bus Powered Peripheral Application

In a USB bus powered application, use external MOSFETs to decrease path resistance for $V_{BUS}$ and GND. In this case, configure the MAX22505 as shown in Figure 3. Note that GND and GNDA are connected together. Choose the resistor between GNDS and GNDA for the lowest current limit satisfying the application. Using a larger than necessary current limit results in large ground currents before the MAX22505 reacts to a fault condition.

## USB Host Application

In a USB host application (see Figure 4), use external MOSFETs to decrease path resistance for $V_{BUS}$ and GND. Note that GND and GNDA are connected together. The current limit set by the GNDS resistor must allow for ≥ 1A (50mΩ). A USB host is required to have a total bulk capacitance on $V_{BUS}$ of ≥ 120µF to allow for the inrush current of a connected USB peripheral. This can be split. Provisioning at least 100µF on the potentially unsafe side. The peripheral may have a capacitor up to 10µF (typically 1µF). Without any additional bulk capacitance between $V_{BUS}$ and UGND, this inrush current would cause the fault current limit to trip, shutting off the MAX22505. It is required to have a capacitor between $V_{BUS}$ and UGND to provide this peak inrush current to the attached peripheral.

In a host application, if the MAX22505 is powered up after a USB device is connected, and a leakage path exists charging UGND vs GND to a voltage, the MAX22505 may detect a fault when it is powered up. This is due to internal MAX22505 leakage charging the external ≥ 100µF $V_{BUS}$ capacitor. Two possible solutions to this are:

1) Unplug the external device, removing the leakage path, allowing UGND vs. GND to discharge to 0V. The MAX22505 will restart automaticaly.
2) Add a 1KΩ resistor between $V_{BUS}$ and UGND, to shunt the leakage current.

## External Component Recommendations and Requirements

### External MOSFETS

- N-Channel
- Gate: Specified for operation with $V_{GS}$ down to 4.5V. $V_{GS}$ max ≥ 10V, gate leakage ≤ 0.5µA On Resistance ≤ 100mΩ. Total voltage drop across 2 series MOSFET plus GNDS resistor should be < 0.15V at the application current
- Examples: Infineon BSR606N (90mΩ) or Diodes Inc DMN6040SFDE (47mΩ)

### Snubber capacitors

- Rated voltage must be 10V greater than max expected DC fault voltage. Specify ceramic with dielectric X5R/X7R or better.

### Snubber resistors

- 1Ω resistor: Use a high-power pulse rated resistor, rated for ≥ 700W for ≤ 2µs. Example: Ohmite AS12 series.

### $V_{BUS}$-UGND Bypass Capacitor for USB Host Application

- ESR ≤ 50mΩ (ceramic, tantalum or polymer electrolytic)
- 100µF ± 20%
- Voltage rating must be greater than or equal to maximum surge voltage of the external TVS, typically 10V.

### Diode clamp on DP/DN

- Low capacitance: for high-speed USB, ≤ 3pF at 400mV). For Full speed USB, ≤ 30pF at 3.3V
- Voltage rating: higher than max expected fault voltage
- High currents due to events such as IEC61000-4-2 ESD may damage the small diode bridge if a fault is applied to DP or DN independent of VBUS or GND. For independent fault protection, select a high current diode bridge with a separate TVS clamp.
- Diodes Inc DLPA004 (3.0pF max capacitance)

### TVS

- UGND to GND: SMAJ40CA from multiple vendors
- VBUS to UGND: SMAJ6.0A from multiple vendors, Diodes Inc, D5V0M1U2

## External MOSFET drivers

The MAX22505 internal power switches are designed for a USB self powered peripheral application. Self powered devices typically require very low currents <50mA from USB $V_{BUS}$ (e.g., powering the USB transceiver or as a USB attach detect signal). For $V_{BUS}$ currents higher than 50mA, or if the MAX22505 must provide current in a USB host application, decrease power voltage drops by adding external back-to-back N-channel MOSFETS, controlled by the GTGP/GTGC and GTVC/GTVP pins. VCC must be 5.0V ±5% when external MOSFETs are used. See Figure 3 and Figure 4. If using external MOSFETs, place them either on the GND path, or on both the $V_{BUS}$ path and the GND path. In no case should external MOSFETs be placed only on the $V_{BUS}$ path.Also, the total impedance in the GND path (internal + external + GNDS resistor) must always be equal to or lower than the total impedance in the $V_{BUS}$ path (internal + external).

To eliminate potential high frequency oscillations, the total length of the PCB trace from a gate drive pin through an external MOSFET to the source bypass capacitor must be less than 3cm total. For example, if a connection from MAX22505 gate drive pin (GTGP, GTGC, GTVP, GTVC) to the gate of an external MOSFET is 2cm, then the connection from the source of this MOSFET to system GND or to an external bupass capacitor, must be 1cm or less. If trace lengths exceed 3cm total, add a 10Ω resistor in series with the MOSFET gate to damp this potential oscillation.

## Improving USB signal quality

The MAX22505 adds minimal shunt capacitance on the D+ and D- lines. Any shunt capacitance on these lines changes the impedance of the transmission line, resulting in USB signal quality issues. Add a series inductor on each data line to compensate for this. Place these inductors as close to the shunt capacitance as possible. See application note AN4131 for more details **https://www.maximintegrated.com/en/app-notes/index.mvp/id/4131**

## Swap DP and DN

The MAX22505 USB data lines are symmetric. The DP to PDP path inside the MAX22505 matches the DN to PDN path. This can sometimes simplify PCB routing between the USB connector (or the USB transceiver) and the MAX22505. It is important to make sure that the path through the MAX22505 is consistent.

**Example 1:** USB connector D+ connected to DP and D- connected to DN. Then USB transceiver D+ must connect to PDP and D- must connect to PDN.

**Example 2:** USB connector D+ connected to DN and D- connected to DP. Then USB transceiver D+ must connect to PDN and D- must connect to PDP.

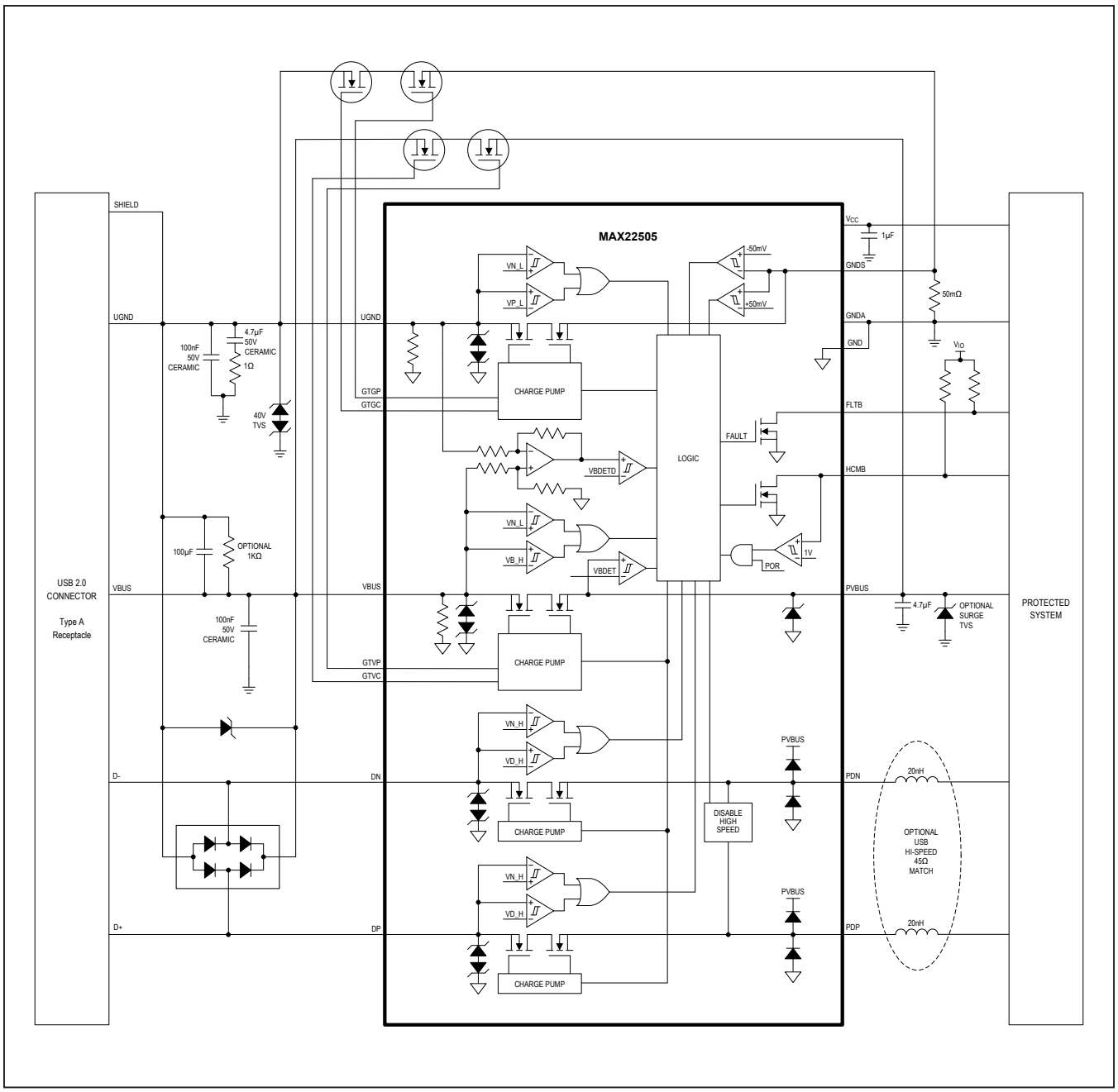
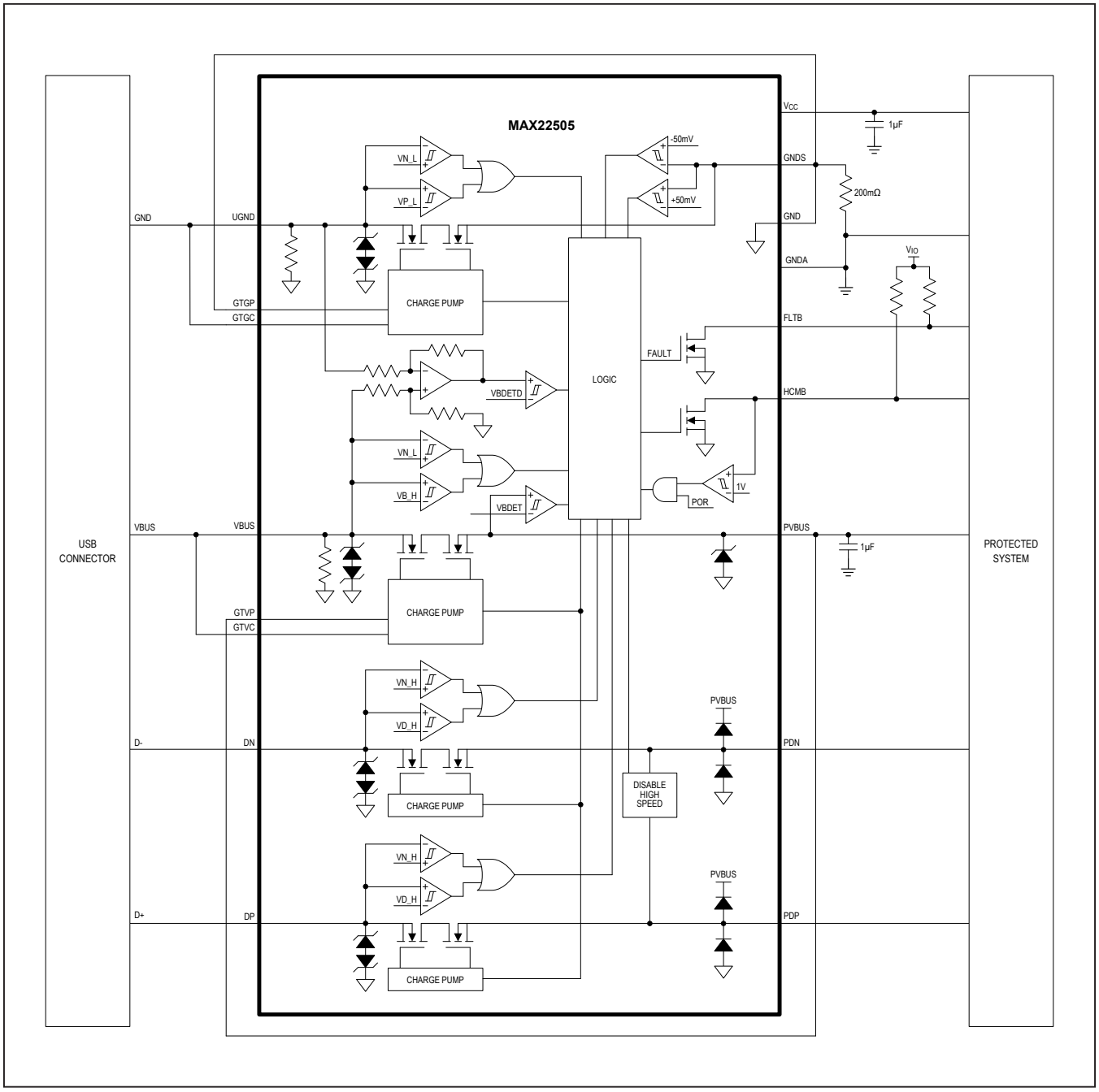



*Figure 4. USB Host Application*

## Functional Block Diagram



## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX22505GTG+ | -40°C to +105°C | 24 TQFN-EP |
| MAX22505GTG+T | -40°C to +105°C | 24 TQFN-EP |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

*T = Tape and reel.*

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 24 TQFN | T2444-4C | **21-0139** | **90-0022** |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 1/18 | Initial Release | — |
| 1 | 5/18 | Updated title, *Electrical Characteristics* table, *Applications Information,* and *Ordering Information* table | 1–18 |
| 2 | 6/20 | Updated Figures 2–4 | 12–13, 16 |