# MAPS-010144

## Digital Phase Shifter
## 4-Bit, 2.3 - 3.8 GHz

Rev. V3

### Features

- 4 Bit Digital Phase Shifter
- 360° Coverage with LSB = 22.5°
- Integrated CMOS Driver
- Serial or Parallel Control
- Low DC Power Consumption
- Minimal Attenuation Variation over Phase Shift Range
- 50 Ω Impedance
- EAR99
- Lead-Free 4 mm 24-Lead PQFN Package
- RoHS* Compliant

### Description

The MAPS-010144 is a GaAs pHEMT 4-bit digital phase shifter with an integrated CMOS driver in a 4 mm PQFN plastic surface mount package. Step size is 22.5° providing phase shift from 0° to 360° in 22.5° steps. This design has been optimized to minimize variation in attenuation over the phase shift range.

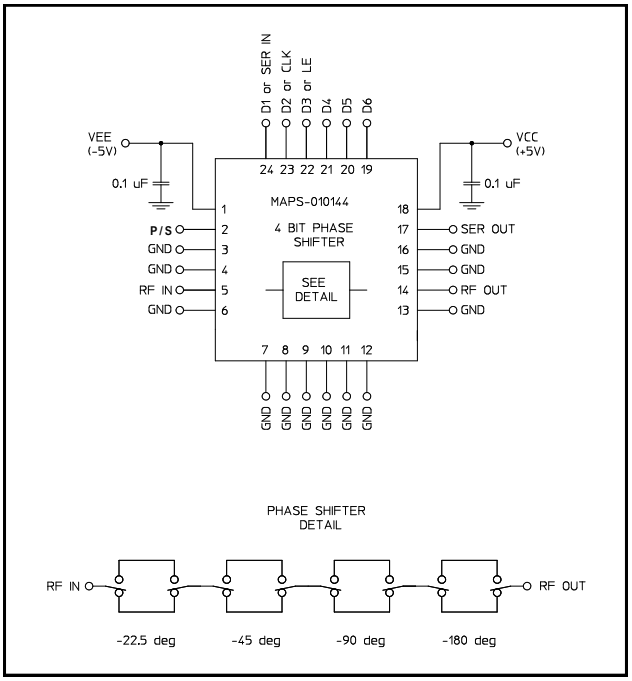
The MAPS-010144 is ideally suited for use where high phase accuracy with minimum loss variation over the phase shift range are required. The 4 mm PQFN package provides a smaller footprint than is typically available for a digital phase shifter with an internal driver. Typical applications include communications antennas and phased array radars.

### Ordering Information [1]

| Part Number | Package |
|---|---|
| MAPS-010144-TR0500 | 500 piece reel |
| MAPS-010144-001SMB | Sample Test Board |

1. Reference Application Note M513 for reel size information.

### Functional Schematic




### Pin Configuration [2]

| Pin No. | Function | Pin No. | Function |
|---|---|---|---|
| 1 | VEE | 13 | GND |
| 2 | P/S | 14 | RF OUT |
| 3 | GND | 15 | GND |
| 4 | GND | 16 | GND |
| 5 | RF IN | 17 | SER OUT |
| 6 | GND | 18 | VCC |
| 7 | GND | 19 | D6 |
| 8 | GND | 20 | D5 |
| 9 | GND | 21 | D4 |
| 10 | GND | 22 | D3 or LE |
| 11 | GND | 23 | D2 or CLK |
| 12 | GND | 24 | D1 or SER IN |

2. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

## Electrical Specifications:

**Freq. = 2.3 - 3.8 GHz, $T_A$ = 25°C, $Z_0$ = 50 Ω, $V_{CC}$ = +5.0 V, $V_{EE}$ = -5.0 V**

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| Operating Power [3] | 2.3 - 3.8 GHz | dBm | — | — | +25 |
| Insertion Loss (Any Phase State) | Any Phase State | dB | — | 2.5 | 4.5 |
| Attenuation Variation | Across All Phase States | dB | — | ± 0.5 | — |
| RMS Attenuation Error [4] | All Values Relative to Insertion Loss at Reference Phase | dB | — | 0.35 | — |
| RMS Phase Error [4] | All Values Relative to Reference Phase | deg | — | 2.5 | — |
| Phase Accuracy [5] Relative to Reference Loss State | 22.5 Degree Bit<br>45 Degree Bit<br>90 Degree Bit<br>180 Degree Bit<br>Sum of All Bits | deg | —<br>—<br>—<br>—<br>— | ± 1.5<br>± 1.5<br>± 3<br>± 4<br>± 4 | —<br>—<br>—<br>—<br>— |
| VSWR | RF IN<br>RF OUT | Ratio | —<br>— | 1.3:1<br>1.3:1 | —<br>— |
| 1 dB Compression | Reference State | dBm | — | 25 | — |
| Input IP3 | Two-tone inputs up to +5 dBm | dBm | — | 47 | — |
| $T_{RISE}$, $T_{FALL}$ | 10% to 90% RF, 90% to 10% RF | ns | — | 50 | — |
| $V_{CC}$<br>$V_{EE}$ | —<br>— | V | 3.0<br>-5.5 | —<br>-5.0 | 5.5<br>-3.0 |
| $V_{IL}$<br>$V_{IH}$ | LOW-level input voltage<br>HIGH-level input voltage | V | 0.0<br>0.7 x $V_{CC}$ | —<br>— | 0.3 x $V_{CC}$<br>$V_{CC}$ |
| $I_{IN}$ (Input Control Current) | $V_{IN}$ = $V_{CC}$ or GND | µA | — | 1 | — |
| $V_{OH}$<br>$V_{OL}$ | For serial out; $I_{OH}$ = -100 µA<br>For serial out; $I_{OL}$ = 100 µA | V | $V_{CC}$ - 0.2<br>— | —<br>— | —<br>0.2 |
| $I_{CC}$ (Quiescent Supply Current) | Vcntrl = $V_{CC}$ or GND | µA | — | — | 2 |
| $I_{EE}$ | $V_{EE}$ min to max<br>Vin = $V_{IL}$ or $V_{IH}$ | mA | -1.0 | -0.1 | — |

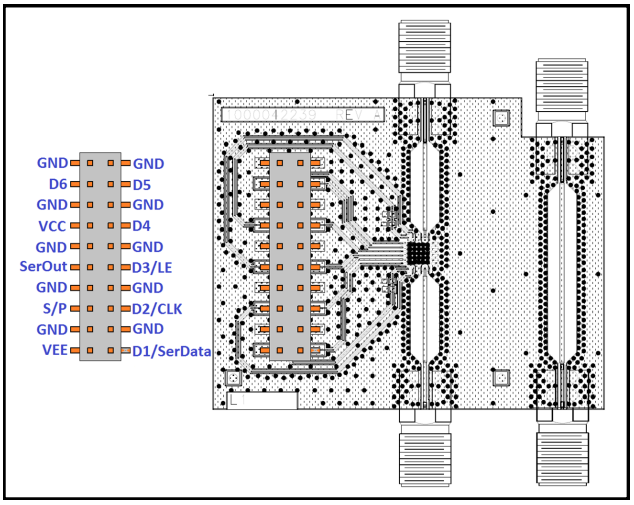
3. Maximum operating power is the maximum power where the specifications are guaranteed.
4. RMS is calculated across all 15 amplitude or phase states relative to the amplitude or phase in the 0° phase state at a given frequency.
5. This phase shifter is guaranteed to have monotonic phase shift.

## Absolute Maximum Ratings [6,7]

| Parameter | Absolute Maximum |
|---|---|
| Input Power 2.3 - 3.8 GHz | +27 dBm |
| $V_{CC}$ | -0.5V ≤ $V_{CC}$ ≤ +7.0V |
| $V_{EE}$ | -7.0V ≤ $V_{EE}$ ≤ +0.5V |
| D1-D4, P/S, LE, CLK or SER IN | -0.5V ≤ $V_{IN}$ ≤ VCC + 0.5V |
| SER OUT | -0.5V ≤ $V_{OUT}$ ≤ $V_{CC}$ + 0.5V |
| Operating Temperature | -40ºC to +85ºC |
| Storage Temperature | -65ºC to +150ºC |

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. M/A-COM Technology Solutions does not recommend sustained operation near these survivability limits.

## Sample Board Header Pin Labels




## Handling Procedures

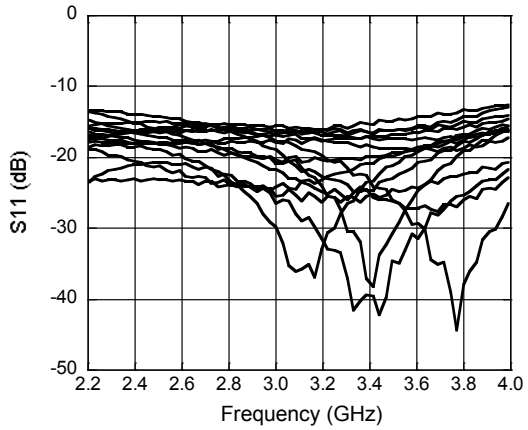
Please observe the following precautions to avoid damage:

## Static Sensitivity

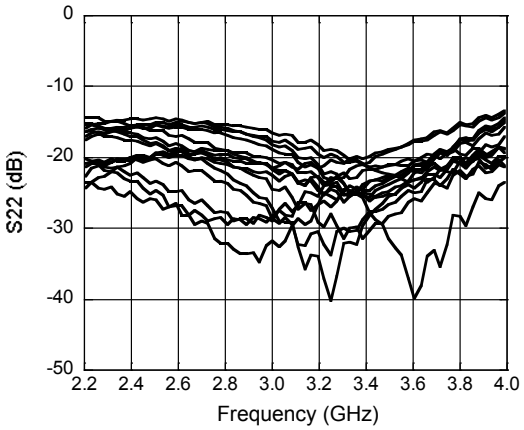
Gallium Arsenide and Silicon Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

## Typical Performance Curves

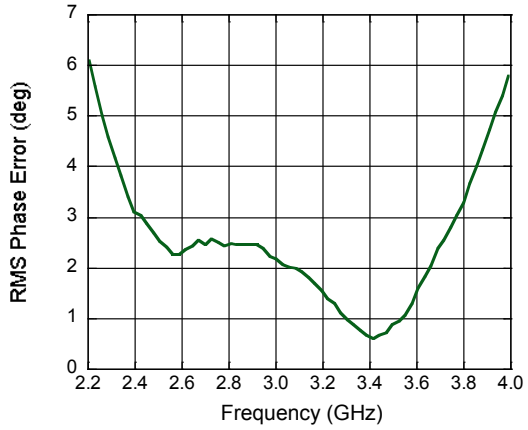
***$RF_{IN}$ Return Loss vs. Frequency (All States)***



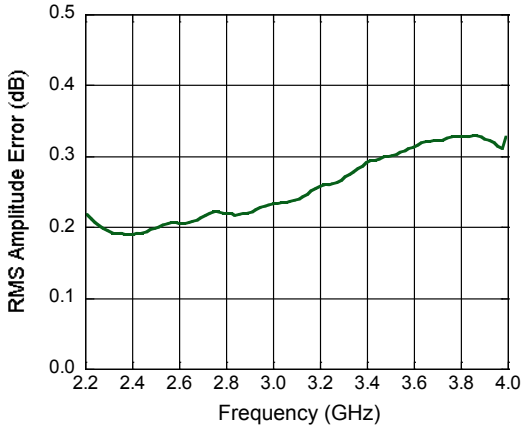

***$RF_{OUT}$ Return Loss vs. Frequency (All States)***



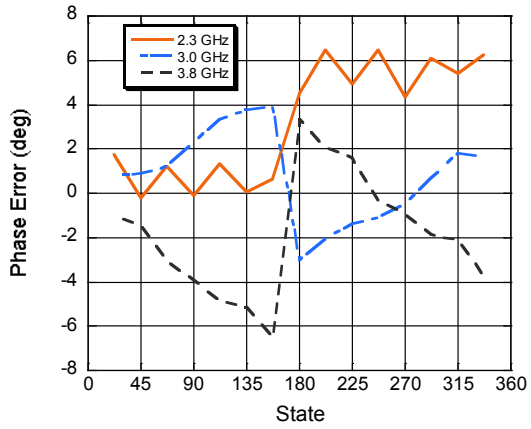

***Mean RMS Phase Error vs. Frequency***



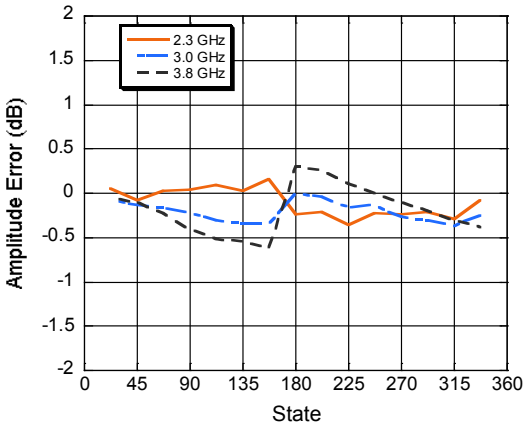

***Mean RMS Amplitude Error vs. Frequency***




***Phase Error (degrees) vs. State***

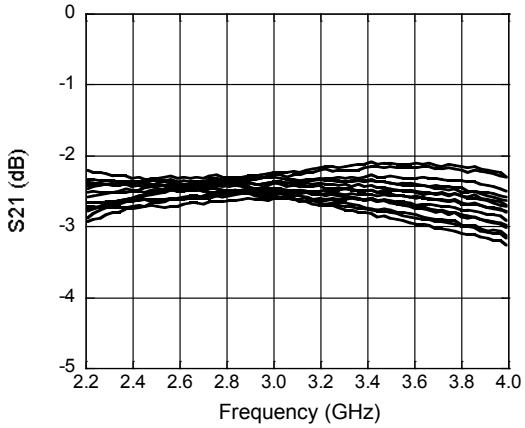



***Amplitude Error (dB) vs. State***

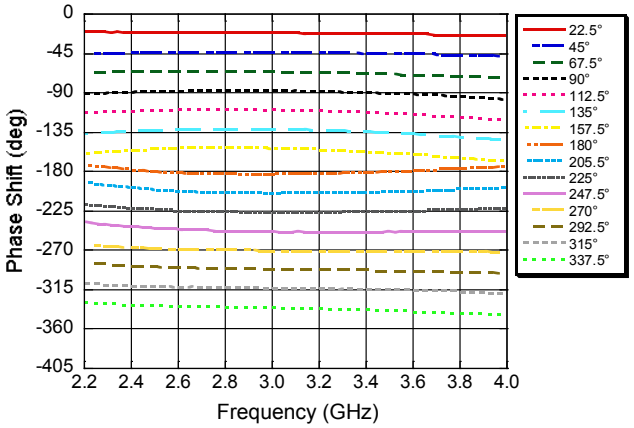


## Typical Performance Curves

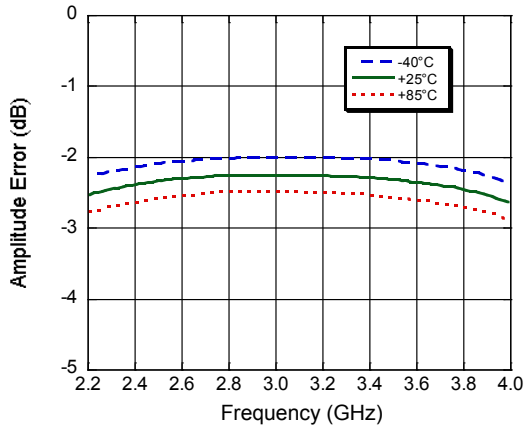
***Amplitude Variation vs. Phase State***




***Phase Shift vs. Frequency (All States)***




***Insertion Loss vs. Frequency (Reference State)***



## Modes of Operation: Serial and Direct Parallel

### *Serial Mode*

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with the MSB first. After shifting in the 6 bit word, a rising edge on LE will set the phase shifter to the desired state. While LE is high the CLK is masked to protect the data while implementing the change. SEROUT is SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled. When P/S is set high, Pins 22, 23, and 24 have the LE, CLK, and SER IN function.

In serial mode operation, the outputs will stay constant while LE is kept low.

### *Direct Parallel Mode*

The parallel mode is enabled when P/S is set low. In the direct parallel mode, the phase shifter is controlled by the parallel control inputs directly. When P/S is set low, Pins 22, 23, and 24 have the D3, D2, and D1 function.

### Mode Truth Table [8,9]

| P/S | LE | Mode |
|---|---|---|
| 1 | X | Serial |
| 0 | N/A | Direct Parallel |

8. There are two dummy bits (D1 & D2), that must be sent in the serial mode. This is because the 4 bit phase shifter uses the same driver as the 6 bit phase shifter.
9. In the parallel mode, D1 and D2 should be tied to ground or to $V_{CC}$.

### Truth Table (Digital Phase Shifter) [10]

| D6 | D5 | D4 | D3 | D2 | D1 | Phase Shift |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | X | X | Reference Phase |
| 0 | 0 | 0 | 1 | X | X | 22.5 deg |
| 0 | 0 | 1 | 0 | X | X | 45 deg |
| 0 | 1 | 0 | 0 | X | X | 90 deg |
| 1 | 0 | 0 | 0 | X | X | 180 deg |
| 1 | 1 | 1 | 1 | X | X | 337.5 deg |

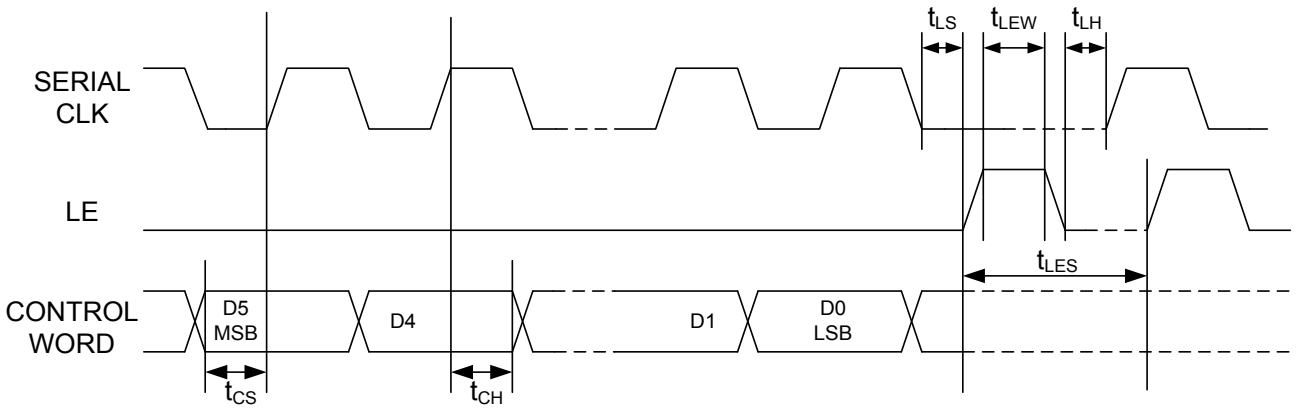
10. 0 = CMOS Low; 1 = CMOS High, X is CMOS Low or High

## Serial Interface Timing Characteristics

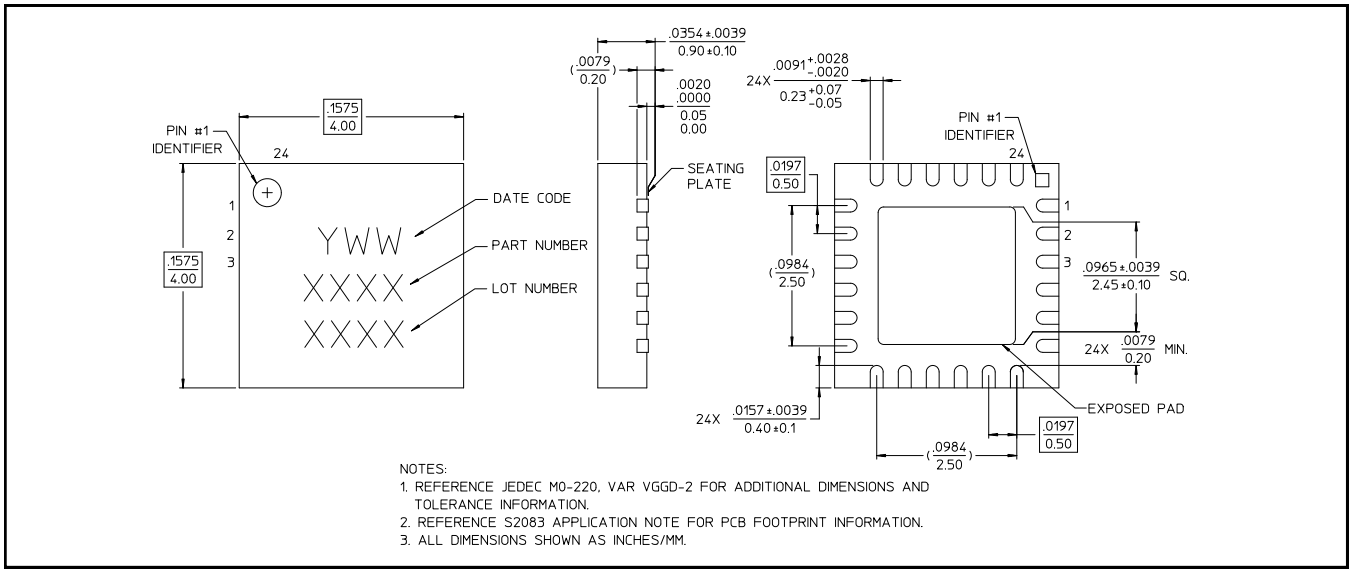
| Symbol | Parameter | Typical Performance | | | Units |
|---|---|---|---|---|---|
| | | -40°C | 25°C | +85°C | |
| $t_{SCK}$ | Min. Serial Clock Period | 100 | 100 | 100 | ns |
| $t_{CS}$ | Min. Control Set-up Time | 20 | 20 | 20 | ns |
| $t_{CH}$ | Min. Control Hold Time | 20 | 20 | 20 | ns |
| $t_{LS}$ | Min. LE Set-up Time | 10 | 10 | 10 | ns |
| $t_{LEW}$ | Min. LE Pulse Width | 10 | 10 | 10 | ns |
| $t_{LH}$ | Min. Serial Clock Hold Time from LE | 10 | 10 | 10 | ns |
| $t_{LES}$ | Min. LE Pulse Spacing | 630 | 630 | 630 | ns |

## Functionality
## Modes of Operation: Serial and Direct Parallel

### Serial Input Interface Timing Diagram




### *Lead Free 4* mm 24-Lead PQFN †




† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.