dsPIC33CH512MP508 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CH512MP508 family devices that you have received conform functionally to the current Device Data Sheet (DS70005371**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CH512MP508 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on Page 11, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CH512MP508 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision		
		A0	A1	A2
Devices with CAN FD				
dsPIC33CH256MP505	0x7D42	0x0000	0x0001	0x0002
dsPIC33CH512MP505	0x7D52			
dsPIC33CH256MP506	0x7D43			
dsPIC33CH512MP506	0x7D53			
dsPIC33CH256MP508	0x7D44			
dsPIC33CH512MP508	0x7D54			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID[1]	Revision ID for Silicon Revision		
		A0	A1	A2
Devices with No CAN FD				
dsPIC33CH256MP205	0x7D02	0x0000	0x0001	0x0002
dsPIC33CH512MP205	0x7D12			
dsPIC33CH256MP206	0x7D03			
dsPIC33CH512MP206	0x7D13			
dsPIC33CH256MP208	0x7D04			
dsPIC33CH512MP208	0x7D14			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions		
				A0	A1	A2
I^2C	Interrupt	1.	In Client mode, incorrect interrupt generated with DHEN = `1`.	X	X	X
I^2C	Error	2.	False bus collision error generated.	X	X	
I^2C	Idle	3.	SFRs are reset in Idle mode.	X	X	X
I^2C	SMBus 3.0	4.	When Configuration bit, SMBEN (FDEVOPT[10]) = `1`, the SMBus 3.0 V_{IH} minimum specification may not be met.	X		
Oscillator	HS, XT	5.	Removed.	—	—	—
UART	FERR	6.	The FERR bit will not get set if one Stop bit is received.	X	X	X
UART	OERR	7.	The 9th byte received will not be available to be read.	X	X	X
UART	TXWRE	8.	TXWRE bit (UxSTAH[7]) cannot be cleared once it gets set.	X	X	X
UART	Address Detect	9.	When writing to UxP1 with UTXBRK = `1`, content of P1 will not get transmitted.	X	X	X
UART	Address Detect	10.	In Address Detect mode, content of P1 is not transmitted on writing to P1 with UTXBRK = `1`.	X	X	X
UART	Sleep	11.	When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = `1`.	X	X	X
UART	Smart Card	12.	Wait time interrupt flag is set when the last character transmitted has the bit, LAST = `0`.	X	X	X
MBIST	MBISTDONE	13.	After executing a Reset, the MBISTDONE bit will always be set.	X	X	X
CPU	`FLIM` Instruction	14.	When the operands are of different signs, the `FLIM` instruction may not force the correct data limit.	X	X	X
CPU	`MAXAB`/`MINAB`/`MINZAB` Instructions	15.	When the operands are of different signs, the `MAXAB`, `MINAB` and `MINZAB` instructions may not output the correct value.	X	X	X
CPU	`DIV.SD` Instruction	16.	When using the signed 32-by-16-bit division instruction, `DIV.SD`, the Overflow bit is not getting set when an overflow occurs.	X	X	X
SCCP/MCCP	Clock Source	17.	Using FOSC as the clock source may cause synchronization issues.	X	X	X
I/O	POR	18.	Spike on I/O at POR.	X		
DMA	ADC Triggers	19.	DMA is triggered continuously from ADC.	X		
PWM	Time Base Capture	20.	PWM Capture Status (CAP) flag will not set again under certain conditions.	X	X	X
I^2C	I^2C	21.	All instances of I^2C may exhibit errors and should not be used.	X		
Oscillator	VCO and AVCO Dividers	22.	Main and auxiliary PLL external VCO dividers can fail to output clock signal.	X	X	
Main Secondary Interface (MSI)	DMA Transfer	23.	DMA transfer of mailbox data.	X	X	X
Secondary CPU	`REPEAT`	24.	`REPEAT` loops interrupted by nested interrupts on the Secondary core may corrupt data and traps.	X	X	X
UART	UART	25.	TXWRE bit is not cleared when transmitter is disabled.	X	X	X
Secondary CPU	PRAM ECC	26.	Secondary core CPU may read from unprogrammed PRAM location.	X	X	X
SCCP	Timer Interrupt	27.	In Capture mode, the CCP timer interrupt may not occur if the timer prescale is not 1:1.	X	X	

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: I^{2}C

In Client mode with DHEN = `1` (Data Hold Enable), if software sends a NACK, a Client interrupt is asserted at the 9th falling edge of the clock.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

2. Module: I^{2}C

In Client mode, a false bus collision event is generated when the bus collision is enabled (SBCDE = `1`) and a Stop bit is received.

Work around

None.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X				
Secondary	X	X				

3. Module: I^{2}C

In Client mode, the SFRs are reset when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = `1`).

Work around

None.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

4. Module: I^{2}C

When selecting SMBus 3.0 operation using Configuration bit, SMBEN (FDEVOPT[10]), the Voltage Input High (V_{IH}) of the SMBus 3.0 specification minimum may not be met.

Work around

None.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X					
Secondary	X					

5. Module: Oscillator

This errata is no longer applicable to any silicon revisions of this product. See **Section 2.5 "External Oscillator Pins"** in the current device data sheet (DS70005371**D**) for guidance on oscillator design to avoid start-up related issues.

6. Module: UART

When the UART is operating with STSEL[1:0] = `2` (two Stop bits sent, two checked at receive) and STPMD = `0`, the FERR bit will not get set if one Stop bit is received.

Work around

Use STPSEL = `3` instead of STSEL = `2`. When operating with STSEL = `3` mode, the UART will be configured to send two Stop bits, but check one at receive.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

7. Module: UART

When the receive buffer overflows, the 9th byte received will get lost and cannot be read.

Work around

Do not allow the OERR bit to get set by reading the received data byte on each byte reception.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

8. Module: UART

Once the TX Write Transmit Error Status bit (TXWRE, UxSTAH[7]) gets set, the TXWRE bit cannot be cleared by a single clear instruction.

Work around

Use multiple clear instructions in a loop until the TXWRE bit gets cleared.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

9. Module: UART

In UART Address Detect mode, writing to UxP1 with UTXBRK = 1 should cause a Break to be transmitted, followed by the content in P1x, but the content of P1x will not get transmitted.

Work around

After writing to P1x, wait for UTXBRK to get clear and then rewrite to P1x.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

10. Module: UART

In Address Detect mode, the content of P1x is not transmitted on writing to P1x with UTXBRK = 1.

Work around

Write P1x a second time after waiting for the Break transmission to start.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

11. Module: UART

When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.

Work around

Set the SPLEN bit in addition to WAKE before entering Sleep.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

12. Module: UART

In Smart Card T = 1 mode, the Wait time interrupt flag is set when the last character transmitted has the bit, LAST = 0.

Work around

Ignore WTC interrupt events on non-last bytes.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

13. Module: MBIST

After a Reset, the MBISTDONE status bit will be set regardless of a BIST test being executed. If a BIST is requested and executed, the MBISTDONE bit will set as expected.

Work around

None.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

14. Module: CPU

The `FLIM` instruction may incorrectly limit the data range when operating on signed operands of different sign values. If the operands are either all negative or all positive, the limit is correct.

Work around

None.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

15. Module: CPU

When operating on signed operands of different sign values, the output for `MAXAB`, `MINAB` and `MINZAB` instructions may be incorrect. If the operands are either all negative or all positive, the output is correct.

Work around

None.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

16. Module: CPU

When using the Signed 32-by-16-Bit Division instruction, `DIV.SD`, the Overflow bit may not always get set when an overflow occurs. This erratum only affects operations in which at least one of the following conditions is true:

- Dividend and divisor differ in sign,
- Dividend > 0x3FFFFFFF or
- Dividend < 0xC0000000

Work around

The application software must perform both the following actions to handle possible undetected overflow conditions:

a) The value of the dividend must always be constrained to be in the following range: 0xC0000000 ≤ Dividend ≤ 0x3FFFFFFF.

b) If the dividend and divisor differ in sign (e.g., dividend is negative and divisor is positive), then after executing the `DIV.SD` instruction or the compiler built-in function, `__builtin_divsd()`, inspect the sign of the resultant quotient. If the quotient is found to be a positive number, then treat it as an overflow condition.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

17. Module: SCCP/MCCP

When FOSC is selected as the clock source using the CLKSEL[2:0] bits (CCPxCON1L[10:8]), unexpected operation may occur. For proper SCCP/MCCP input clock synchronization, do not use FOSC as the CCP clock source.

Work around

Use any of the other available clock sources in CLKSEL[2:0].

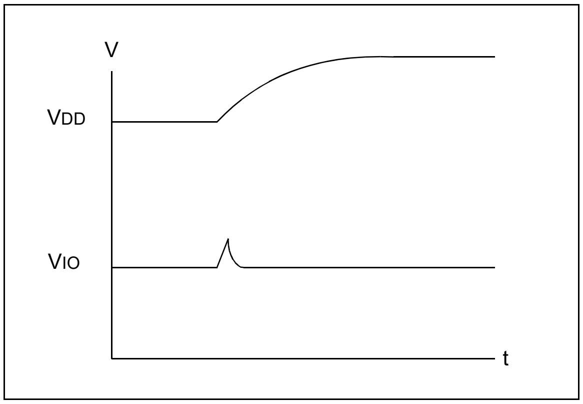
Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

18. Module: I/O

During a fast device power-up, when the VDD ramp is less than 4 mS, the I/O pins may drive up to 100 µA current for a duration of up to 10 µS (Figure 1-1).

FIGURE 1-1: I/O RAMP



Work around

1. Slow down the VDD ramp time (greater than 4 mS for VDD to ramp 0V to 3.3V).
2. Ensure the circuitry that is connected to the pins can endure this pulse.

   Example applications affected may include complementary power switches, where a transient current shoot-through might occur. High-voltage applications with complementary switches should power the high-voltage 200 µSec later than powering the dsPIC® device to avoid the current shoot-through. This behavior is specific to each device and not affected by aging.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X					
Secondary	X					

19. Module: DMA

The DMA receives multiple continuous triggers from the ADC until the trigger event from ADC is cleared. The OVRUNIF flag (DMAINTn[3]) will be set. When the OVRUNIF bit changes state, from '0' to '1', a DMA interrupt is generated.

Work around

Ignore the OVRUNIF bit and the first DMA interrupt. Clear the ADC trigger source, ANxRDY, with a DMA read of the ADC buffer, ADCBUFx, for the corresponding ADC channel.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X					
Secondary	X					

20. Module: PWM

When using a PWM Control Input (PCI) to trigger a time base capture, the Capture Status flag, CAP (PGxSTAT[5]), may not set again under certain conditions. When a subsequent PWM capture event occurs while, or just after, reading the current capture value from the PGxCAP register, the Capture Status Flag, CAP, will not set again.

Work around

Read the PWM Generator x Capture (PGxCAP) register as soon as possible to avoid the condition. Poll the CAP bit and read the PGxCAP value within the associated PWM Generator (1-8) interrupt or any of the six PWM Event (A-F) interrupts corresponding to the PCI event which triggered the time base capture.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

21. Module: I^{2}C

All instances of I^{2}C/SMBus may exhibit errors and should not be used. When operating I^{2}C/SMBus in a noisy environment, the I^{2}C module may exhibit various errors. These errors may include, but are not limited to, corrupted data, unintended interrupts or the I^{2}C bus getting hung up due to injected noise. Examples of system noise include, but are not limited to, PWM outputs or other pins toggled at high speed adjacent to the I^{2}C pins. Both Host and Client I^{2}C/SMBus modes may exhibit this issue.

Work around

If I^{2}C is required, use a software I^{2}C implementation. An example I^{2}C software library is available from Microchip:

www.microchip.com/dsPIC33C_I2C_SoftwareLibrary

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X					
Secondary	X					

22. Module: Oscillator

At PLL start-up, the main and auxiliary PLL VCO dividers may occasionally halt and not provide a clock output. The VCO and AVCO dividers can be selected as clock sources for different peripheral modules, including the ADC, PWM, DAC, CAN FD, UART, etc.

All VCO and AVCO divider outputs, FVCO/2, FVCO/3, FVCO/4, FVCODIV, AFVCO/2, AFVCO/3, AFVCO/4 and AFVCODIV, are affected and may show the issue independently.

Any type of Reset may recover the VCO/AVCO divider clock outputs (Software Reset, WDT, $\overline{\text{MCLR}}$ or POR).

Work around 1

Use another clock source, such as the FOSC, PLL or APLL output (FPLLO and AFPLLO), instead of the VCO or AVCO dividers.

Work around 2

If the application requires the VCO/AVCO divider, peripheral activity should be verified within some time or the device should be Reset.

The Watchdog Timer (WDT) or Timer1 may be used to establish the time-out period and reset the device. The following steps may be taken to implement this work around for any given peripheral and VCO/AVCO divider combination.

1) Set up the WDT or Timer1 time-out period.
2) Set up the VCO/AVCO divider source to be used by the peripheral.
3) Start the peripheral from this source.
4) Verify peripheral activity using an interrupt or other method and disable the time-out.
5) If the time-out expires, the device should be reset; WDT will reset the device without intervention, but Timer1 will require a SWR in the Timer1 Interrupt Service Routine.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X				
Secondary	X	X				

23. Module: Main Secondary Interface (MSI)

When transferring data between cores using the MSI mailbox with DMA, if the transmitting core is running more than two times the system clock frequency of the receiving core, the data transfer may not be processed correctly and the MSI may appear to be in a Freeze state.

An example of the application includes the DMA in the transmitting core may load data to the MSI Mailbox register after the receiving core initiates the MSI interrupt to Acknowledge data reception, but prior to hardware clear of the DTRDY bit, causing the hardware to appear to be frozen in the state where DTRDY is set in the transmitting core and cleared in the receiving core.

Work around

Do not use DMA for MSI data transfer when the core sending data will be operating at more than two times the system clock frequency of the core receiving data. Instead, in the MSI ISR, clear the DTRDY bit and load the next data to the MSI buffer/FIFO directly.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

24. Module: Secondary CPU

While the Secondary CPU core is executing the instruction targeted by a `REPEAT` loop and two or more nestable interrupts occur in near simultaneous proximity, data corruption may occur within the lowest priority Interrupt Service Routine (ISR) and/or original `REPEAT` loop code. Specifically, when the CPU is vectoring to the lower priority ISR and a higher priority stimulus forces the CPU to vector to a different ISR, hardware will retarget the background `REPEAT` loop onto the first instruction of the lower priority ISR. Typically, ISRs start with a stack `PUSH` instruction, resulting in repeated stack pushes later when the lower priority ISR executes. This manifests as an Address Error Trap upon return from the low-priority ISR as the CPU attempts to use the repeated stack push data as the ISR's return address.

If the first instruction of the lower priority ISR is repeatable without harmful effects, such as a `NOP`, data corruption will still be apparent in the background code as its `REPEAT` loop will prematurely terminate.

Work around 1

Avoid using `REPEAT` instructions in projects built for the Secondary core. For compiled code, use MPLAB® XC16, v1.61 or higher and specify `-merrata=repeat_gie` or `-merrata=repeat_nstdis` as an additional option for XC16 (Global Options). Alternatively, this option may be individually added to the command-lines invoking `xc16-gcc` and `xc16-ld`.

`-merrata=repeat_gie` will suppress generation of `REPEAT` loops unless required for a hardware divide instruction. For divides, the `REPEAT` loop will be prefixed with instructions to save INTCON2. Write GIE (INTCON2[15]) = `0` to globally disable all interrupts, then postfix with an instruction to restore INTCON2. Toolchain library calls, such as `memcpy()`/`printf()`, etc., will also link against implementations that avoid `REPEAT` loops and globally mask interrupts where needed for divide instructions.

`-merrata=repeat_nstdis` will also suppress `REPEAT` loops. However, for hardware divide loops, saving/restoring will be applied to INTCON1 and NSTDIS (INTCON1[15]) = `1` will be written to disable interrupt nesting while maintaining GIE unchanged. Toolchain libraries will continue to use GIE (INTCON2[15]) global interrupt masking instead of relying on NSTDIS (INTCON1[15]) to protect divide loops.

Note:	Blocking interrupt nesting typically adds no latency to interrupt processing, but increases worst-case interrupt latency for higher priority ISRs. A low-priority interrupt triggered immediately before a high-priority stimulus adds the entire execution time of the low-priority ISR to the worst-case response latency for the higher priority ISR.

Work around 2

Ensure that all `REPEAT` instructions only execute in a context where back-to-back interrupts of nestable priority are impossible, such as within IPL6 and IPL7 ISRs, or anywhere all enabled interrupts are known to be configured to the same priority level. Also, if the application implements periodic interrupts corresponding to internal/synchronously timed events, it may be possible to find or wait for an execution window where a `REPEAT` loop can deterministically complete without two nested interrupts able to clobber it. A `PWRSAV` call to enter Idle mode may help find synchronized, safe windows as code flow will halt, then resume in response to the next interrupt.

As compiled code can have `REPEAT` loops hidden within them, this work around should only be attempted on a per source file basis with Work around 1 applied for all other files that cannot be carefully controlled or which do not require `REPEAT` loops. It is additionally suggested that the full project disassembly listing be searched for `REPEAT` instructions and that proper interrupt masking, nest disabling or contextual state and timing conditions for safe `REPEAT` execution have been met.

Affected Silicon Revisions

Core	A0	A1	A2			
Main						
Secondary	X	X	X			

25. Module: UART

The TXWRE bit is not cleared when the UART transmitter is disabled.

Work around

To clear the TXWRE bit, the user can first flush the FIFO via writing TXBE = `1`, then the TXWRE bit can be cleared.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X	X			
Secondary	X	X	X			

26. Module: Secondary CPU

If MSTRPR[5] = `1` (DMA priority higher than the CPU) and an interrupt occurs, the Secondary CPU, "`cpu_pmem_addr`", may be corrupted with the DMA data before fetching the proper `RETFIE` return address. If the DMA data correspond to the address of an unprogrammed location in the PRAM, ECC single-bit and double-bit errors may be observed.

Work around

A routine called, "`_wipe_secondary(1);`", has been added in MPLAB® XC16, v1.70 or higher, and requires the MPLAB IDE device family pack dsPIC33CH-MP_DFP 1.6.183. This routine will load the PRAM with a known value and valid ECC contents. The Main core application should call this routine at least once each time the device is powered on and should do so before loading the PRAM with the Secondary core user application image.

The time needed to run the "`_wipe_secondary(1);`" routine is Main core execution speed-dependent, but will be similar to loading a full size image to a PRAM of a given size.

Affected Silicon Revisions

Core	A0	A1	A2			
Main						
Secondary	X	X	X			

27. Module: SCCP

In Capture mode, the CCPx timer interrupt, _CCTxInterrupt, may not occur if the Timer Prescale Value, TMRPS[1:0], is not configured for 1:1 operation.

Work around

If the _CCTxInterrupt is needed in Capture mode, maintain TMRPS[1:0] = `00` for 1:1 timer prescale.

Affected Silicon Revisions

Core	A0	A1	A2			
Main	X	X				
Secondary	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005371**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Characteristics

In Table 24-29, the FRC percentage is changed from -3 to +3, to -2 to +2. All changes are shown below in **bold**.

2. Module: Functional Safety and Qualification Support

Functional Safety

- Class B Safety Library – IEC 60730
- For ASIL B and Beyond Applications – ISO 26262
- FMEDA Computation Spreadsheet (evaluation of Random Hardware Failures Metric)
- Functional Safety Manual
- Functional Safety Diagnostics Suite

Qualification Support

- AEC-Q100 REV-H (Grade 0: -40°C to +150°C) Compliant

TABLE 24-29: INTERNAL FRC ACCURACY

Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min.	Max.	Units	Conditions
Internal FRC Accuracy @ FRC Frequency = 8 MHz[1]					
F20a	FRC	**-2**[2]	**+2**	%	-40°C ≤ TA ≤ **-5**°C
		-1.5	+1.5	%	**-5**°C ≤ TA ≤ +85°C
		-2	+2	%	+85°C ≤ TA ≤ +125°C
F22	BFRC	-17	+17	%	-40°C ≤ TA ≤ +125°C

Note 1: Frequency is calibrated at +25°C and 3.3V.

2: Due to the effect of aging, this value may drift by an additional -0.5% over lifetime of the device.

3. **Module: Guidelines for Getting Started with 16-Bit Digital Signal Controllers**

Additional information is added to **Section 2.5 "External Oscillator Pins"** and **Section 2.6 "External Oscillator Layout Guidance"** is added.

2.5 External Oscillator Pins

When the Primary Oscillator (POSC) circuit is used to connect a crystal oscillator, special care and consideration is needed to ensure proper operation. The POSC circuit should be tested across the environmental conditions that the end product is intended to be used. The load capacitors specified in the crystal oscillator data sheet can be used as a starting point, however, the parasitic capacitance from the PCB traces can affect the circuit and the values may need to be altered to ensure proper start-up and operation.

Excessive trace length and other physical interaction can lead to poor signal quality. Poorly tuned oscillator circuits can have reduced amplitude, incorrect frequency (runt pulses), distorted waveforms and long start-up times that may result in unpredictable application behavior, such as instruction misexecution, illegal op code fetch, etc. Ensure that the crystal oscillator circuit is at full amplitude and correct frequency before the system begins to execute code. In planning the application's routing and I/O assignments, ensure that adjacent port pins, and other signals in close proximity to the oscillator, do not have high frequencies, short rise and fall times and other similar noise. For further information on the Primary Oscillator, see Primary Oscillator (POSC).

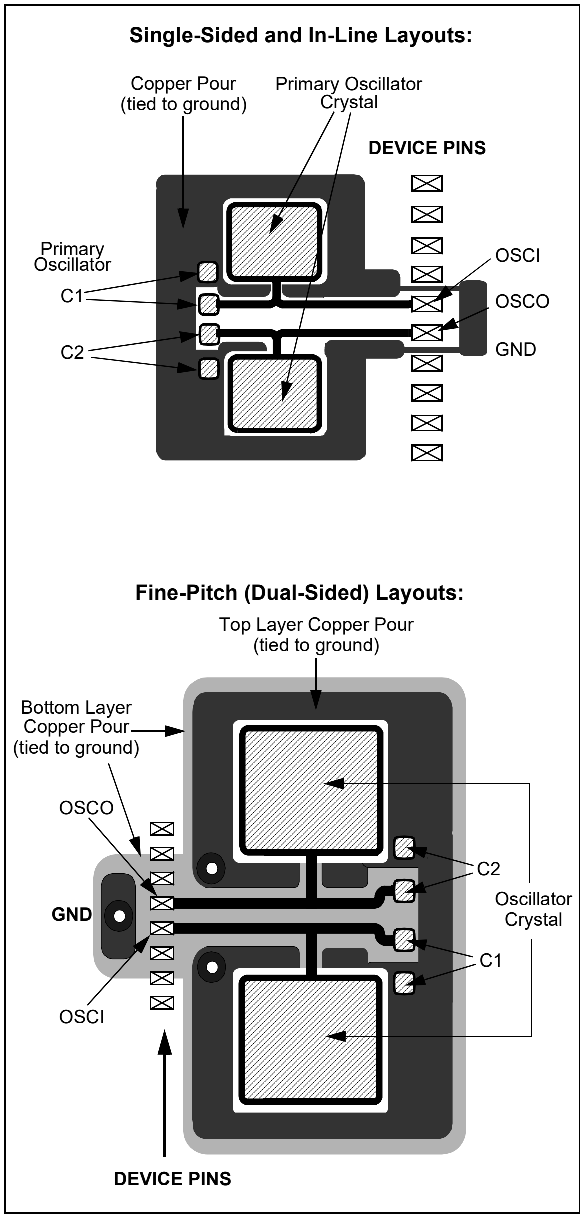
2.6 External Oscillator Layout Guidance

Use best practices during PCB layout to ensure robust start-up and operation. The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. If using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. Suggested layouts are shown in Figure 2-2. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the Microchip website (www.microchip.com):

- *AN943, "Practical PICmicro® Oscillator Analysis and Design"*
- *AN949, "Making Your Oscillator Work"*
- *AN1798, "Crystal Selection for Low-Power Secondary Oscillator*

FIGURE 2-2: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



4. Module: dsPIC® Core Naming Convention

When referring to the dsPIC cores implemented in a dual core device, all instances of “Master” and “Slave” have been replaced with “Main” and “Secondary”, respectively. This includes the Master Slave Interface (MSI) module which is now named the Main Secondary Interface (MSI) module.

5. Module: SPI

The following text in the first paragraph of the SPI section: “One of the SPI modules can work up to 50 MHz speed when selected as a non-PPS pin. For the Master core, it will be SPI2 and for the Slave core, it will be SPI1.”

has been changed to:

“On 48, 64 and 80-pin devices, one of the SPI modules can operate at higher speeds when selected as a non-PPS pin. For the Main core, it will be SPI2 and for the Secondary core, it will be SPI1.”

6. Module: Oscillator

Table 6-3 has been updated as shown below in **bold**.

TABLE 6-3: OSCO FUNCTION FOR THE **MAIN** AND **SECONDARY** CORE(1)

[OSCIOFNC:S1OSCIOFNC]	RB1 or OSCO pin function
1:1	**Main** clock output on OSCO pin
1:0	**Main** clock output on OSCO pin
0:1	**Secondary** clock output on OSCO pin
0:0	Clock out disabled, RB1 works as an I/O port; output function is based on pin ownership (CPRB1 = `1` or `0`)

Note 1: The RB1 pin will toggle during programming or debugging time, irrespective of the OSCIOFNC or S1OSCIOFNC settings.

7. Module: Electrical Characteristics

AD60, AD61 and AD62 have been added to Table 24-43, as shown below in **bold**.

TABLE 24-43: ADC MODULE SPECIFICATIONS

Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	AVSS	—	AVDD	V	
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	100	—	Ω	For minimum sampling time (Note 1)
AD60	**CHOLD**	**Sample-and-Hold Capacitance**	**—**	**5**	**—**	**pF**	**Dedicated cores**
AD61	**CHOLD**	**Sample-and-Hold Capacitance**	**—**	**15**	**—**	**pF**	**Shared core**
AD62	**RIC**	**Internal Interconnection Resistance**	**—**	**—**	**1000**	**Ω**	
AD66	VBG	Internal Voltage Reference Source	1.14	1.2	1.26	V	

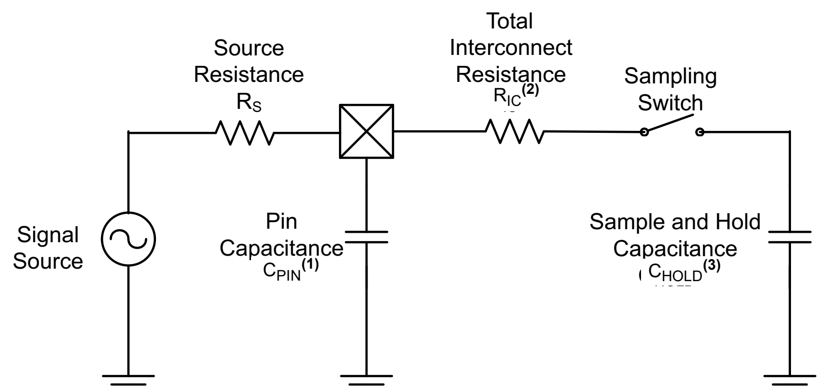
8. Module: ADC

The following **Sampling Time Requirements** section has been added to both **Section 3.16 "High-Speed, 12-Bit Analog-to-Digital Converter (Main Core ADC)"** and **Section 4.7 "High-Speed, 12-Bit Analog-to-Digital Converter (Secondary Core ADC)"**.

Sampling Time Requirements

The analog input model of the ADC is shown in the figure below.

FIGURE: ADC ANALOG INPUT MODEL



Note 1: The CPIN value depends on the device package and is not tested. The effect of the CPIN is negligible if $R_S \le 5\ k\Omega$.

2: See the AD62 parameter in Table 24-43.

3: See the AD60 and AD61 parameters in Table 24-43.

The total acquisition time for the Analog-to-Digital conversion is a function of the Holding Capacitor (CHOLD) charge time. For the ADC module to meet its specified accuracy, the Holding Capacitor (CHOLD) must be allowed to fully charge to the voltage level on the analog input pin. The Signal Source Impedance (RS) and the Interconnect Impedance (RIC) combine to affect the time required to charge the CHOLD. The total resistance (RS + RIC) must therefore, be small enough to fully charge the Holding Capacitor within the selected sample time.

9. Module: DAC

The following changes have been made in Table 3-31 and Table 4-27 as shown below in **bold**.

TABLE 3-31: **MAIN CORE** REMAPPABLE PIN INPUTS

RPINRx[15:8] or RPINRx[7:0]	Function	Available on Ports
168	**DAC1 pwm_req_on**	**Internal**
169	**DAC1 pwm_req_off**	**Internal**

TABLE 4-27: **SECONDARY CORE** REMAPPABLE PIN INPUTS

RPINRx[15:8] or RPINRx[7:0]	Function	Available on Ports
162	**DAC3 pwm_req_on**	**Internal**
163	**DAC3 pwm_req_off**	**Internal**
164	**DAC2 pwm_req_on**	**Internal**
165	**DAC2 pwm_req_off**	**Internal**
166	**DAC1 pwm_req_on**	**Internal**
167	**DAC1 pwm_req_off**	**Internal**

10. Module: PTG

The following changes have been made in Table 3-46 as shown below in **bold**.

TABLE 3-46: PTG INPUT DESCRIPTIONS

PTG Input Number	PTG Input Description
PTG Trigger Input 0	**Trigger Input from Main Core PWM1 ADC Trigger 2**
PTG Trigger Input 1	**Trigger Input from Main Core PWM2 ADC Trigger 2**
PTG Trigger Input 2	**Trigger Input from Main Core PWM3 ADC Trigger 2**
PTG Trigger Input 3	**Trigger Input from Main Core PWM4 ADC Trigger 2**
PTG Trigger Input 4	**Trigger Input from Secondary Core PWM1 ADC Trigger 2**
PTG Trigger Input 5	**Trigger Input from Secondary Core PWM2 ADC Trigger 2**
PTG Trigger Input 6	**Trigger Input from Secondary Core PWM3 ADC Trigger 2**

11. Module: PPS

The following changes have been made to Table 4-27 as shown below in **bold**.

TABLE 4-27: **SECONDARY CORE** REMAPPABLE PIN INPUTS

RPINRx[15:8] or RPINRx[7:0]	Function	Available on Ports
170	S1RP170	**Main RPV0**
171	S1RP171	**Main RPV1**
172	S1RP172	**Main RPV2**
173	S1RP173	**Main RPV3**
174	S1RP174	**Main RPV4**
175	S1RP175	**Main RPV5**
176	S1RP176	**Secondary RPV0**
177	S1RP177	**Secondary RPV1**
178	S1RP178	**Secondary RPV2**
179	S1RP179	**Secondary RPV3**
180	S1RP180	**Secondary RPV4**
181	S1RP181	**Secondary RPV5**

12. Module: Electrical Characteristics

Table 24-34 has been updated as shown below. The maximum data rate column has been deleted, and references to tables and figures have been included to provide more detailed information.

TABLE 24-34: SPIx MAXIMUM DATA/CLOCK RATE SUMMARY

SPI Host Transmit Only (Half-Duplex)	SPI Host Transmit/ Receive (Full-Duplex)	SPI Client Transmit/Receive (Full-Duplex)	CKE
Figure 24-7 Table24-35	—	—	0
Figure 24-8 Table 24-35	—	—	1
—	Figure 24-9 Table 24-36	—	0
—	Figure 24-10 Table 24-37	—	1
—	—	Figure 24-12 Table 24-39	0
—	—	Figure 24-13 Table 24-38	1

13. Module: Main Core Memory Organization

Equation 3-1 has been removed from **Section 3.4.7 "BIST at Start-up"** and the text has changed to the following:

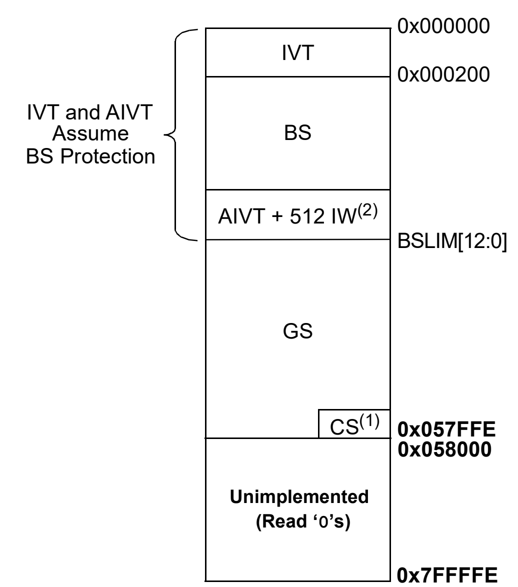
The BIST can be configured to automatically run on a POR-type Reset, as shown in Figure 4-10. By default, when BISTDIS (FPOR[6]) = `1`, the BIST is disabled and will not be part of device start-up. If the BISTDIS bit is cleared during device programming, the BIST will run after all Configuration registers have been loaded and before code execution begins. BIST will always run on FRC+PLL with PLL settings resulting in a 125 MHz clock rate.

Run-time BIST uses the same 125 MHz clock rate.

14. Module: Special Features

Figure 21-4 has been updated as shown in **bold** below.

FIGURE 21-4: FLASH SECURITY SEGMENTS (SINGLE PARTITION MODE)



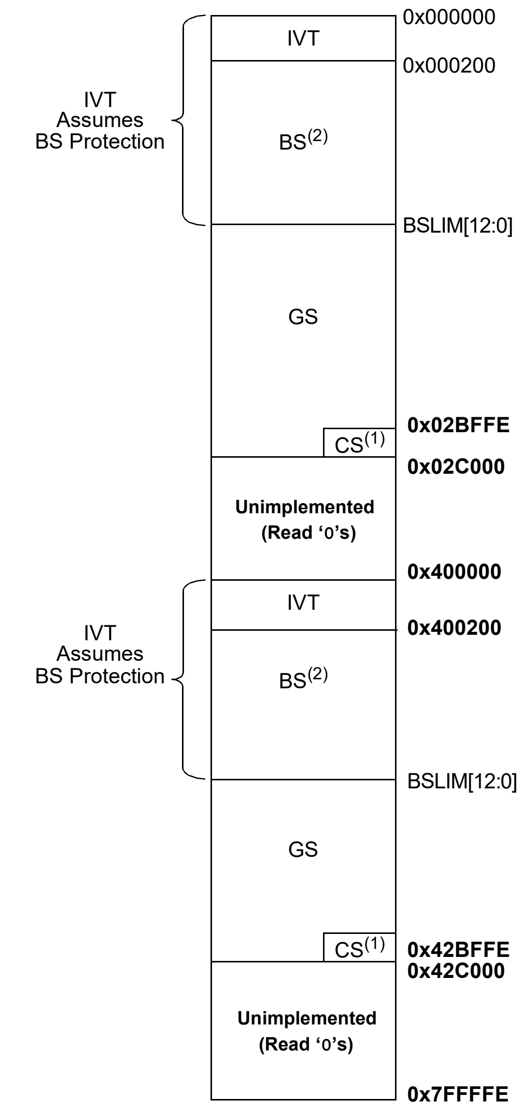
Note 1: If CS is write-protected, the last page (GS + CS) of program memory will be protected from an erase condition.

2: The last half (256 IW) of the last page of BS is unusable program memory.

15. Module: Special Features

Figure 21-5 has been updated as shown in **bold** below.

FIGURE 21-5: FLASH SECURITY SEGMENTS (DUAL PARTITION MODE)



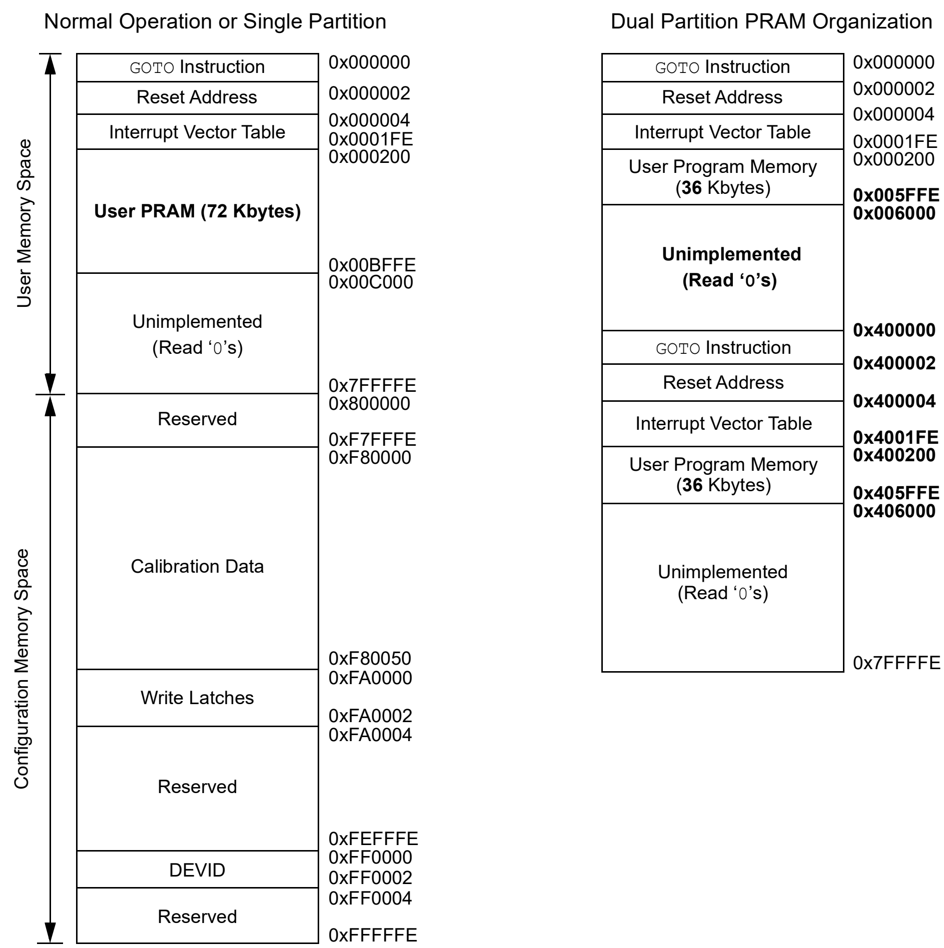
Note 1: If CS is write-protected, the last page (GS + CS) of program memory will be protected from an erase condition.

2: The last half (512 IW) of the last page of BS is unusable program memory.

16. Module: Secondary Core Memory Organization

Figure 4-3 has been updated as shown in **bold** below.

FIGURE 4-3: PRAM (PROGRAM MEMORY) FOR SECONDARY CORE dsPIC33CH512MP508S1 DEVICES



Note: Memory areas are not shown to scale.

17. Module: Electrical Characteristics

In Table 24-18, Parameters DI10 and DI20 are updated to include SMBus 3.0 V_{IL} and V_{IH} levels.

All changes are shown below in bold.

TABLE 24-18: I/O PIN INPUT SPECIFICATIONS

Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	Symbol	Characteristic	Min.	Typ.[1]	Max.	Units	Conditions
DI10	V_{IL}	Input Low Voltage					
		Any I/O Pin and $\overline{\text{MCLR}}$	Vss	—	0.2 VDD	V	
		I/O Pins with SDAx, SCLx	Vss	—	0.3 VDD	V	SMBus disabled
		I/O Pins with SDAx, SCLx	Vss	—	0.8	V	SMBus enabled
		I/O Pins with SDAx, SCLx	**Vss**	**—**	**0.8**	**V**	**SMBus 3.0 enabled**
DI20	V_{IH}	Input High Voltage					
		I/O Pins Not 5V Tolerant[3]	0.8 VDD	—	VDD	V	
		5V Tolerant I/O Pins and $\overline{\text{MCLR}}$[3]	0.8 VDD	—	5.5	V	
		5V Tolerant I/O Pins with SDAx, SCLx[3]	0.8 VDD	—	5.5	V	SMBus disabled
		5V Tolerant I/O Pins with SDAx, SCLx[3]	2.1	—	5.5	V	SMBus enabled
		5V Tolerant I/O Pins with SDAx, SCLx[3]	**1.35**	**—**	**VDD**	**V**	**SMBus 3.0 enabled**
		I/O Pins with SDAx, SCLx Not 5V Tolerant[3]	0.8 VDD	—	VDD	V	SMBus disabled
		I/O Pins with SDAx, SCLx Not 5V Tolerant[3]	2.1	—	VDD	V	SMBus enabled
		I/O Pins with SDAx, SCLx Not 5V Tolerant[3]	**1.35**	**—**	**VDD**	**V**	**SMBus 3.0 enabled**

Note 1: Data in "Typ." column are at 3.3V, +25°C unless otherwise stated.
2: Negative current is defined as current sourced by the pin.
3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
4: All parameters are characterized but not tested during manufacturing.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2018)

Initial version of this document; issued for revision A0.

Rev B Document (7/2019)

Removes original silicon errata issues 6 (PWM) and 18 (CPU). The issues are no longer relevant and were removed.

Updates silicon errata issue 18 (I/O)

Adds silicon errata issues 19 (DMA) and 20 (PWM).

Rev C Document (9/2019)

Updates device data sheet reference to the current revision D.

Rev D Document (2/2020)

Adds silicon issue 21 (I^2C).

Rev E Document (6/2020)

Adds silicon issues 22 (Oscillator) and 23 (Main Secondary Interface (MSI)).

Adds data sheet clarification 1 (Electrical Characteristics).

Removes silicon issue 5 (Oscillator) since it is no longer applicable.

Rev F Document (7/2020)

Adds silicon revision A1.

Updates the wording in silicon issue 21 (I^2C).

Adds data sheet clarification 2 (Functional Safety and Qualification Support) and 3 (Guidelines for Getting Started with 16-Bit Digital Signal Controllers).

Rev G Document (10/2020)

Updates silicon issue 22 (Oscillator).

Adds silicon issue 24 (Secondary CPU).

Updates data sheet clarification 2 (Functional Safety and Qualification Support).

Adds data sheet clarification 4 (dsPIC® Core Naming Convention).

Rev H Document (12/2020)

Adds silicon issue 25 (UART) and 26 (Secondary CPU).

Adds data sheet clarifications 5 (SPI), 6 (Oscillator), 7 (Electrical Characteristics), 8 (ADC), 9 (DAC), 10 (PTG), 11 (PPS), 12 (Electrical Characteristics), 13 (Main Core Memory Organization), 14 (Special Features), 15 (Special Features) and 16 (Secondary Core Memory Organization).

Rev J Document (4/2021)

Updates silicon issue 26 (Secondary CPU).

Adds silicon issue 27 (SCCP).

Adds data sheet clarification 17 (Electrical Characteristics).

Rev K Document (7/2021)

Adds silicon revision A2.

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