Revision 1.1.0
PCN Issue Date: 11/8/2022

PROCESS CHANGE NOTIFICATION
PCN2227

Minor Substrate Change for Selected Intel® Stratix® 10 Devices

This is not a new PCN issuance. This is a revision of the previously PCN2227 release. See Revision History (last page) for details.

Change Description:

Intel® is announcing a minor change to the substrate routing related to the unconnected Advanced Interface Bus (AIB) for selected Intel Stratix® 10 devices. The rest of the Bill of Materials (BOM) remains the same.

Products Affected:

Product Family	Pin Count
Selected Intel® Stratix 10 SX	F1760
Selected Intel® Stratix 10 GX	F1760

The list of affected part numbers (OPNs) can be downloaded in Excel form:
https://cdrdv2.intel.com/v1/dl/getContent/751575

Recommended Action

Customers are requested to:

1. Acknowledge receipt of this notification.
2. Review and inform us, at the earliest convenience, of any questions or concerns regarding this change.

Please refer to the "Product Transition Dates" for the key milestones.

Upon implementation, Intel will ship either pre-change or post-change materials.

Product Transition Dates:

Customers are requested to take note of the key dates shown in the table below.

Table 3: Key Dates

Milestone	*Date*
Last date to acknowledge receipt of this notification[1]	Nov 30, 2022
Earliest change implementation	Jan 30, 2023

Note 1: J-STD-046, section 3.2.3.1b, stipulates that lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change.

Reason for Change:

Continuous improvement on production test coverage of unconnected Advanced Interface Bus (AIB).

Impact and Benefit of Change:

There is no impact to form, fit, and function. The products will meet existing electrical and mechanical specifications.

Qualification Testing

Package design review data indicated no significant impact to performance and reliability. Electrical verification tests were successfully completed to evaluate effectiveness of the change. ESD Charge Device Model test was also performed to ensure no impact to the ESD CDM threshold. (See Table 4)

Table 4: ESD CDM Results

Test	Conditions	# of Lots/#of units	Result
ESD Charged Device Model (CDM)	+/- 250V	3 Lots/9 units	0 failures/Pass
	+/-350V	3 Lots/3 units	

Contact

For more information, please contact Sales in your region, or submit a Service Request at the My Intel support page.

Customer Notifications Subscription

If you would like to receive customer notifications by email, please follow the instructions in ADV 2209

Intel references J-STD-046 guidelines for PCN.
In accordance with J-STD-046, this change is deemed acceptable to the customer if no acknowledgement is received within 30 days from date of notification.

Revision History

Date	Rev	Description
10/28/2022	1.0.0	Initial Release
11/08/2022	1.1.0	Updated product family description table in page 1. No change in actual parts list.