

8 7 6 5 4 3 2 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

D

D

C


C

B

B

A

A

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	HW TYPE : Customer Evaluation Product(s) : AD9683-250EBZ : AD6677		
	DESIGN VIEW -	DRAWING NO. 02_040310	REV B
	PTD ENGINEER J. HARRIS	SIZE D	SCALE 1:1

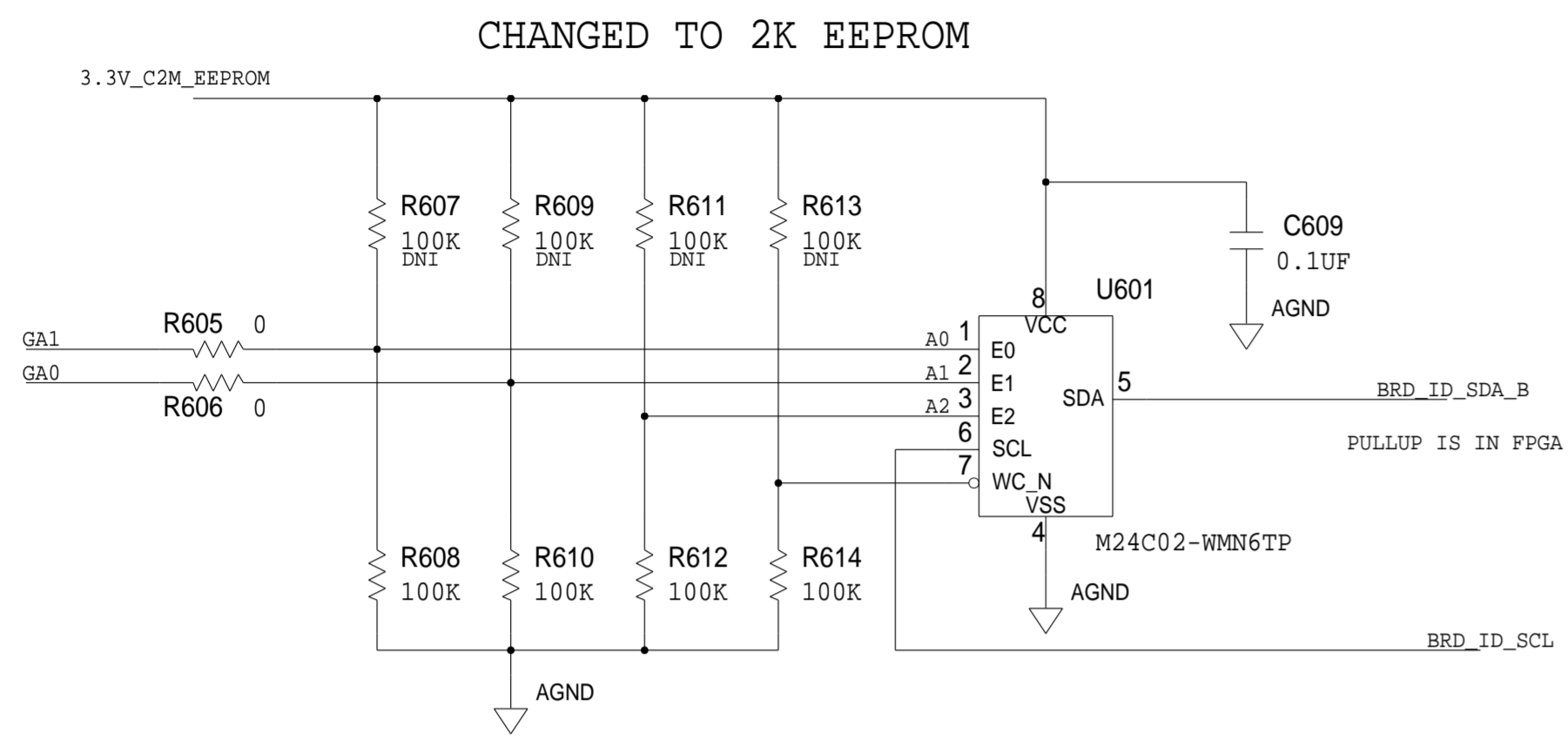
SHEET 1 OF 7

8 7 6 5 4 3 2 1



AD9683 / AD6677 EVAL / APPS BOARD

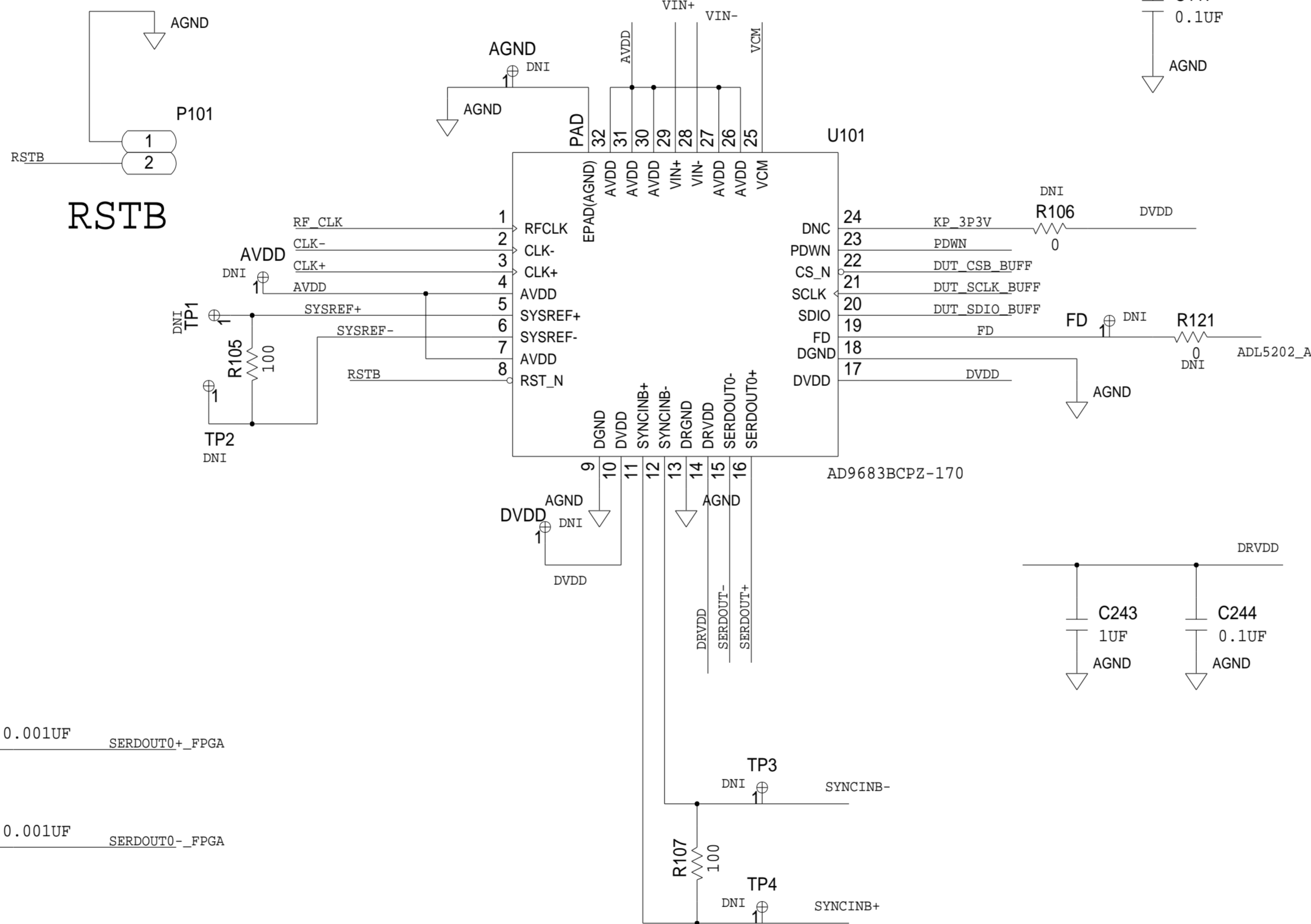
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



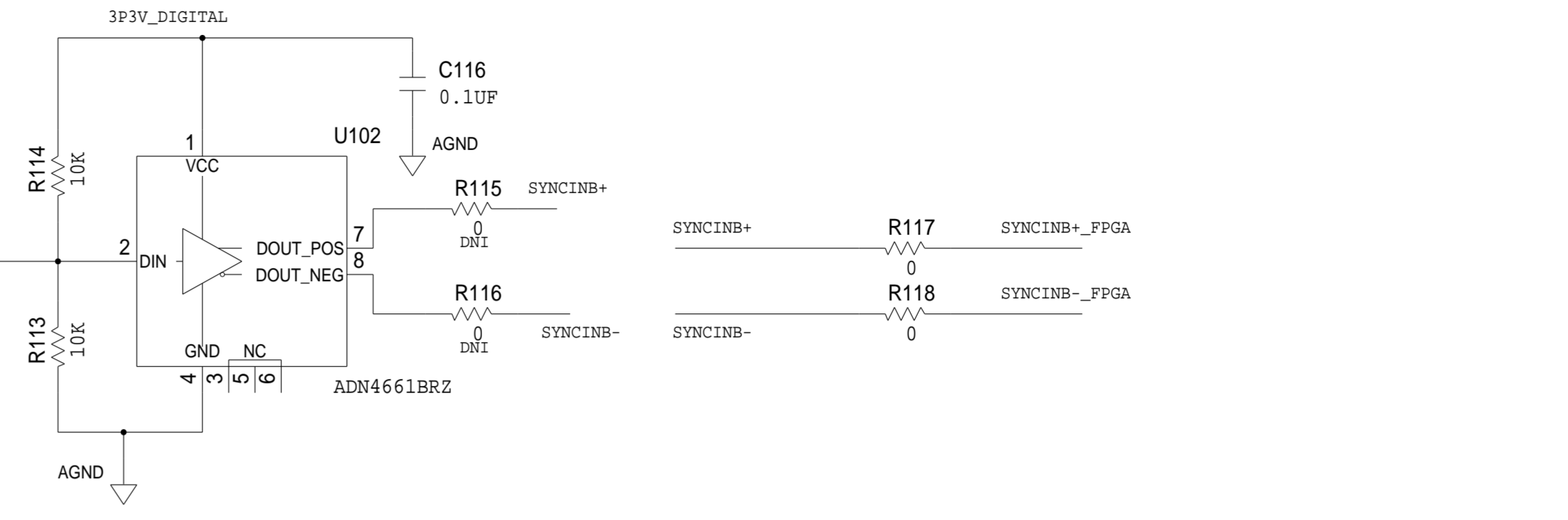
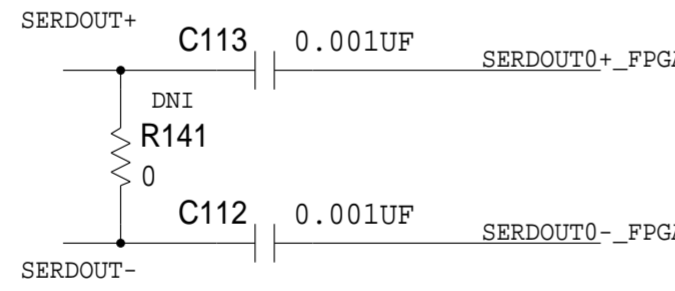
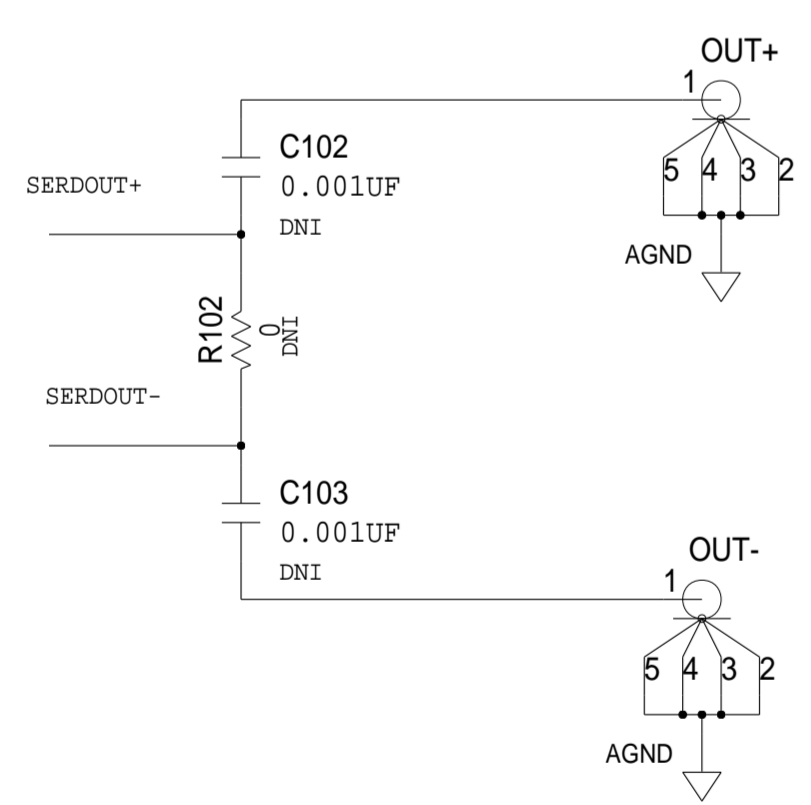
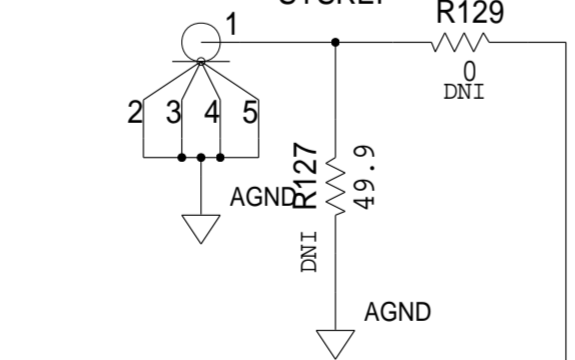
EEPROM - BOARD ID

DUT

THE FOOTPRINT FOR THIS SOCKED NEEDS TO BE CHECKED AGAINST THE DRAWING

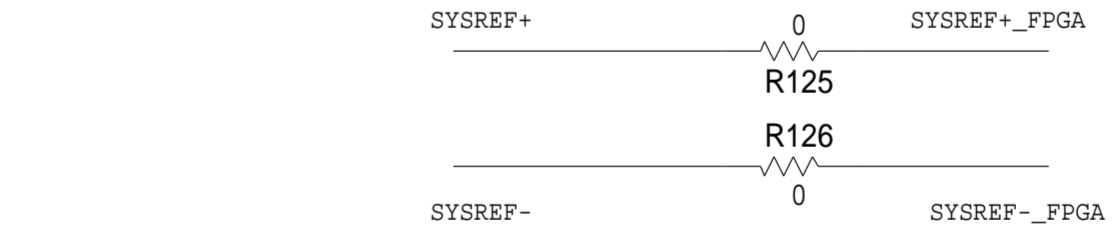
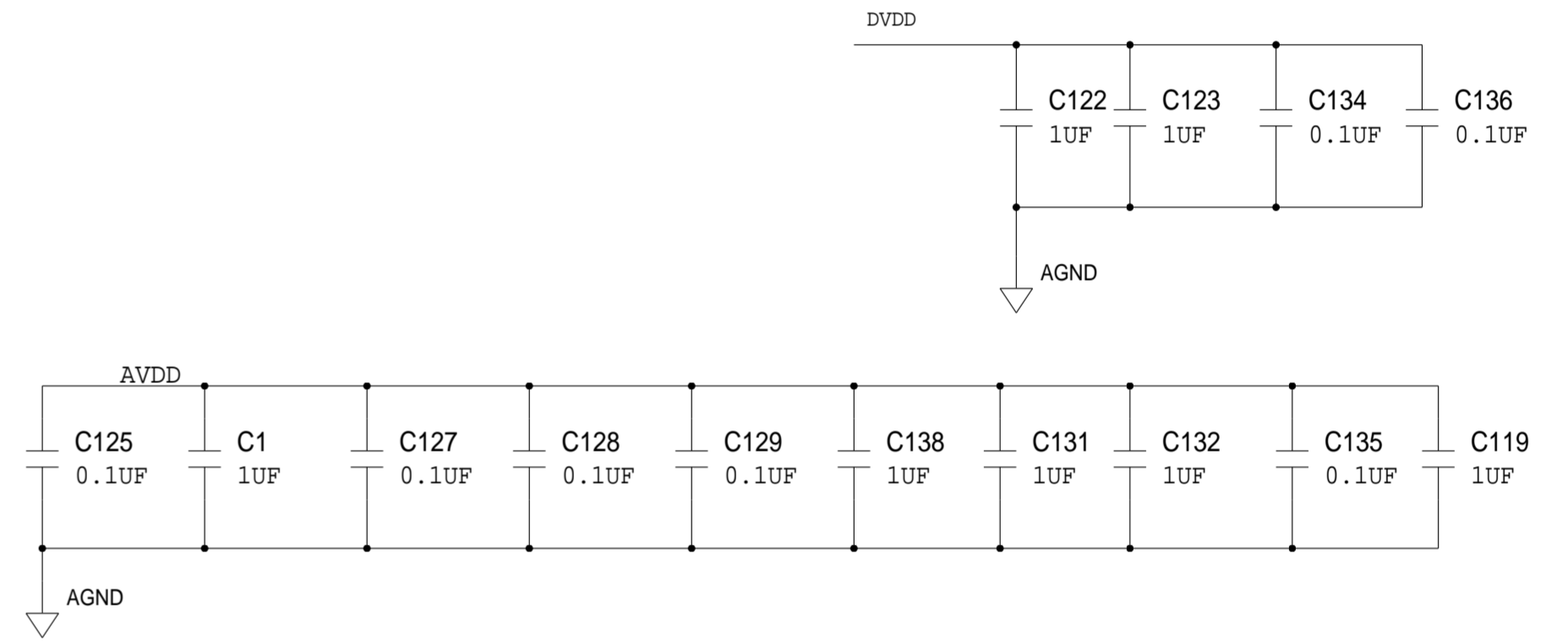
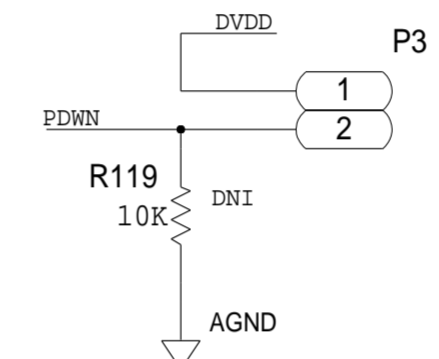


SYSREF SE TO DE



LAYOUT: DECOUPLING QUANTITY MAY VARY LAYOUT DEPENDING

PDWN

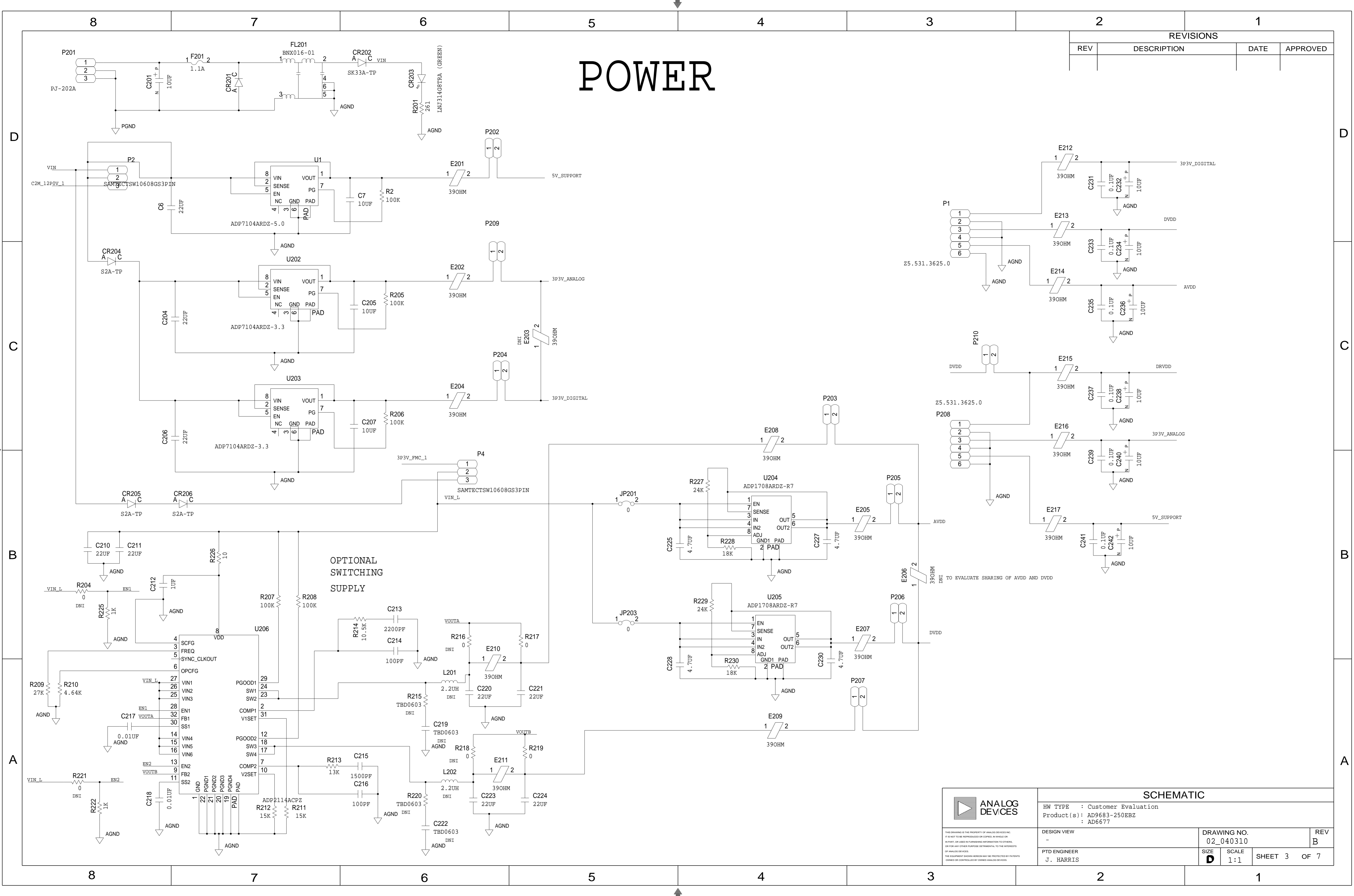


ANALOG DEVICES		SCHEMATIC		
HW TYPE : Customer Evaluation Product(s) : AD9683-250EBZ : AD6677		DESIGN VIEW	DRAWING NO.	REV
J. HARRIS		-	02_040310	B
SIZE	SCALE	SHEET 2 OF 7		
D	1:1			

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POWER

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



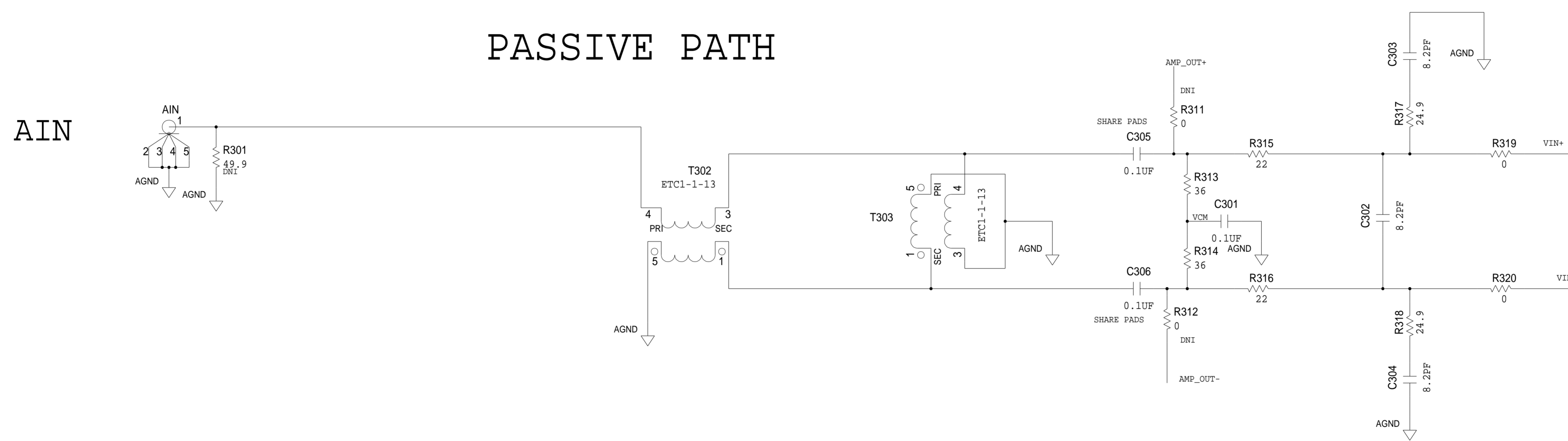
OPTIONAL SWITCHING SUPPLY

SCHEMATIC			
		HW TYPE : Customer Evaluation Product(s) : AD9683-250EBZ : AD6677	
DESIGN VIEW	-	DRAWING NO.	02_040310
PTD ENGINEER	J. HARRIS	SIZE	D
		SCALE	1:1
		SHEET	3 OF 7
		REV	B

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANALOG INPUT

PASSIVE PATH

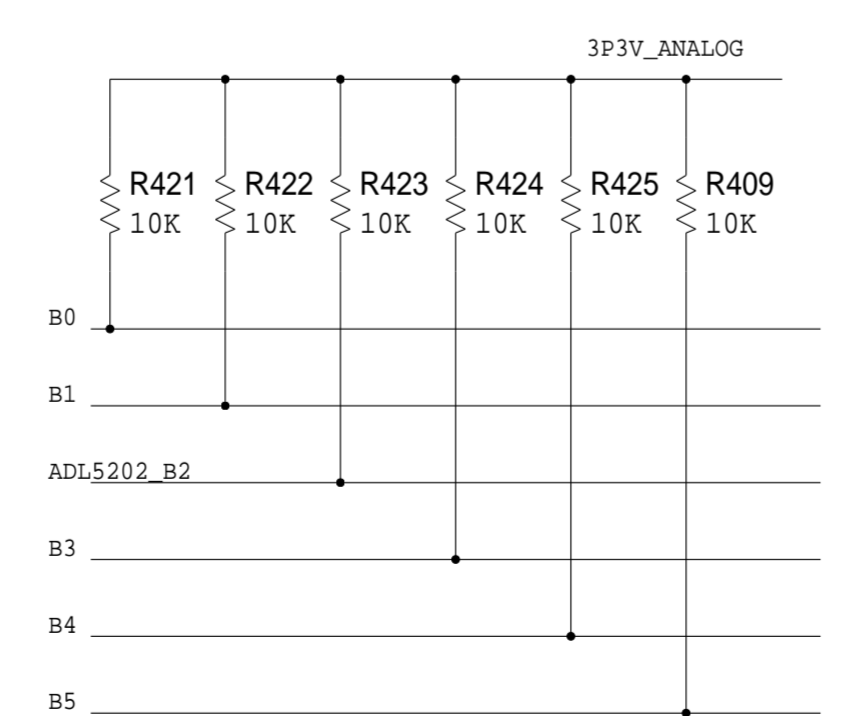
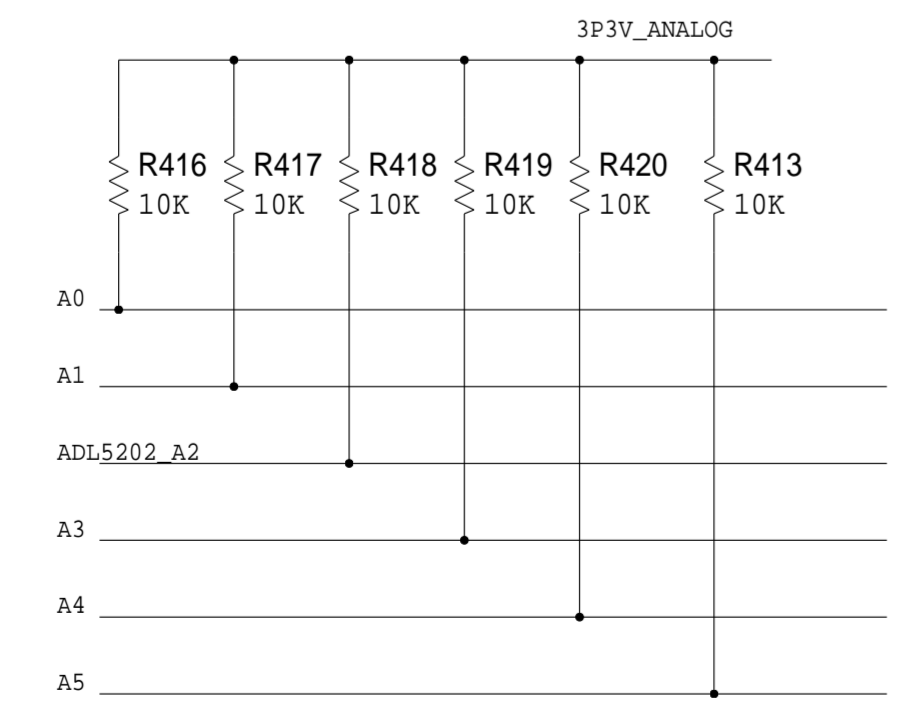
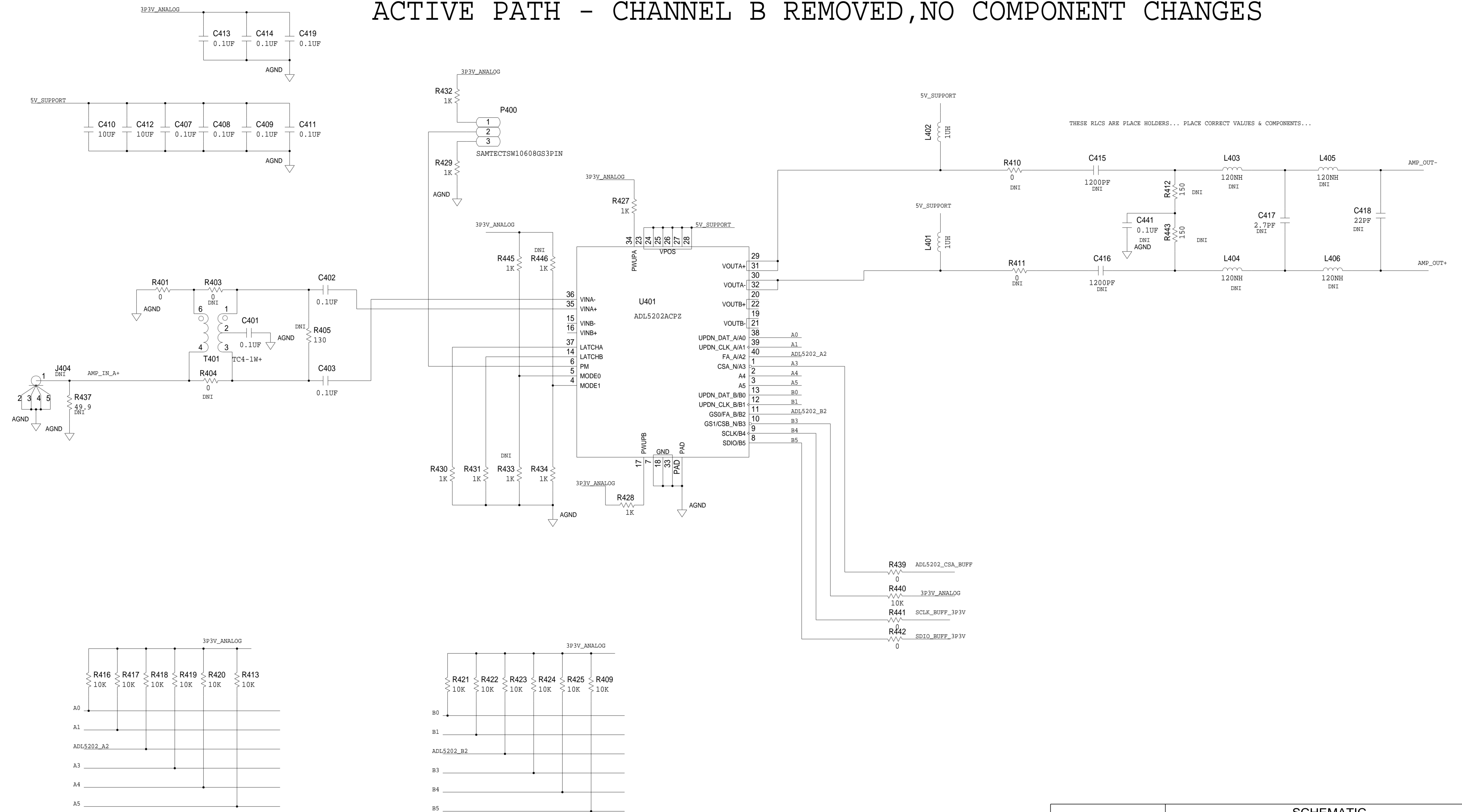


	SCHEMATIC		
	HW TYPE : Customer Evaluation Product(s) : AD9683-250EBZ : AD6677		
	DESIGN VIEW -	DRAWING NO. 02_040310	REV B
PTD ENGINEER J. HARRIS	SIZE D	SCALE 1:1	SHEET 4 OF 7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ACTIVE PATH - CHANNEL B REMOVED, NO COMPONENT CHANGES

THESE RLCS ARE PLACE HOLDERS... PLACE CORRECT VALUES & COMPONENTS...

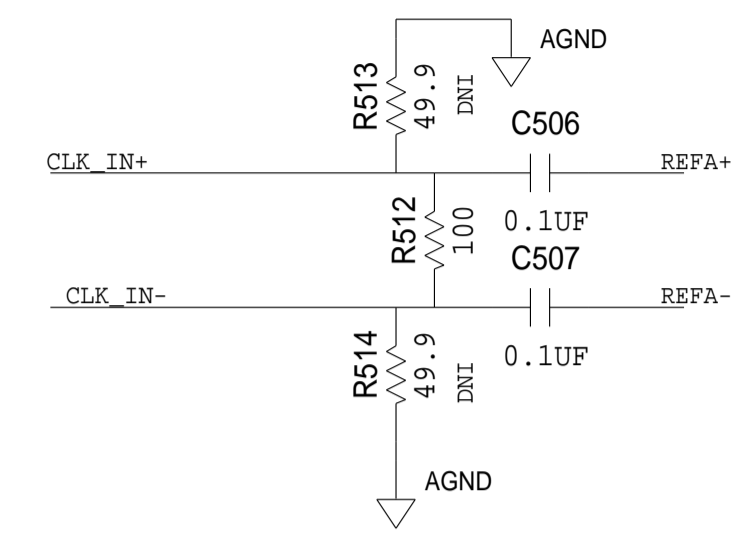


	SCHEMATIC		
	HW TYPE : Customer Evaluation Product(s) : AD9683-250EBZ : AD6677		
DESIGN VIEW	-	DRAWING NO.	REV
PTD ENGINEER	J. HARRIS	02_040310	B
SIZE	D	SCALE	1:1
		SHEET	5 OF 7

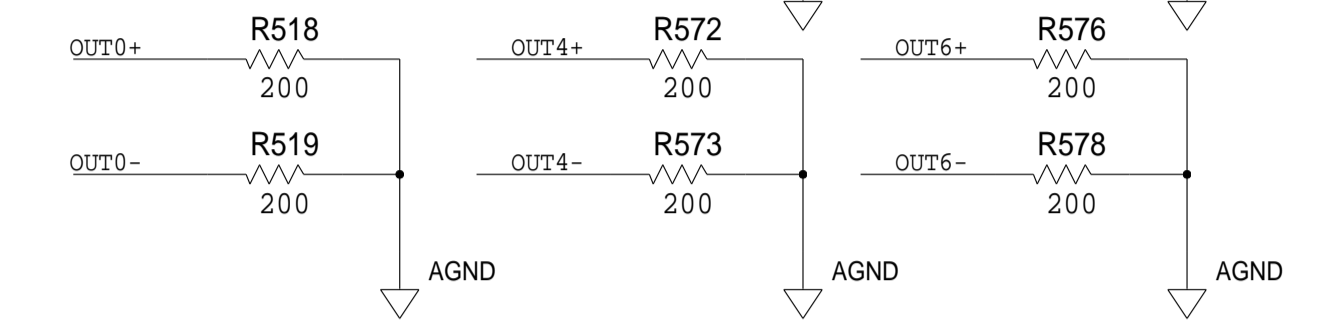
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ACTIVE CLOCK PATH

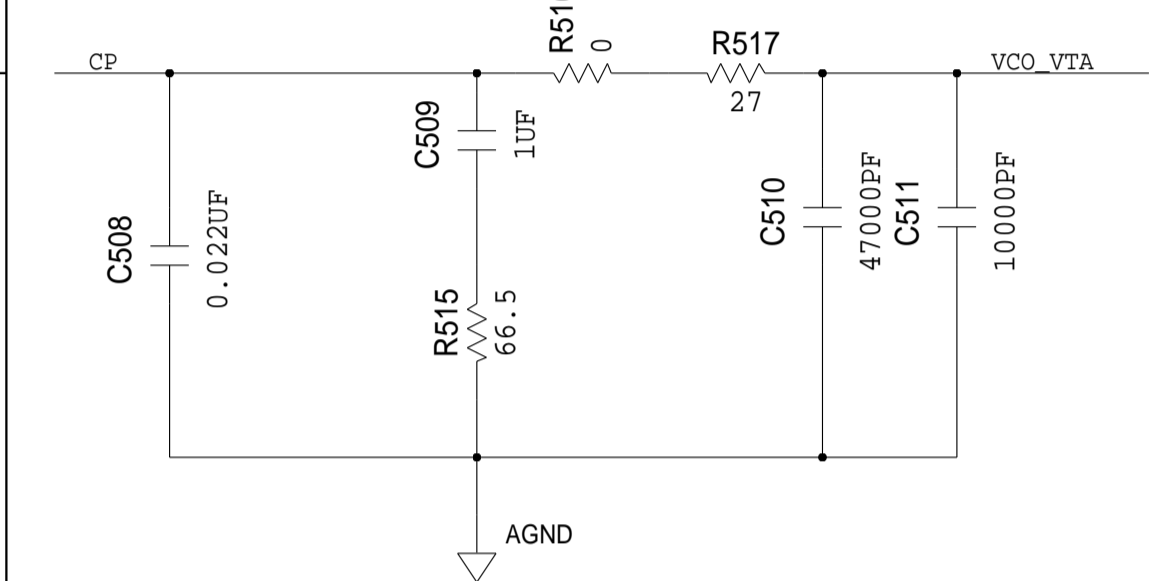
REFERENCE INPUT



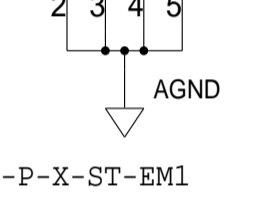
OUTPUT TERMS



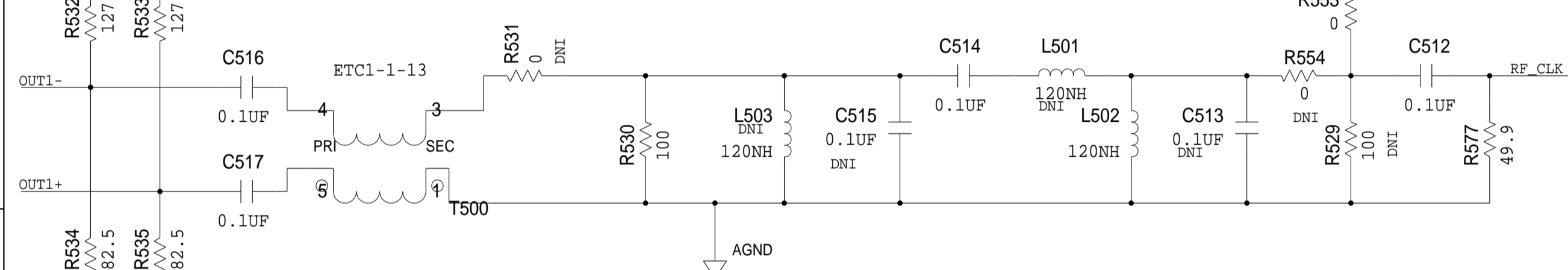
CP / VCO CONNECTION



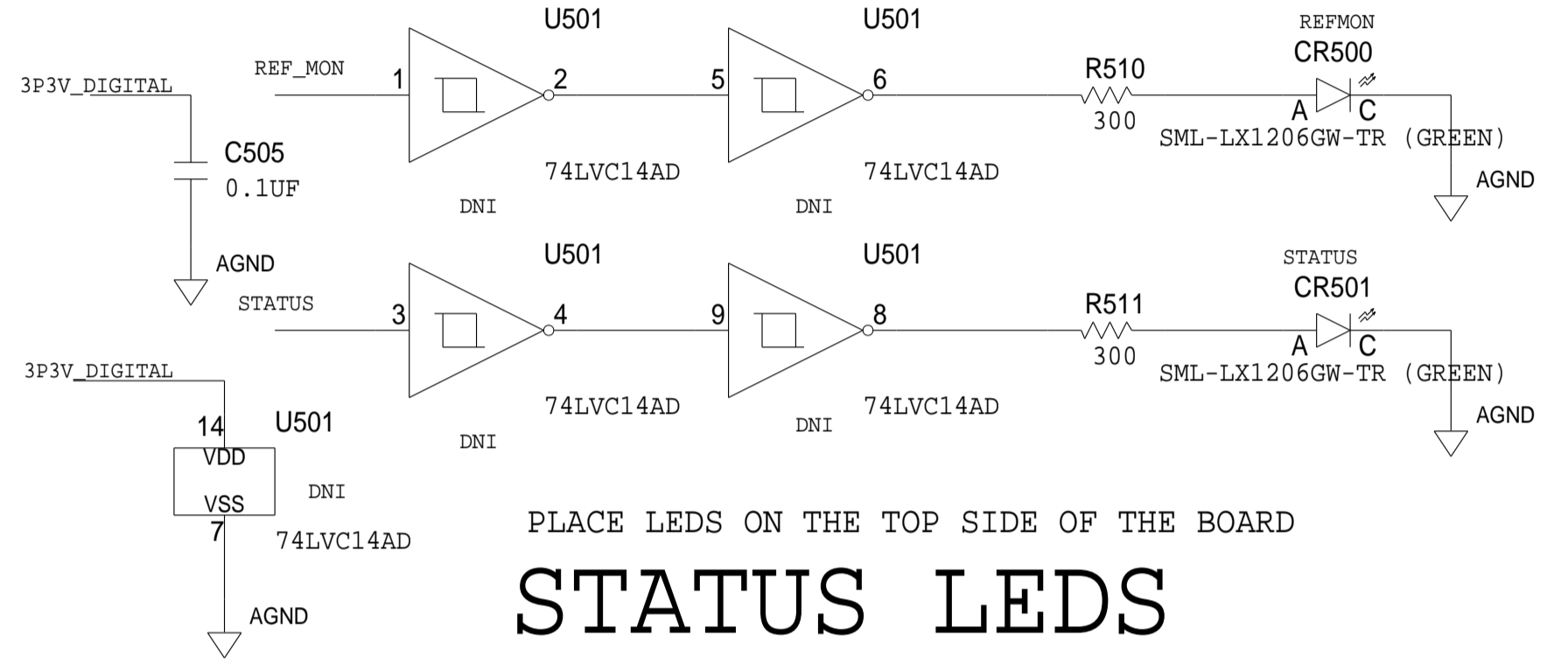
RF_CLK



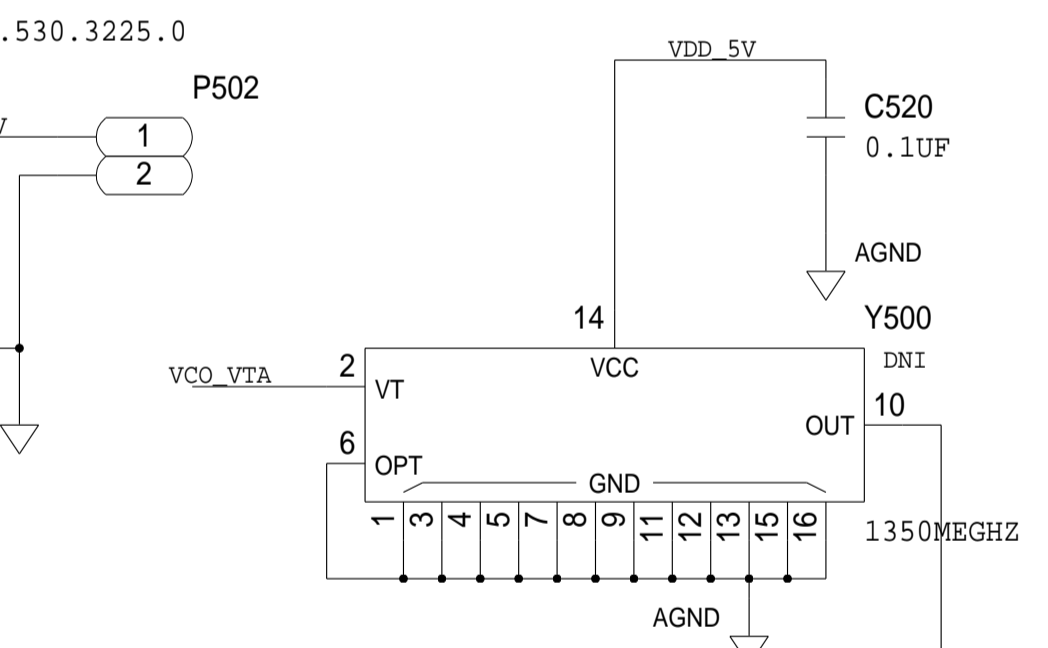
RF CLK OUTPUT



PLACE LEDS ON THE TOP SIDE OF THE BOARD
STATUS LEDS



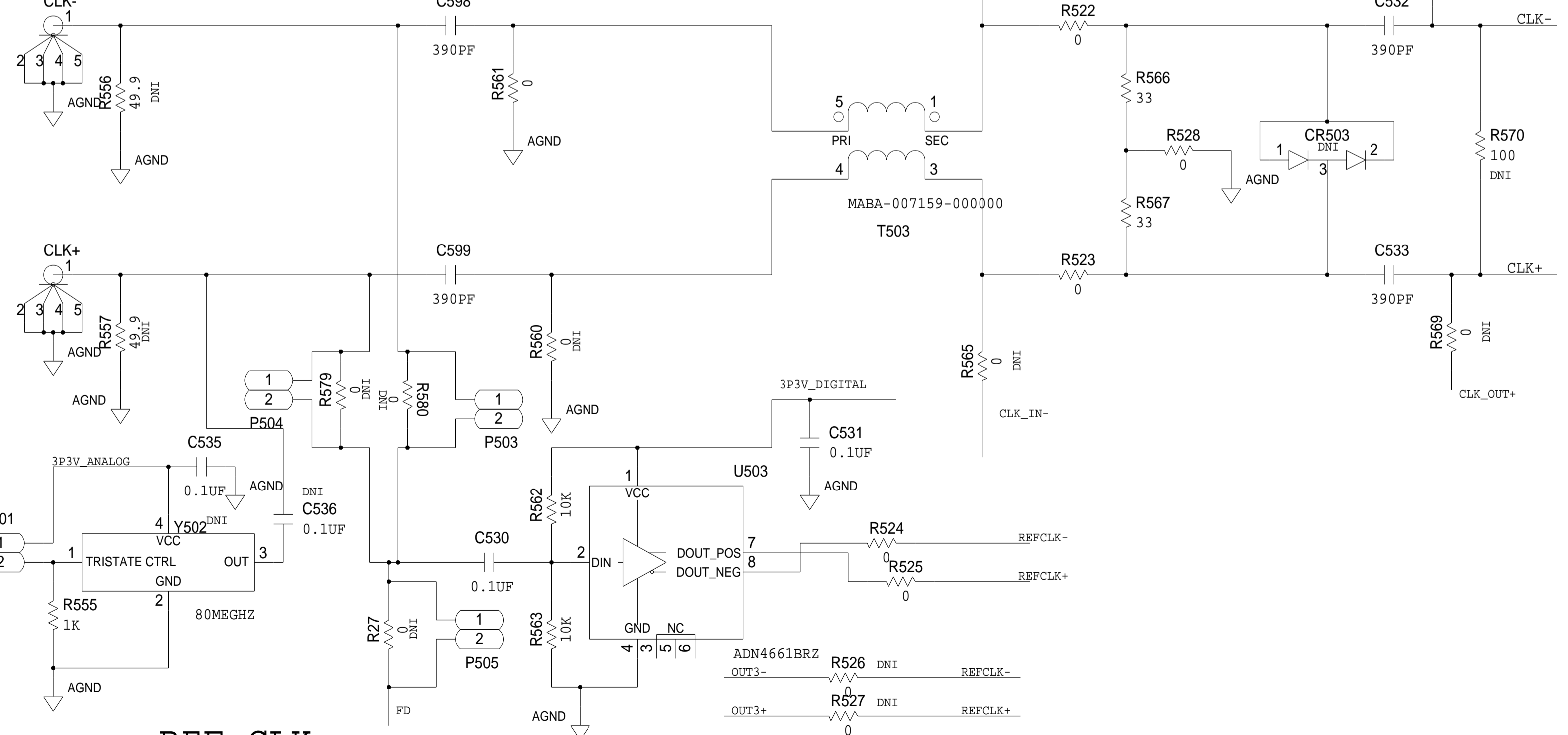
VCO/CLK INPUT



PASSIVE CLOCK

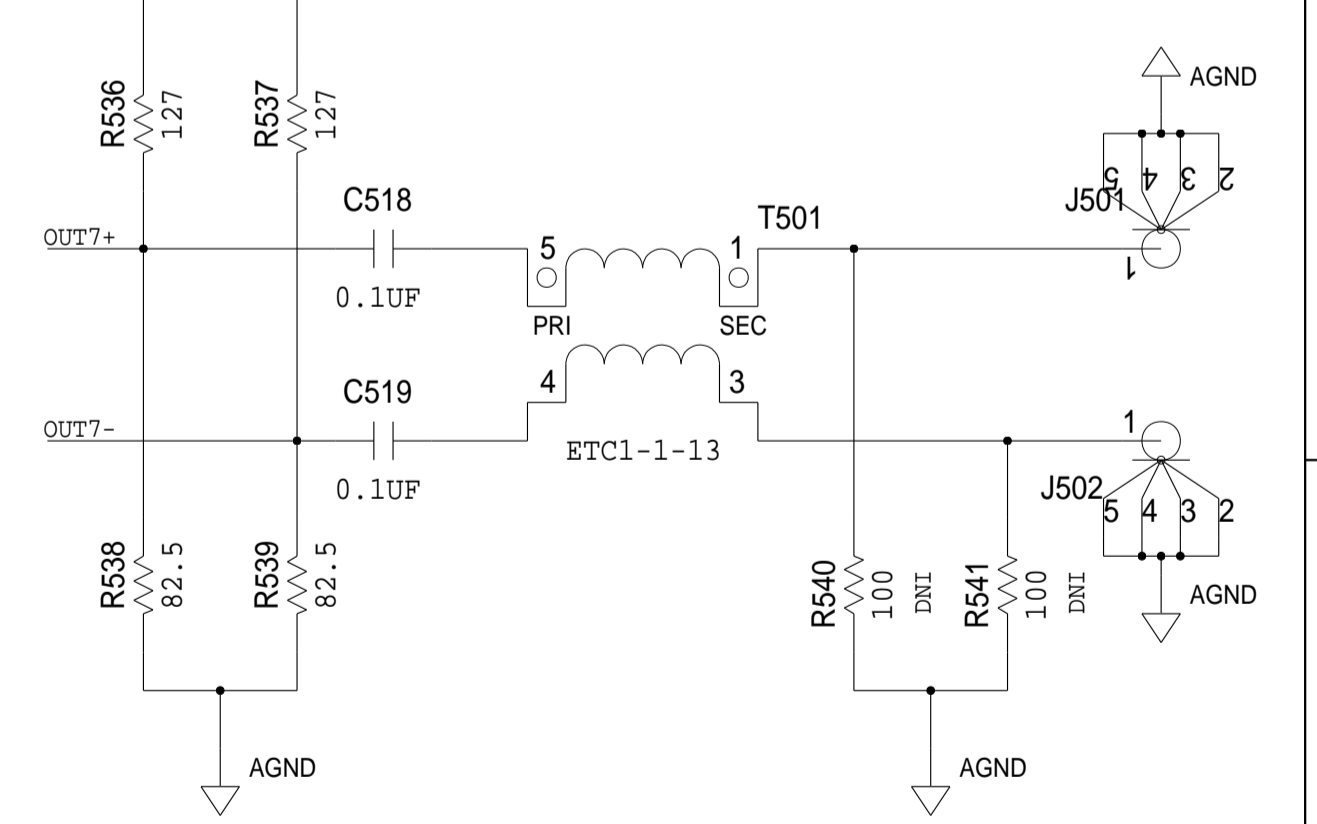
LAYOUT: SMA'S SHOULD BE 575 MILS CENTER TO CENTER
LAYOUT: SHARE PADS WITH ACTIVE CLOCK PATH R'S

CLK

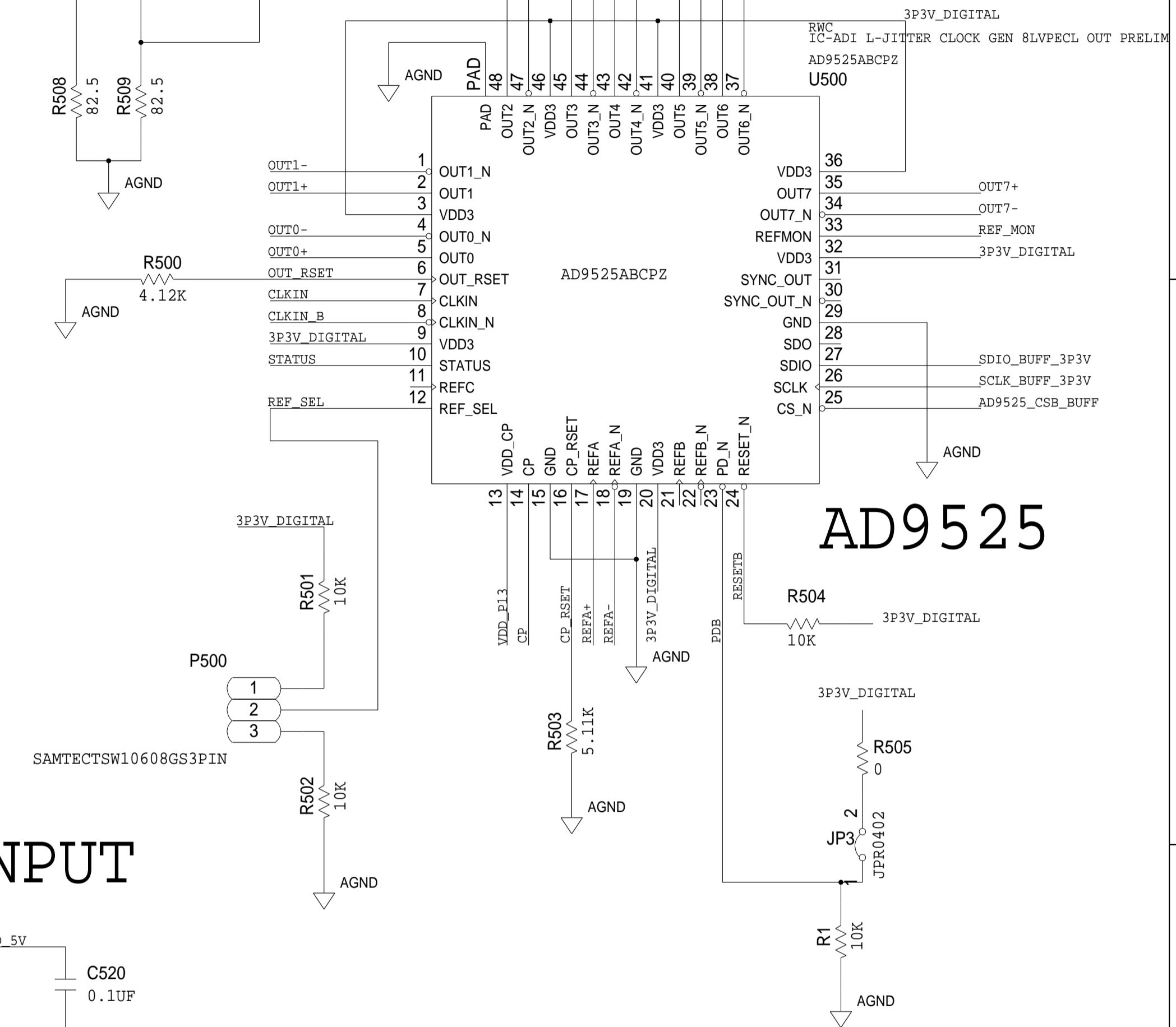


REF CLK

ADDITIONAL CLOCK OUTPUT



AD9525

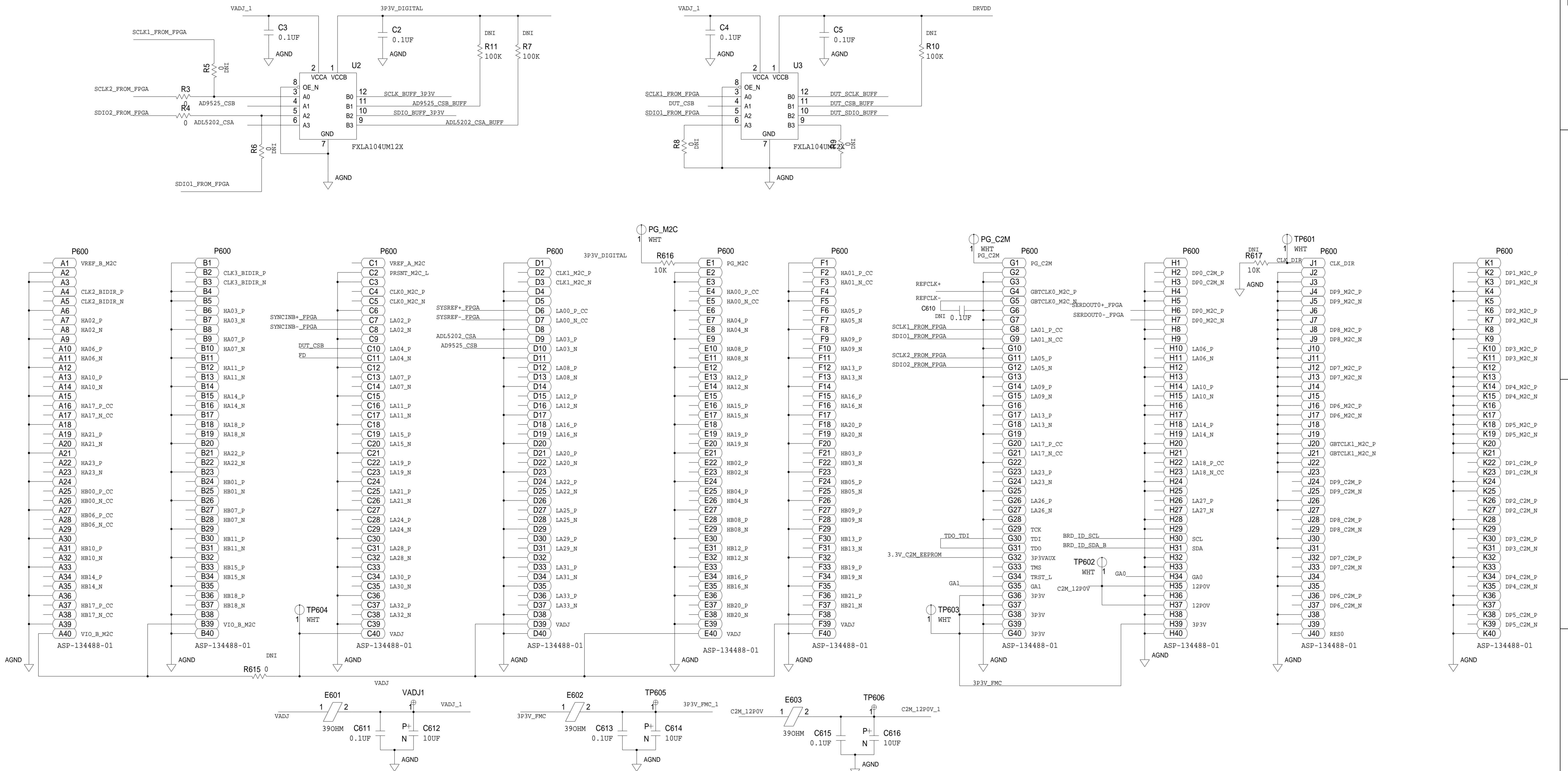


SCHEMATIC			
HW TYPE	Customer Evaluation		
Product(s)	AD9683-250EBZ AD6677		
DESIGN VIEW	-	DRAWING NO.	02_040310
PTD ENGINEER	J. HARRIS	SCALE	1:1
		SHEET	6 OF 7

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FPGA CONN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC			
		HW TYPE : Customer Evaluation Product(s) : AD9683-250EBZ : AD6677	
DESIGN VIEW	-	DRAWING NO.	02_040310
PTD ENGINEER	J. HARRIS	SIZE	D
		SCALE	1:1
		SHEET	7 OF 7
		REV	B

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